DATA SHEET

74F621

Octal bus transceiver, non-inverting (open collector)

Product specification

1996 Jan 05

IC15 Data Handbook

Philips Semiconductors

PHILIPS

Octal bus transceiver, non-inverting (open collector) 74F621

FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Octal bidirectional bus interface
- Open collector outputs sink 64mA
- Non-inverting

DESCRIPTION

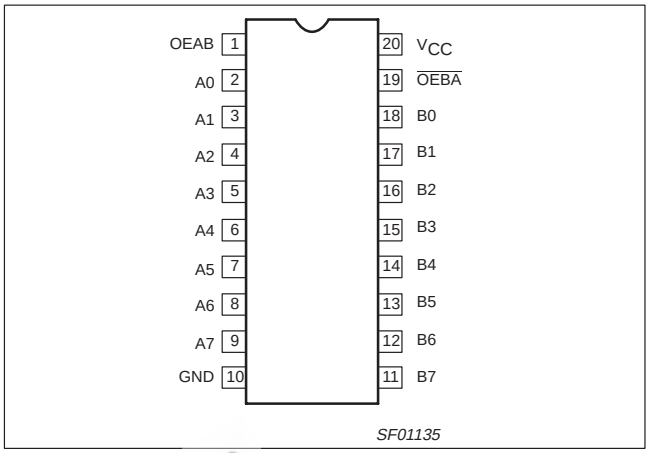
The 74F621 is an octal transceiver featuring non-inverting open collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA, providing very good capacitive drive characteristics.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 74F621 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain in their last states.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F621N	SOT146-1
20-pin plastic SOL	N74F621D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	1.0/0.033	20µA/20µA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20µA/20µA
A0 - A7	Data outputs	OC/40	OC/24mA
B0 - B7	Data outputs	OC/106.7	OC/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state. OC = Open Collector.

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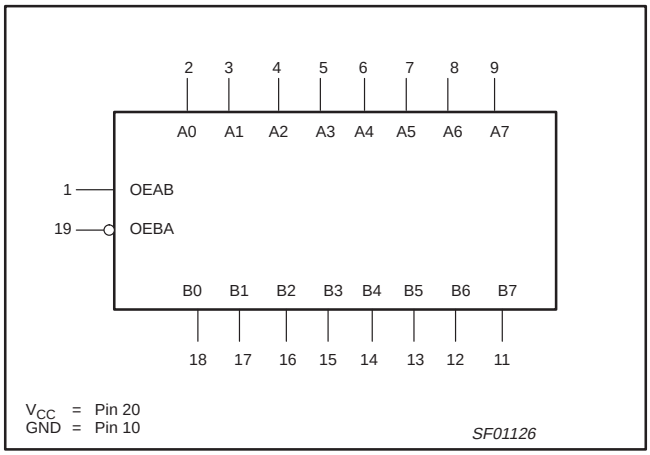
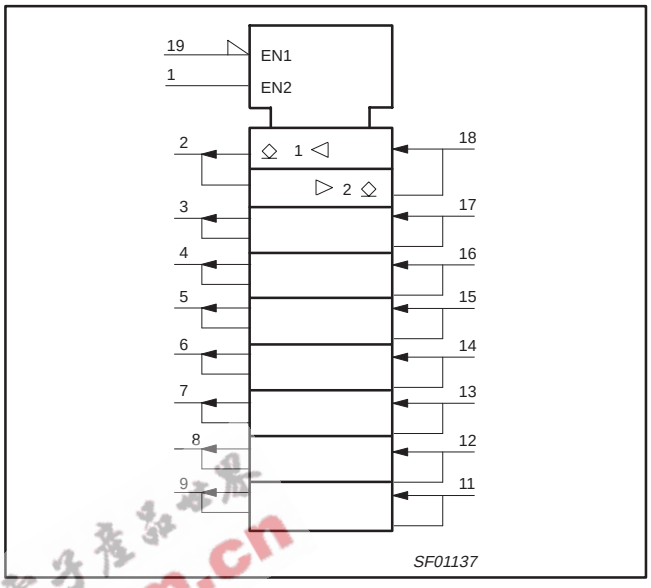
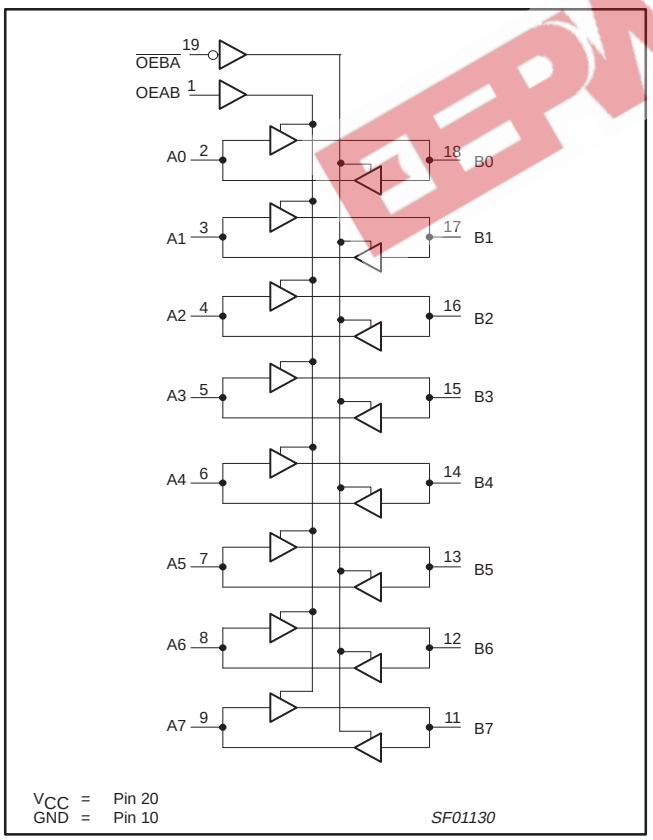
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OPERATING MODES
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	OFF
L	H	B data to A bus
		A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
V_{OH}	High-level output current				4.5	V
I_{OL}	Low-level output current	A0–A7			24	mA
		B0–B7			64	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]			LIMITS MIN	LIMITS TYP NO TAG	LIMITS MAX	UNIT
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH}=MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output voltage	A0–A7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B0–B7		I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$, OEAB	V_{CC} = MAX, V_I = 7.0V					100	µA
		others	V_{CC} = 0.0V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$ = OEAB = A0–A7 = 4.5V			105	140	mA
		I_{CCL}		$\overline{OEBA}$ = OEAB = 4.5V, A0–A7 = GND			105	140	mA

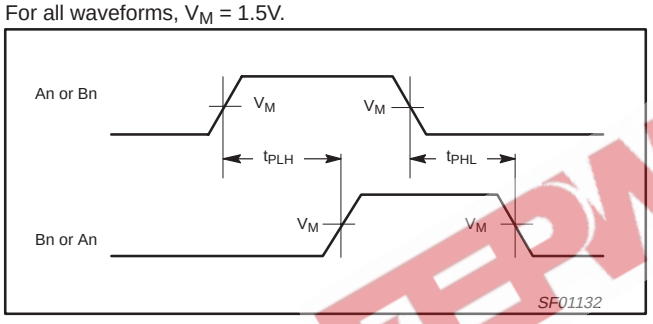
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

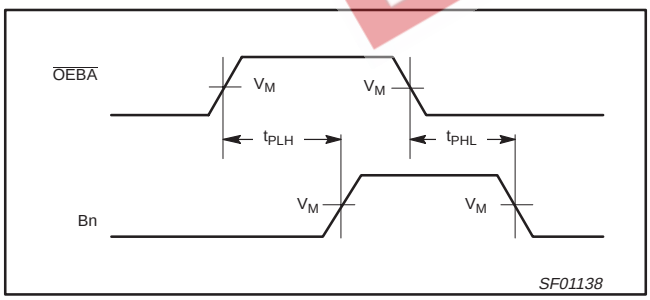
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn	Waveform 1	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay Bn to An	Waveform 1	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to An	Waveform 2	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to Bn	Waveform 3	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

AC WAVEFORMS

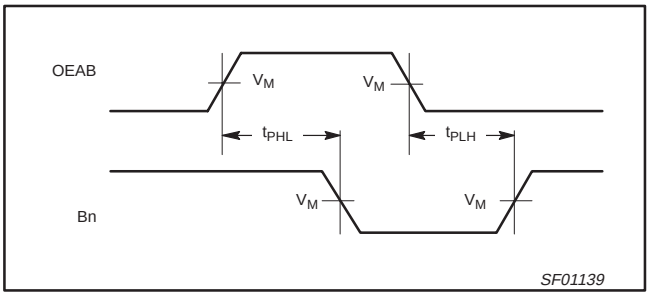
For all waveforms, V_M = 1.5V.



Waveform 1. For Non-Inverting Outputs

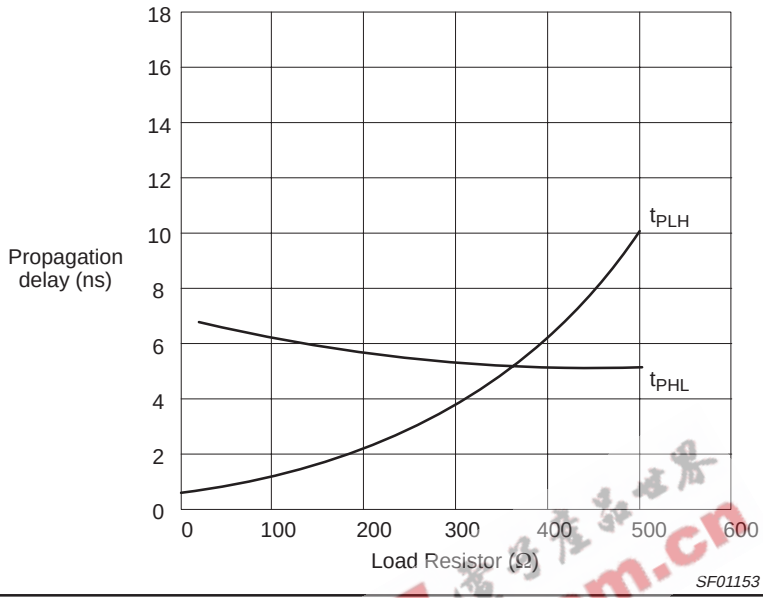


Waveform 2. Propagation Delay, $\overline{OEBA}$ to An



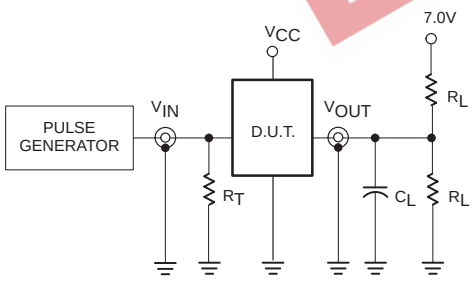
Waveform 3. Propagation Delay, OEAB to Bn

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

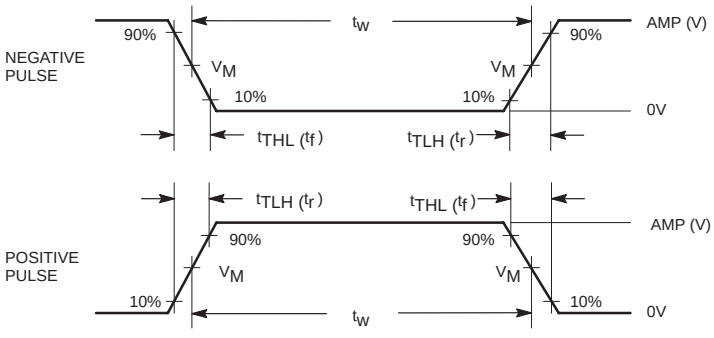


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must take certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



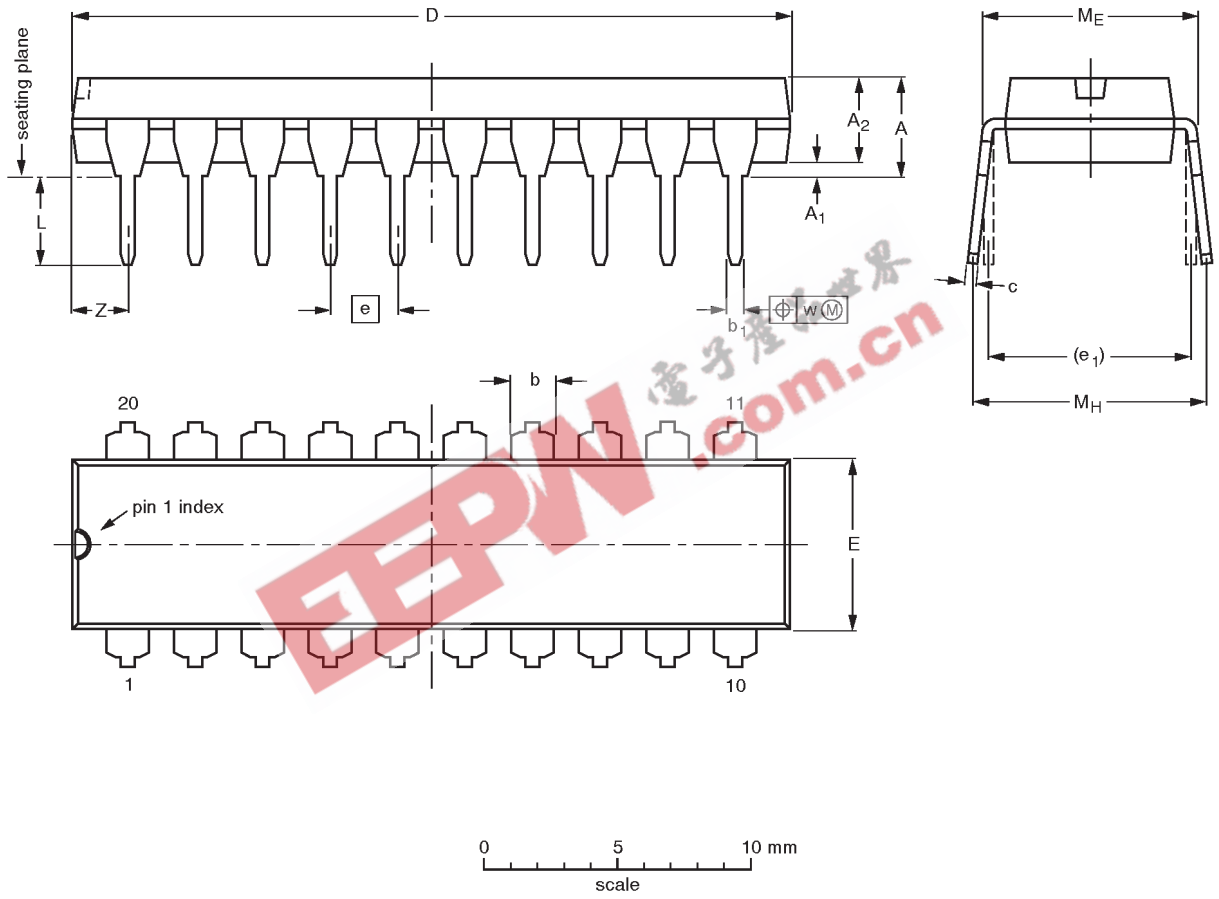
Input Pulse Definition

DEFINITIONS:
R_L = Load resistor;
see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00027

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

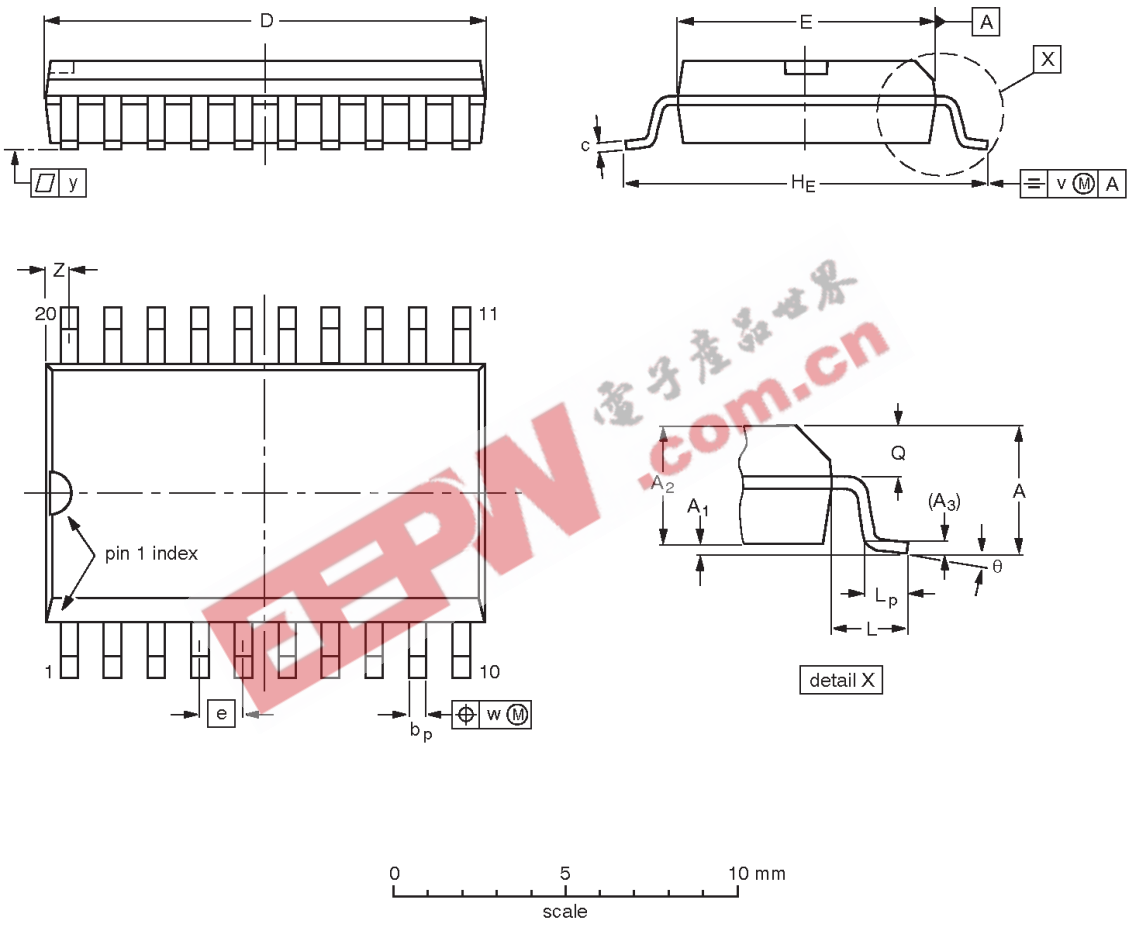
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

NOTES

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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(print code) Date of release: July 1994

Document order number: 9397-750-05147