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Status	Product Specification
ACL Products	

74AC/ACT11623

Octal transceiver with dual enable (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Non-inverting version of '620
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11623 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11623 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		4.8	5.8	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	49	41	pF
			Disabled	9	8	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

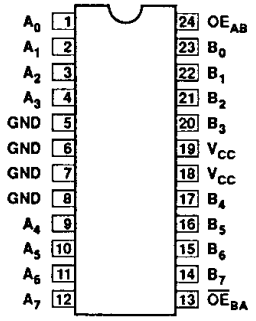
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

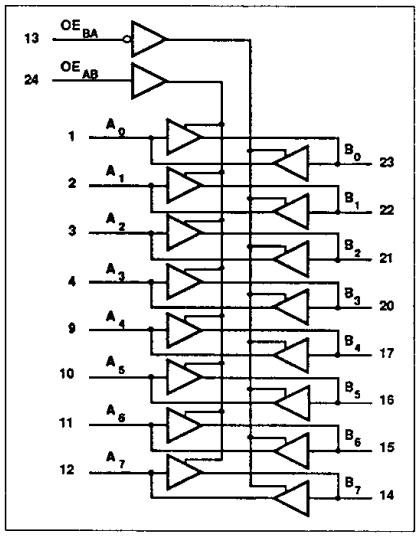
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11623N 74ACT11623N
24-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11623D 74ACT11623D

PIN CONFIGURATION

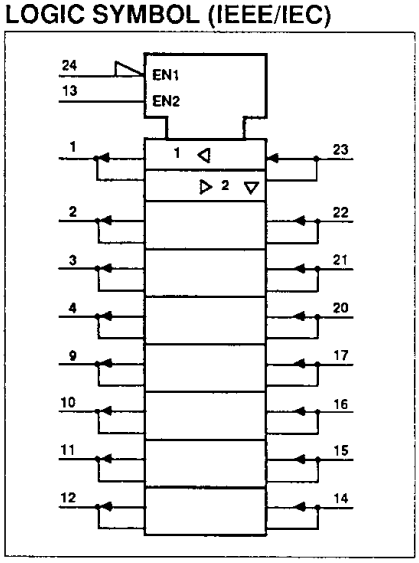
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver with dual enable (3-State)

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control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The Enable inputs can be used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives these transceivers the capability to store data by the simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	OE_{AB}	3-state output enable (active High)
13	$\overline{OE}_{BA}$	3-state output enable (active Low)
1, 2,3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus, A data to B bus

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11623			74ACT11623			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

Octal transceiver with dual enable (3-State)

74AC/ACT11623

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver with dual enable (3-State)

74AC/ACT11623

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11623				74ACT11623				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver with dual enable (3-State) 74AC/ACT11623

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11623					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	1	1.5 1.5	6.8 6.3	9.2 8.2	1.5 1.5	11.4 10.6	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	1	1.5 1.5	6.8 6.3	9.2 8.2	1.5 1.5	11.4 10.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	8.0 7.9	10.6 10.4	1.5 1.5	13.3 12.5	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to B_n	2	1.5 1.5	8.2 8.3	10.4 10.8	1.5 1.5	13.2 13.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	7.0 8.0	8.7 9.9	1.5 1.5	9.7 11.3	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	2	1.5 1.5	7.0 8.0	8.8 9.9	1.5 1.5	9.8 11.1	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

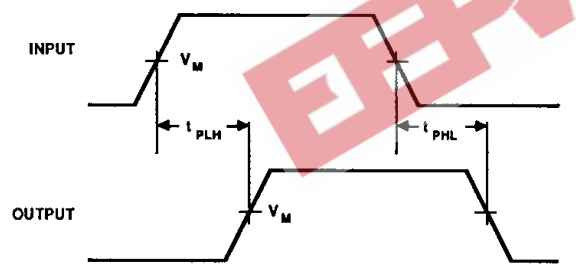
SYMBOL	PARAMETER	WAVEFORM	74AC11623					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	1	1.5 1.5	4.9 4.6	6.8 6.4	1.5 1.5	8.4 7.7	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	1	1.5 1.5	4.9 4.6	6.8 6.4	1.5 1.5	8.4 7.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	5.8 5.9	7.9 8.1	1.5 1.5	9.8 9.9	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to B_n	2	1.5 1.5	6.2 6.1	8.0 8.3	1.5 1.5	10.0 10.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	6.1 6.6	7.7 8.2	1.5 1.5	8.6 9.3	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	2	1.5 1.5	6.2 6.5	7.8 8.1	1.5 1.5	8.7 9.2	ns

Octal transceiver with dual enable (3-State) 74AC/ACT11623

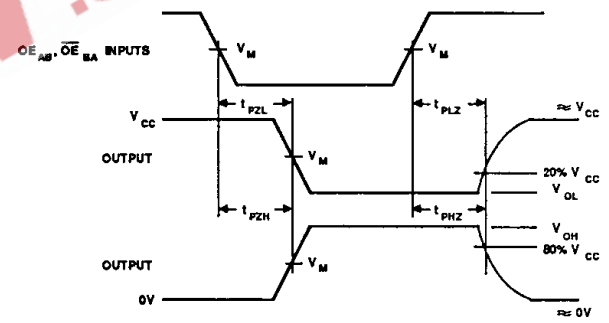
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11623					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	1	1.5 1.5	6.0 5.5	7.5 7.2	1.5 1.5	9.1 8.4	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	1	1.5 1.5	6.0 5.5	7.5 7.2	1.5 1.5	9.1 8.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	6.9 6.9	8.6 9.0	1.5 1.5	10.4 10.6	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to B_n	2	1.5 1.5	7.7 7.7	9.3 9.7	1.5 1.5	11.5 11.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	8.1 8.5	10.0 10.5	1.5 1.5	11.4 12.2	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	2	1.5 1.5	7.1 7.3	8.8 9.2	1.5 1.5	9.8 10.4	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enables (OE_{AB}, $\overline{OE}_{BA}$) and Disable Times

Octal transceiver with dual enable (3-State)

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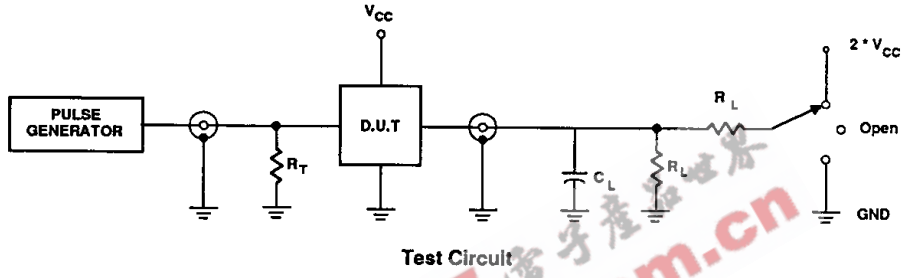
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Document No.	853-1503
ECN No.	00732
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11643

Octal transceiver (3-State) True/INV

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11643 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11643 devices are octal transceivers featuring 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The devices feature an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control. Note that data transmitted from the A side to the B side is inverted and that data transmitted from the B side to the A side is not inverted.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.2	5.7	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	46	41	pF
			Disabled	9.0	9.0	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

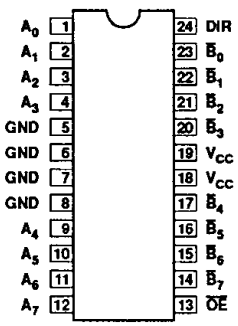
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

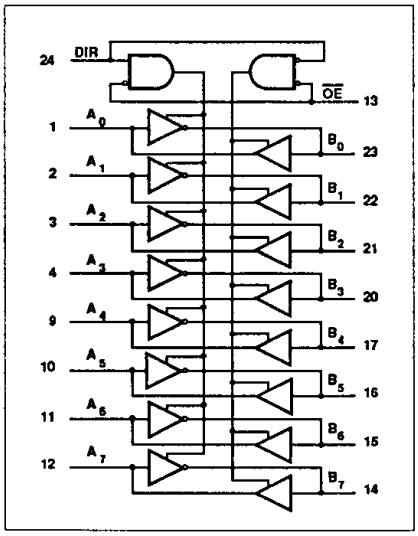
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11643N 74ACT11643N
24-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11643D 74ACT11643D

PIN CONFIGURATION

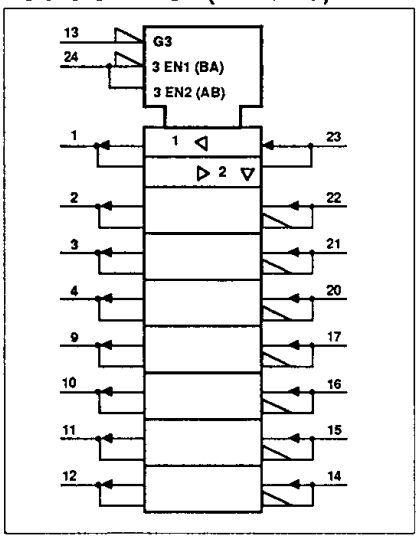
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver (3-State) True/INV

74AC/ACT11643

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
13	$\overline{OE}$	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to $\overline{B}$ bus
H	X	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11643			74ACT11643			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver (3-State) True/INV

74AC/ACT11643

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11643				74ACT11643				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver (3-State) True/INV

74AC/ACT11643

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$, B_n to A_n	1	1.5 1.5	7.4 6.6	10.1 8.7	1.5 1.5	11.3 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.4 8.9	11.8 11.4	1.5 1.5	13.3 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.3 8.9	10.1 10.9	1.5 1.5	10.9 12.0	ns

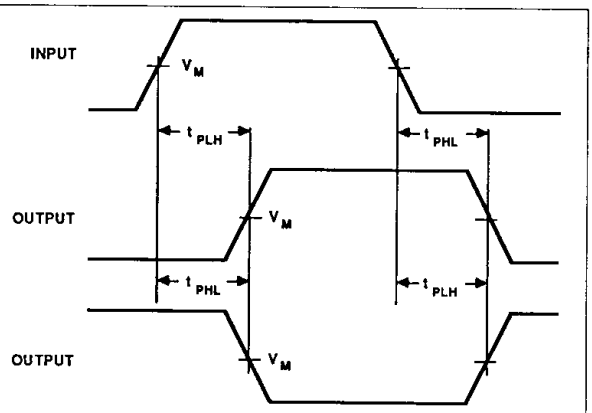
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$, B_n to A_n	1	1.5 1.5	5.4 5.0	7.7 6.8	1.5 1.5	8.6 7.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.0 6.6	9.2 8.7	1.5 1.5	10.4 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.1 7.2	8.8 9.0	1.5 1.5	9.4 9.8	ns

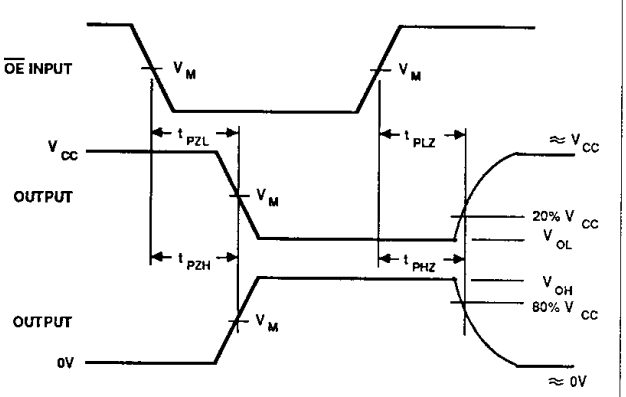
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11643					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$, B_n to A_n	1	1.5 1.5	5.6 5.7	8.3 7.7	1.5 1.5	9.3 8.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.1 7.7	11.5 10.1	1.5 1.5	12.9 11.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.1 9.3	12.0 11.6	1.5 1.5	13.1 12.7	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

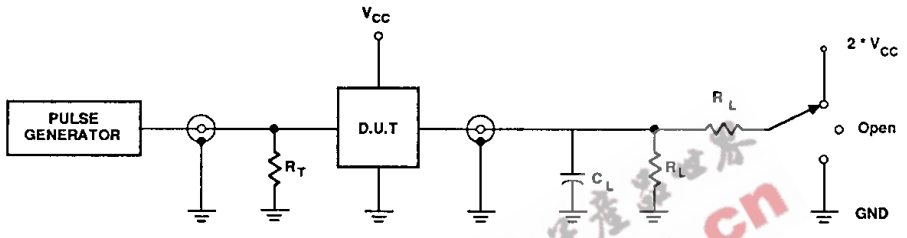
Octal transceiver (3-State) True/INV

74AC/ACT11643

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns