

74ABT2244

Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The ABT2244 is an octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

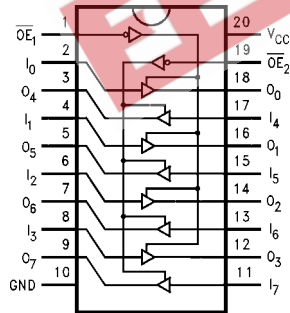
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

| Order Number | Package Number | Package Description |
|---------------|----------------|---|
| 74ABT2244CSC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body |
| 74ABT2244CSJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74ABT2244CMSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide |
| 74ABT2244CMTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ABT2244CPC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices are also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

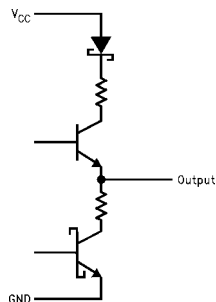
Connection Diagram



Pin Descriptions

| Pin Names | Description |
|------------------------------------|----------------------------------|
| $\overline{OE}_1, \overline{OE}_2$ | Output Enable Input (Active LOW) |
| I_0-I_7 | Inputs |
| O_0-O_7 | Outputs |

Schematic of Each Output



Truth Table

| \overline{OE}_1 | I_{0-3} | O_{0-3} | \overline{OE}_2 | I_{4-7} | O_{4-7} |
|-------------------|-----------|-----------|-------------------|-----------|-----------|
| H | X | Z | H | X | Z |
| L | H | H | L | H | H |
| L | L | L | L | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

| Absolute Maximum Ratings ^(Note 1) | | Recommended Operating Conditions | |
|--|--------------------------------------|---|----------------|
| Storage Temperature | -65°C to +150°C | Free Air Ambient Temperature | -40°C to +85°C |
| Ambient Temperature under Bias | -55°C to +125°C | Supply Voltage | +4.5V to +5.5V |
| Junction Temperature under Bias | -55°C to +150°C | Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V | Data Input | 50 mV/ns |
| Input Voltage (Note 2) | -0.5V to +7.0V | Enable Input | 20 mV/ns |
| Input Current (Note 2) | -30 mA to +5.0 mA | | |
| Voltage Applied to Any Output | | | |
| in the Disabled or | | | |
| Power-off State | -0.5V to 5.5V | | |
| in the HIGH State | -0.5V to V _{CC} | | |
| Current Applied to Output | | | |
| in LOW State (Max) | twice the rated I _{OL} (mA) | | |
| DC Latchup Source Current | | | |
| (Across Comm Operating Range) | -300 mA | | |
| Over Voltage Latchup (I/O) | 10V | | |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|--|-----------------|-----|------|------------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH | 2.5 | | | V | Min | I _{OH} = -3 mA |
| | | 2.0 | | | V | Min | I _{OH} = -32 mA |
| V _{OL} | Output LOW Voltage | | | 0.8 | V | Min | I _{OL} = 15 mA |
| I _{IH} | Input HIGH Current | | | 1 | μA | Max | V _{IN} = 2.7V (Note 4) |
| | | | | 1 | μA | Max | V _{IN} = V _{CC} |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7 | μA | Max | V _{IN} = 7.0V |
| I _{IL} | Input LOW Current | | | -1 | μA | Max | V _{IN} = 0.5V (Note 4) |
| | | | | -1 | μA | Max | V _{IN} = 0.0V |
| V _{ID} | Input Leakage Test | 475 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OZH} | Output Leakage Current | | | 10 | μA | 0 - 5.5V | V _{OUT} = 2.7V; $\overline{OE}n$ = 2.0V |
| I _{OZL} | Output Leakage Current | | | -10 | μA | 0 - 5.5V | V _{OUT} = 0.5V; $\overline{OE}n$ = 2.0V |
| I _{OS} | Output Short-Circuit Current | -100 | | -275 | mA | Max | V _{OUT} = 0.0V |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| I _{ZZ} | Bus Drainage Test | | | 100 | μA | 0.0 | V _{OUT} = 5.5V; All Others GND |
| I _{CCH} | Power Supply Current | | | 50 | μA | Max | All Outputs HIGH |
| I _{CCL} | Power Supply Current | | | 30 | mA | Max | All Outputs LOW |
| I _{CCZ} | Power Supply Current | | | 50 | μA | Max | $\overline{OE}n$ = V _{CC} All Others at V _{CC} or GND |
| I _{CCT} | Additional Outputs Enabled I _{CC} /Input | Outputs Enabled | | 2.5 | mA | | V _I = V _{CC} - 2.1V |
| | | Outputs 3-STATE | | 2.5 | mA | Max | Enable Input V _I = V _{CC} - 2.1V |
| | | Outputs 3-STATE | | 50 | μA | | Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND |
| I _{CCD} | Dynamic I _{CC} (Note 4) | No Load | | 0.1 | mA/ MHz | Max | Outputs OPEN $\overline{OE}n$ = GND (Note 3) One Bit Toggling, 50% Duty Cycle |

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

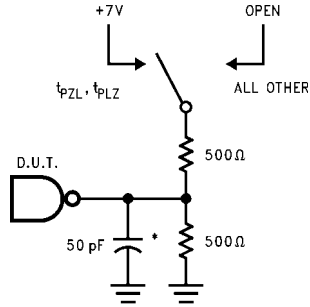
Note 4: Guaranteed, but not tested.

| AC Electrical Characteristics | | | | | | | |
|-------------------------------|-----------------------|---|-----|-----|--|-----|-------|
| (SOIC and SSOP Package) | | | | | | | |
| Symbol | Parameter | T _A = +25°C V _{CC} = +5V C _L = 50 pF | | | T _A = -40°C to +85°C V _{CC} = 4.5V-5.5V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation | 1.0 | 2.2 | 3.9 | 1.0 | 3.9 | ns |
| t _{PHL} | Delay Data to Outputs | 1.0 | 2.9 | 4.4 | 1.0 | 4.4 | |
| t _{PZH} | Output Enable | 1.5 | 3.7 | 6.0 | 1.5 | 6.0 | ns |
| t _{PZL} | Time | 2.1 | 4.3 | 7.0 | 2.1 | 7.0 | |
| t _{PHZ} | Output Disable | 1.7 | 3.5 | 5.8 | 1.7 | 5.8 | ns |
| t _{PLZ} | Time | 1.7 | 3.7 | 5.8 | 1.7 | 5.8 | |

| Capacitance | | | | | |
|---------------------------|--------------------|-----|-------|-------------------------------------|--|
| Symbol | Parameter | Typ | Units | Conditions T _A = 25°C | |
| C _{IN} | Input Capacitance | 5.0 | pF | V _{CC} = 0V | |
| C _{OUT} (Note 5) | Output Capacitance | 9.0 | pF | V _{CC} = 5.0V | |

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

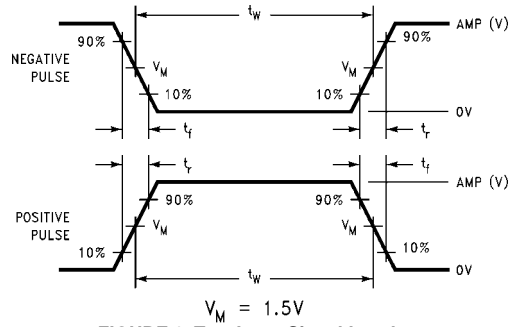


FIGURE 2. Test Input Signal Levels

| Amplitude | Rep. Rate | t_w | t_r | t_f |
|-----------|-----------|--------|--------|--------|
| 3.0V | 1 MHz | 500 ns | 2.5 ns | 2.5 ns |

FIGURE 3. Test Input Signal Requirements

AC Waveforms

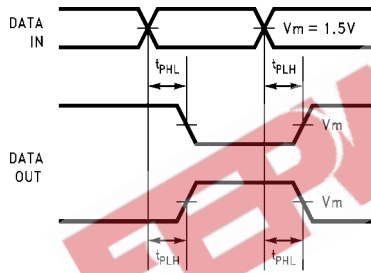


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

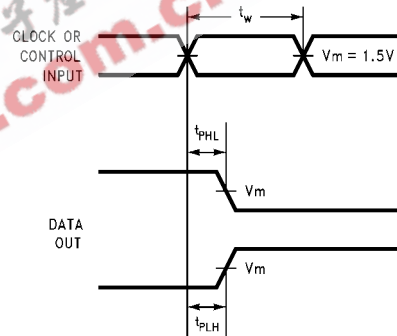


FIGURE 6. Propagation Delay, Pulse Width Waveforms

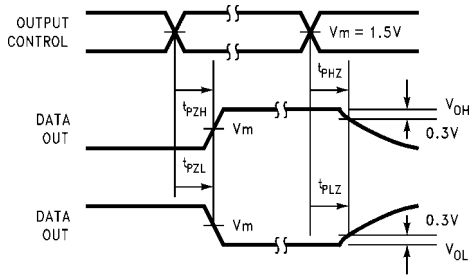


FIGURE 5. 3-STATE Output HIGH and LOW Enable and Disable Times

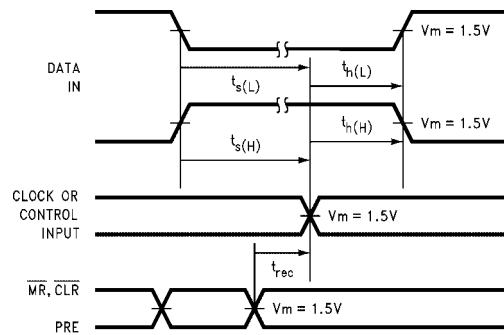
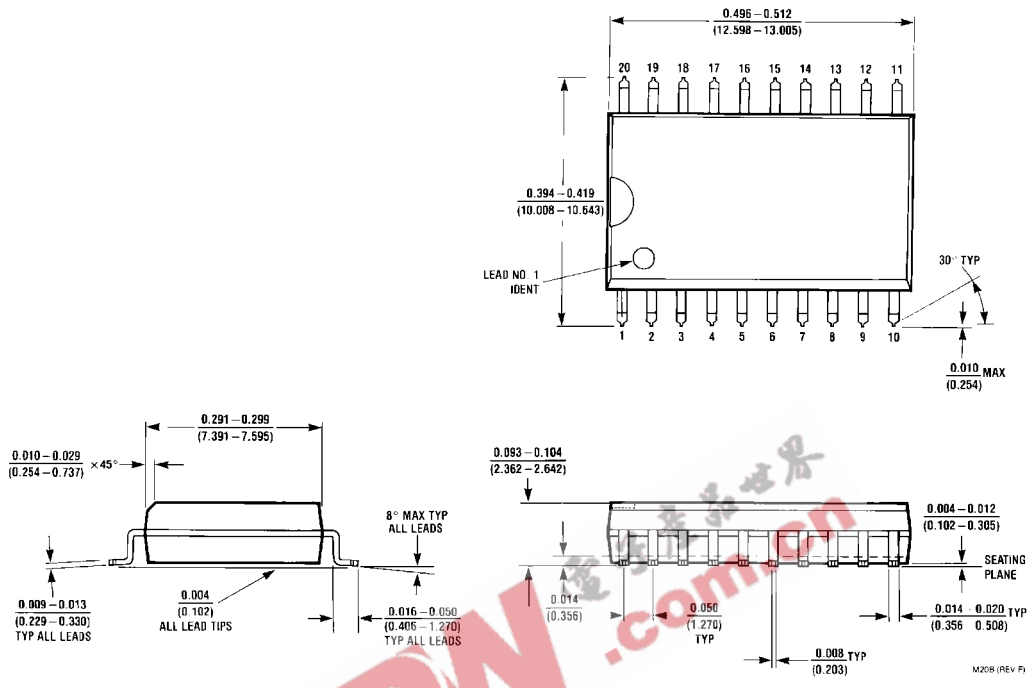


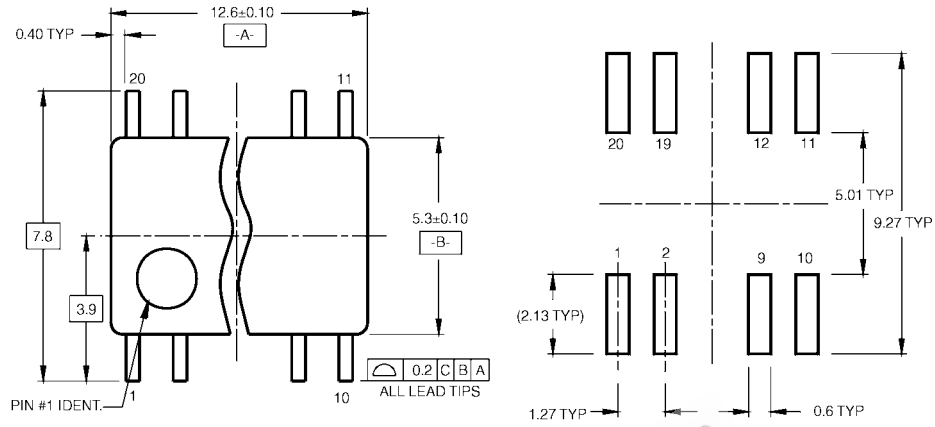
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

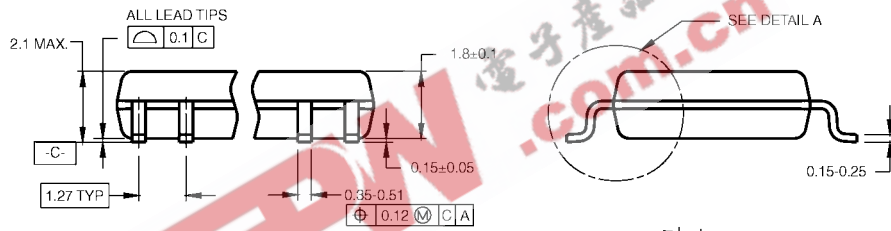


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

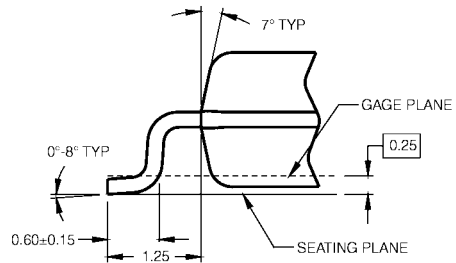


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1996.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

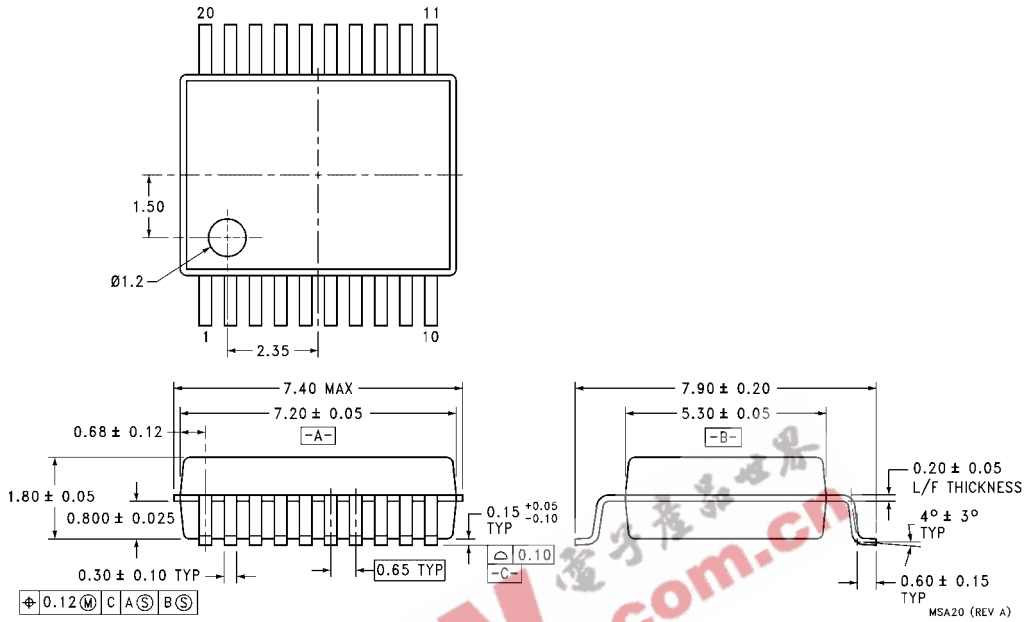
M20DRevB1



DETAIL A

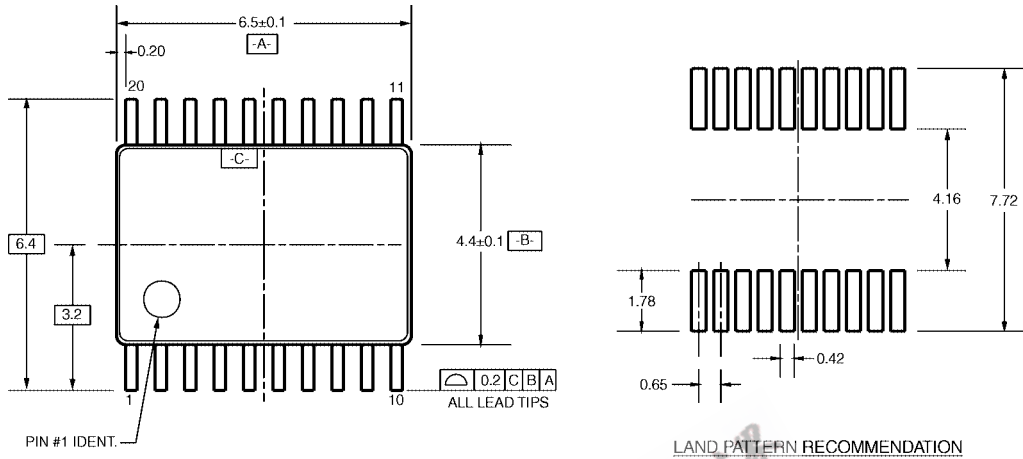
**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



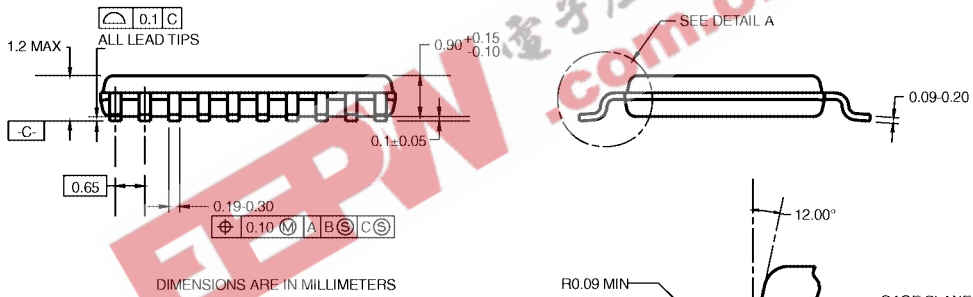
**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



PIN #1 IDENT.

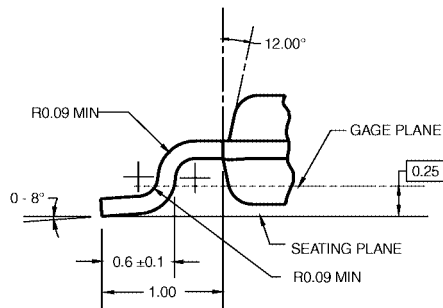
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

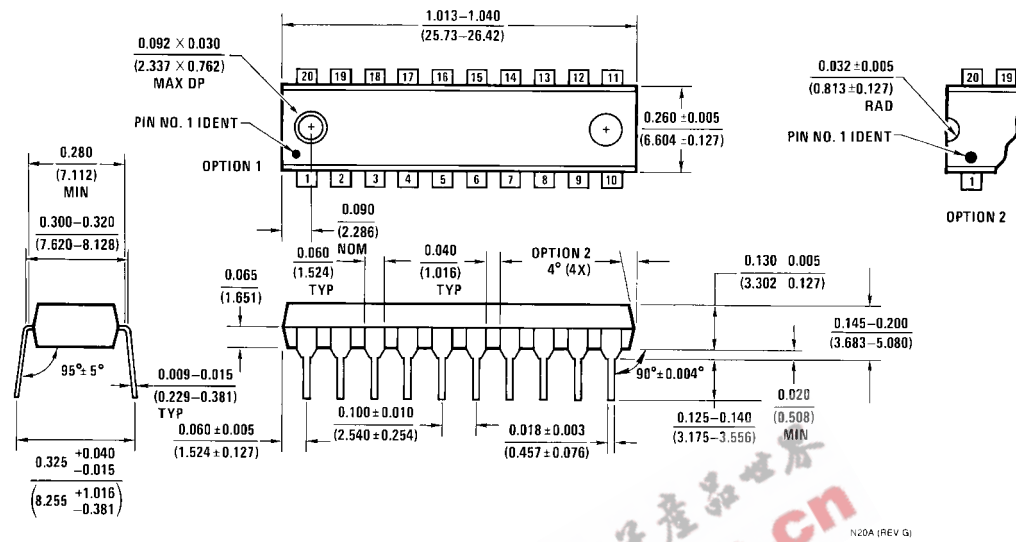
MTC20RevD1



DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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