

74LCXZ245

Low Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The 74LCXZ245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/\bar{R} input determines the direction of data flow through the device. The \overline{OE} input disables both the A and B ports by placing them in a high impedance state.

The 74LCXZ245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation. When V_{CC} is between 0V and 1.5V, the 74LCXZ245 is on the high impedance state during power up or power down. This places the outputs in the high impedance (Z) state preventing intermittent low impedance loading or glitching in bus oriented applications.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 7.0 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

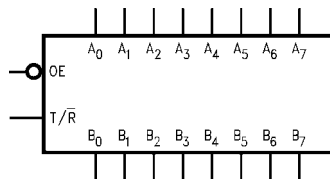
Note 1: To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

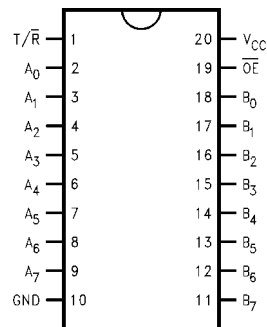
Order Number	Package Number	Package Description
74LCXZ245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCXZ245SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCXZ245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCXZ245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
\overline{OE}	Output Enable Input
T/\bar{R}	Transmit/Receive Input
A_0 – A_7	Side A Inputs or 3-STATE Outputs
B_0 – B_7	Side B Inputs or 3-STATE Outputs

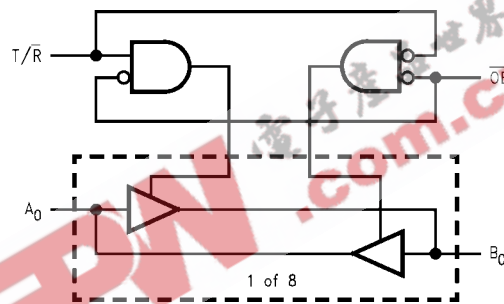
Truth Table

Inputs		Outputs
\overline{OE}	T/\overline{R}	
L	L	Bus B ₀ – B ₇ Data to Bus A ₀ – A ₇
L	H	Bus A ₀ – A ₇ Data to Bus B ₀ – B ₇
H	X	HIGH Z State on A ₀ – A ₇ , B ₀ – B ₇ (Note 2)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Note 2: Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings (Note 3)						
Symbol	Parameter	Value	Conditions	Units		
V _{CC}	Supply Voltage	-0.5 to +7.0		V		
V _I	DC Input Voltage	-0.5 to +7.0		V		
V _O	DC Output Voltage	-0.5 to +7.0 -0.5 to V _{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 4)	V		
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA		
I _{OK}	DC Output Diode Current	-50 +50	V _O < GND V _O > V _{CC}	mA		
I _O	DC Output Source/Sink Current	±50		mA		
I _{CC}	DC Supply Current per Supply Pin	±100		mA		
I _{GND}	DC Ground Current per Ground Pin	±100		mA		
T _{STG}	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 5)						
Symbol	Parameter	Min	Max	Units		
V _{CC}	Supply Voltage	Operating 2.7	3.6	V		
V _I	Input Voltage	0	5.5	V		
V _O	Output Voltage	HIGH or LOW State 0 3-STATE 0	V _{CC} 5.5	V		
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V - 3.6V V _{CC} = 2.7V - 3.0V V _{CC} = 2.3V - 2.7V	±24 ±12 ±8	mA		
T _A	Free-Air Operating Temperature	-40	85	°C		
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V - 2.0V, V _{CC} = 3.0V	0	10	ns/V		
<p>Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 4: I_O Absolute Maximum Rating must be observed.</p> <p>Note 5: Unused inputs or I/O pins must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V _{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 - 3.6	V _{CC} - 0.2		V
		I _{OH} = -8 mA	2.3		1.8	
		I _{OH} = -12 mA	2.7		2.2	
		I _{OH} = -18 mA	3.0		2.4	
		I _{OH} = -24 mA	3.0		2.2	
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 - 3.6		0.2	V
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 - 3.6		±5.0	μA
I _{OZ}	3-STATE I/O Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.3 - 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{PU/PD}	Power Up/ Power Down 3-STATE Output Current	V _O = to V _{CC} V _I = V _{CC} or GND	0 - 1.5		±5.0	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		225	μA
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 6)	2.3 – 3.6		±225	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 – 3.6		500	μA

Note 6: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω				Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		
		C _L = 50 pF		C _L = 50 pF		
		Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	ns
t _{PLH}	A _n to B _n or B _n to A _n	1.5	7.0	1.5	8.0	
t _{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	ns
t _{PZH}	Output Disable Time	1.5	8.5	1.5	9.5	
t _{PLZ}	Output Skew (Note 7)	1.5	7.5	1.5	8.5	ns
t _{PHZ}		1.5	7.5	1.5	8.5	
t _{OSSL}	Output to Output Skew (Note 7)		1.0			ns
t _{OSLH}			1.0			

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8	V
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	25	pF

AC LOADING and WAVEFORMS Generic for LCX Family

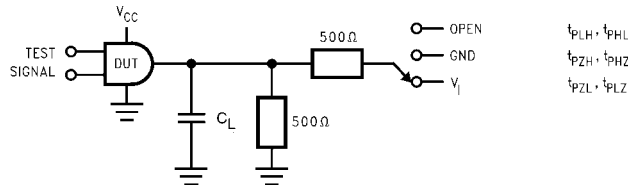
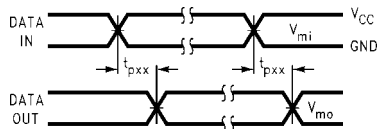
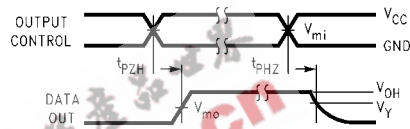


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

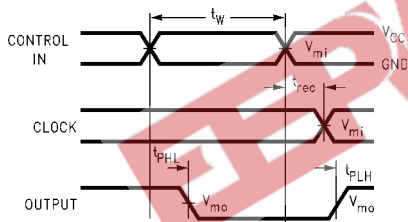
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND



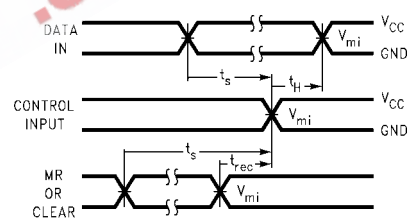
Waveform for Inverting and Non-Inverting Functions



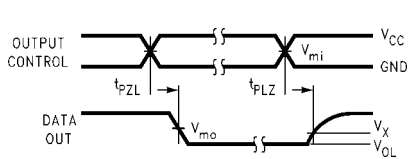
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

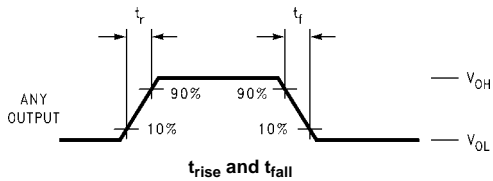
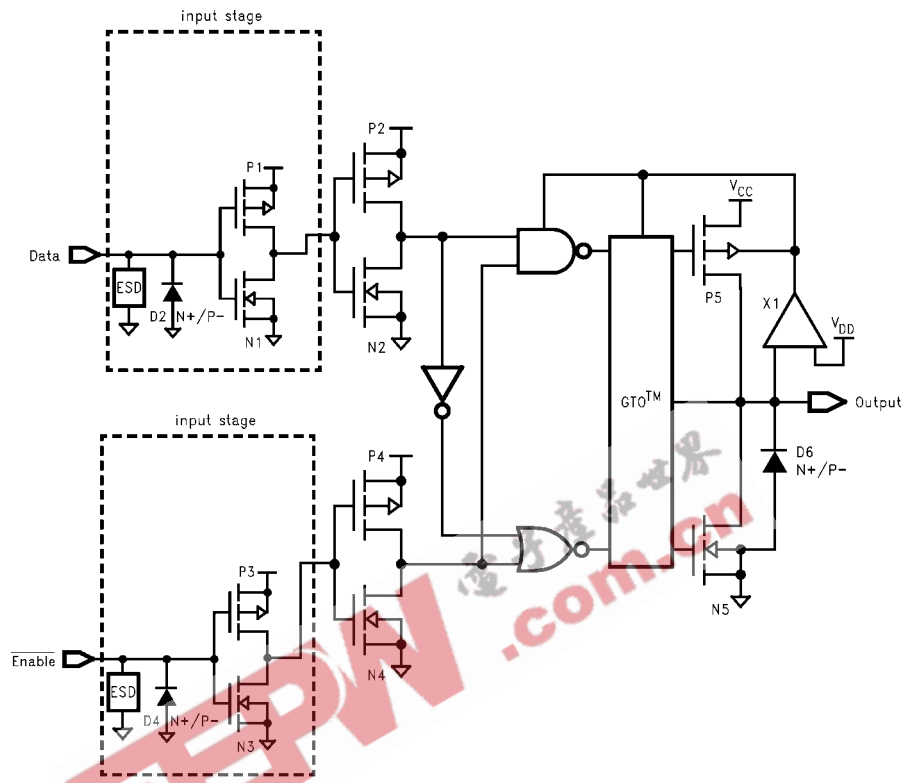


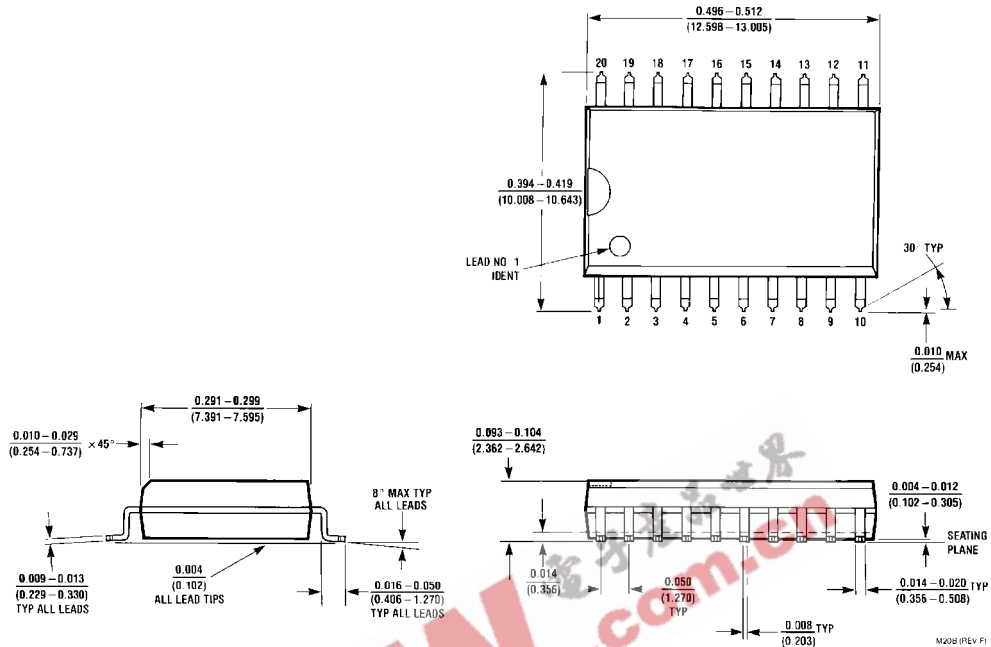
FIGURE 2. Waveforms (Input Characteristics; $f = 1MHz, t_R = t_F = 3ns$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

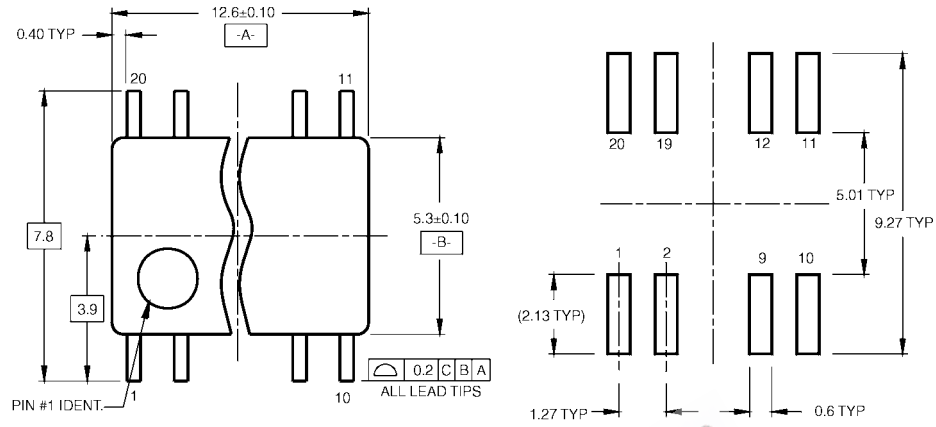


Physical Dimensions inches (millimeters) unless otherwise noted

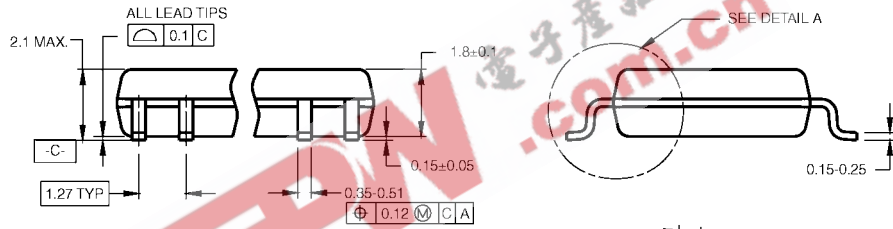


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



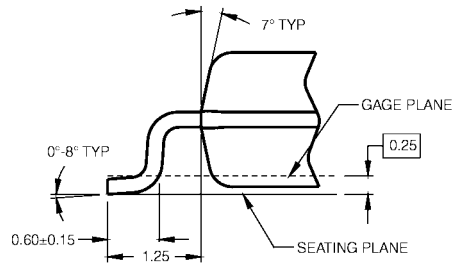
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1996.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

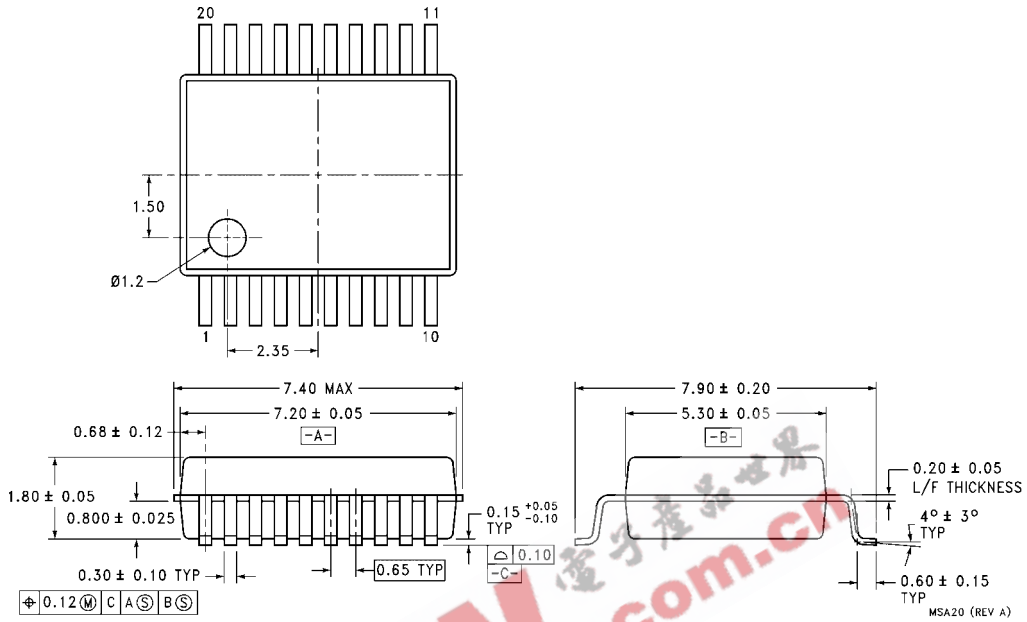
M20DRevB1



DETAIL A

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

PIN #1 IDENT.

LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS

NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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