

# 74F269 8-Bit Bidirectional Binary Counter

## Features

- Synchronous counting and loading
- Built-in lookahead carry capability
- Count frequency 100MHz
- Supply current 113mA typ.
- 300mil slimline package

## General Description

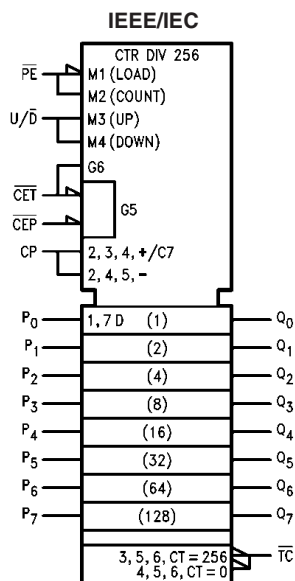
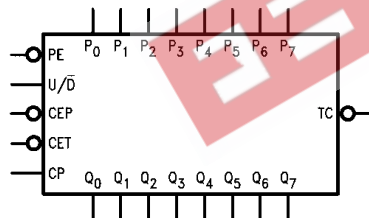
The 74F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a  $U/\bar{D}$  input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

## Ordering Information

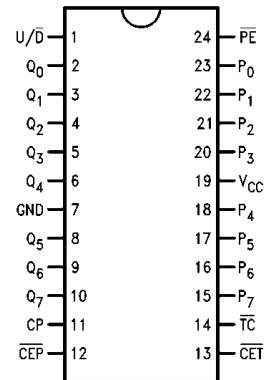
Order Number	Package Number	Package Description
74F269SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F269SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

## Logic Symbols



## Connection Diagram



## Function Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\bar{D}$	CP	Function
L	X	X	X	↗	Parallel Load All Flip-Flops
H	H	X	X	↗	Hold
H	X	H	X	↗	Hold ( $\overline{TC}$ Held High)
H	L	L	H	↗	Count Up
H	L	L	L	↗	Count Down

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = Transition LOW-to-HIGH

## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH / LOW	Input $I_{IH}$ / $I_{IL}$ Output $I_{OH}$ / $I_{OL}$
$P_0$ – $P_7$	Parallel Data Inputs	1.0 / 1.0	20 $\mu$ A / -0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0 / 1.0	20 $\mu$ A / -0.6mA
$U/\overline{D}$	Up-Down Count Control Input	1.0 / 1.0	20 $\mu$ A / -0.6mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0 / 1.0	20 $\mu$ A / -0.6mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0 / 1.0	20 $\mu$ A / -0.6mA
CP	Clock Input	1.0 / 1.0	20 $\mu$ A / -0.6 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	50 / 33.3	-1mA / 20mA
$Q_0$ – $Q_7$	Flip-Flop Outputs	50 / 33.3	-1mA / 20mA

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Logic Diagram

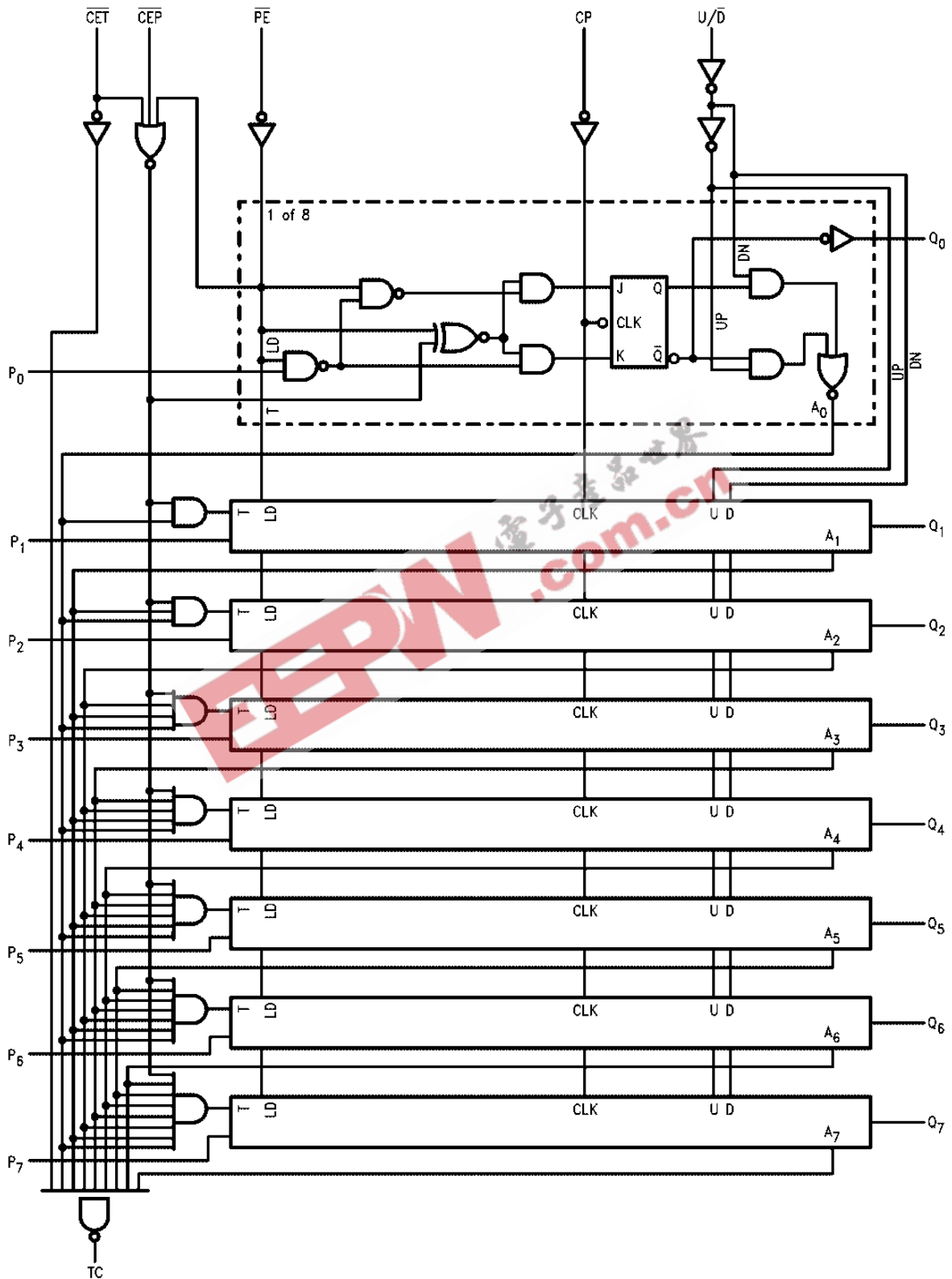


Figure 1.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_A$	Ambient Temperature Under Bias	-55°C to +125°C
$T_J$	Junction Temperature Under Bias	-55°C to +150°C
$V_{CC}$	$V_{CC}$ Pin Potential to Ground Pin	-0.5V to +7.0V
$V_{IN}$	Input Voltage <sup>(1)</sup>	-0.5V to +7.0V
$I_{IN}$	Input Current <sup>(1)</sup>	-30mA to +5.0mA
$V_O$	Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$ )	
	Standard Output	-0.5V to $V_{CC}$
	3-STATE Output	-0.5V to +5.5V
	Current Applied to Output in LOW State (Max.)	twice the rated $I_{OL}$ (mA)

### Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$T_A$	Free Air Ambient Temperature	0°C to +70°C
$V_{CC}$	Supply Voltage	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage		Recognized as a HIGH Signal	2.0			V
V <sub>IL</sub>	Input LOW Voltage		Recognized as a LOW Signal			0.8	V
V <sub>CD</sub>	Input Clamp Diode Voltage	Min.	I <sub>IN</sub> = -18mA			-1.2	V
V <sub>OH</sub>	Output HIGH Voltage 10% V <sub>CC</sub> 5% V <sub>CC</sub>	Min.	I <sub>OH</sub> = -1mA	2.5			V
				2.7			
V <sub>OL</sub>	Output LOW Voltage 10% V <sub>CC</sub>	Min.	I <sub>OL</sub> = 20mA			0.5	V
I <sub>IH</sub>	Input HIGH Current	Max.	V <sub>IN</sub> = 2.7V			5.0	μA
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	Max.	V <sub>IN</sub> = 7.0V			7.0	μA
I <sub>CEX</sub>	Output HIGH Leakage Current	Max.	V <sub>OUT</sub> = V <sub>CC</sub>			50	μA
V <sub>ID</sub>	Input Leakage Test	0.0	I <sub>ID</sub> = 1.9μA, All Other Pins Grounded	4.75			V
I <sub>OD</sub>	Output Leakage Circuit Current	0.0	V <sub>IOD</sub> = 150mV, All Other Pins Grounded			3.75	μA
I <sub>IL</sub>	Input LOW Current	Max.	V <sub>IN</sub> = 0.5V			-0.6	mA
I <sub>OS</sub>	Output Short-Circuit Current	Max.	V <sub>OUT</sub> = 0.0V	-60		-150	mA
I <sub>CCH</sub>	Power Supply Current	Max.	V <sub>O</sub> = HIGH		104	125	mA
I <sub>CCL</sub>	Power Supply Current	Max.	V <sub>O</sub> = LOW		113	135	mA

## AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$ , $V_{CC} = +5.0\text{V}$ , $C_L = 50\text{pF}$			$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ , $V_{CC} = +5.0\text{V}$ , $C_L = 50\text{pF}$		Units
		Min.	Typ.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Count Frequency		100				MHz
$t_{PLH}$	Propagation Delay, CP to $Q_n$ (Count-Up)	3.5		8.0	3.5	7.0	ns
$t_{PHL}$	CP to $Q_n$ (Count-Up)	4.5		10.5	4.5	11.0	
$t_{PLH}$	Propagation Delay, U/ $\bar{D}$ to $\bar{TC}$	3.5		7.5	3.5	10.0	ns
$t_{PHL}$	U/ $\bar{D}$ to $\bar{TC}$	4.5		7.5	4.5	11.0	
$t_{PLH}$	Propagation Delay, $\overline{CET}$ to $\bar{TC}$	3.5		7.0	3.5	10.5	ns
$t_{PHL}$	$\overline{CET}$ to $\bar{TC}$	3.0		10.5	3.0	11.5	
$t_{PLH}$	Propagation Delay, CP to $\bar{TC}$	4.5		10.0	4.5	10.5	ns
$t_{PHL}$	CP to $\bar{TC}$	5.0		10.0	4.5	10.5	
$t_{PLH}$	Propagation Delay, CP to $Q_n$ (Count-Down)	3.5		10.5	3.5	11.0	ns
$t_{PHL}$	CP to $Q_n$ (Count-Down)	4.5		10.5	4.5	11.0	
$t_{PLH}$	Propagation Delay, CP to $Q_n$ (Load)	3.5		7.0	3.5	10.0	ns
$t_{PHL}$	CP to $Q_n$ (Load)	4.0		7.0	4.0	7.0	

## AC Operating Requirements

Symbol	Parameter	$T_A = +25^\circ\text{C}$ , $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ , $V_{CC} = +5.0\text{V}$		Units
		Min.	Max.	Min.	Max.	
$t_S(H)$	Setup Time, HIGH or LOW, Data to CP	3.5		4.0		ns
$t_S(L)$	Data to CP	3.0		3.0		
$t_H(H)$	Hold Time, HIGH or LOW, Data to CP	1.0		2.0		ns
$t_H(L)$	Data to CP	1.0		1.0		
$t_S(H)$	Setup Time, HIGH or LOW, $\overline{PE}$ to CP	5.5		6.5		ns
$t_S(L)$	$\overline{PE}$ to CP	5.5		6.5		
$t_H(H)$	Hold Time, HIGH or LOW, $\overline{PE}$ to CP	0		0		ns
$t_H(L)$	$\overline{PE}$ to CP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW, $\overline{CET}$ or $\overline{CEP}$ to CP	6.0		6.5		ns
$t_S(L)$	$\overline{CET}$ or $\overline{CEP}$ to CP	8.0		9.0		
$t_H(H)$	Hold Time, HIGH or LOW, $\overline{CET}$ or $\overline{CEP}$ to CP	0		0		ns
$t_H(L)$	$\overline{CET}$ or $\overline{CEP}$ to CP	0		0		
$t_W(H)$	Clock Pulse Width, HIGH or LOW	3.5		3.5		ns
$t_W(L)$		3.5		4.0		
$t_S(H)$	Setup Time, HIGH or LOW, U/ $\bar{D}$ to CP	8.0		9.5		ns
$t_S(L)$	U/ $\bar{D}$ to CP	6.0		7.0		
$t_H(H)$	Hold Time, HIGH or LOW, U/ $\bar{D}$ to CP	0.0		0.0		ns
$t_H(L)$	U/ $\bar{D}$ to CP	0.0		0.0		



**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.

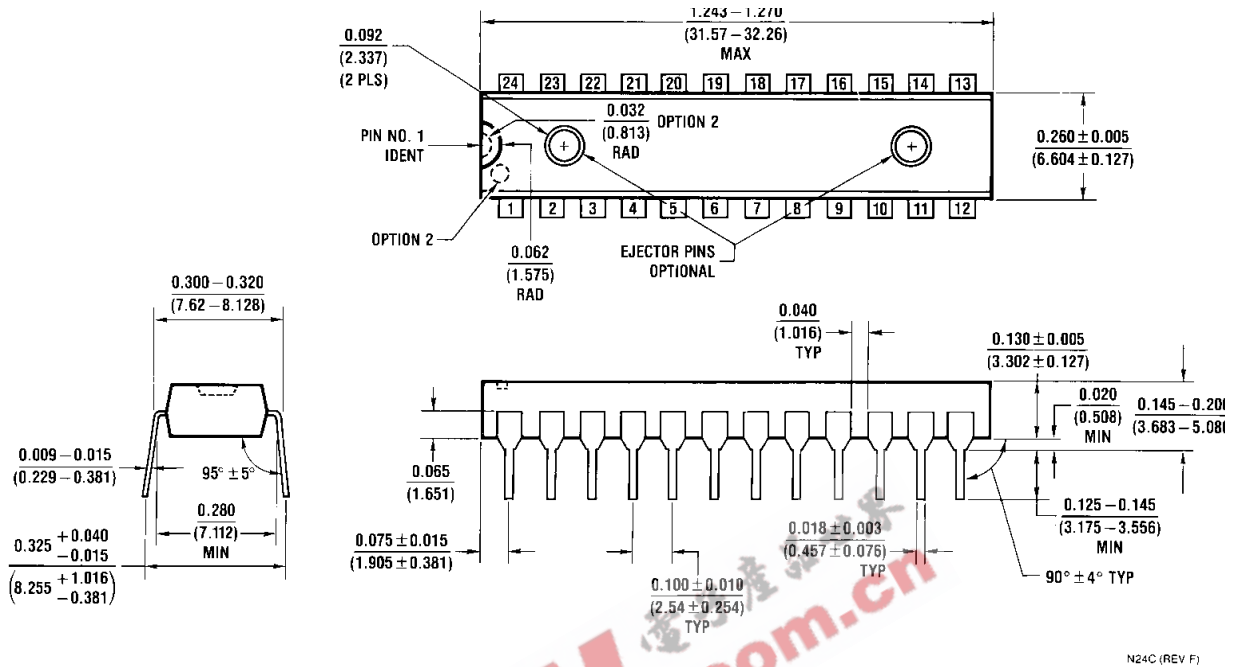


Figure 3. 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N24C

N24C (REV F)





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Rev. I24