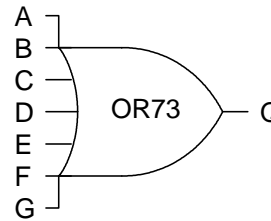


OR73 is a 7-input OR gate with 3x drive strength.

Truth Table

A	B	C	D	E	F	G	Q
L	L	L	L	L	L	L	L
H	X	X	X	X	X	X	H
X	H	X	X	X	X	X	H
X	X	H	X	X	X	X	H
X	X	X	H	X	X	X	H
X	X	X	X	H	X	X	H
X	X	X	X	X	H	X	H
X	X	X	X	X	X	H	H



Capacitance

	C _i (pF)
A	0.046
B	0.043
C	0.048
D	0.044
E	0.041
F	0.043
G	0.048

Area

1.35 mils²

Power

6.28 μW/MHz

Delay [ns] = tpd.. = f(SL, L)

with SL = Input Slope [ns]; L = Output Load [pF]

Output Slope [ns] = op_sl.. = f(L)

with L = Output Load [pF]

AC Characteristics : T_j = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.3	L = 2.1	L = 3.0	L = 0.3	L = 2.1	L = 3.0
Delay A to Q	tpdar	0.69	2.12	2.86	0.94	2.38	3.04
	tpdaf	0.58	1.56	2.01	0.82	1.77	2.26
Delay B to Q	tpdbr	0.76	2.21	2.87	1.05	2.50	3.23
	tpdbf	0.66	1.63	2.08	0.79	1.75	2.25
Delay C to Q	tpdcr	0.87	2.30	2.99	1.10	2.52	3.20
	tpdcf	0.67	1.65	2.12	0.77	1.73	2.23
Delay D to Q	tpddr	0.66	2.13	2.84	0.92	2.38	3.02
	tpddf	0.70	1.75	2.20	0.94	1.98	2.44
Delay E to Q	tpder	0.74	2.21	2.89	1.00	2.43	3.23
	tpdef	0.82	1.87	2.32	0.97	2.01	2.47
Delay F to Q	tpdfr	0.80	2.32	2.97	1.07	2.57	3.27
	tpdff	0.88	1.91	2.38	0.98	2.03	2.48
Delay G to Q	tpdgr	0.86	2.35	3.04	1.13	2.60	3.36
	tpdgf	0.89	1.92	2.38	0.96	2.00	2.47
Output Slope A to Q	op_slar	1.02	5.30	7.28	1.03	5.23	7.32
	op_slaf	0.68	3.51	4.76	0.67	3.53	4.85

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.3	L = 2.1	L = 3.0	L = 0.3	L = 2.1	L = 3.0
Output Slope B to Q	op_slbr	1.03	5.26	7.32	1.05	5.26	7.37
	op_slbf	0.70	3.42	4.87	0.71	3.52	4.88
Output Slope C to Q	op_slcr	1.03	5.26	7.26	1.07	5.20	7.36
	op_slcf	0.67	3.52	4.80	0.66	3.46	4.85
Output Slope D to Q	op_slcr	1.01	5.45	8.03	0.96	5.45	7.96
	op_slcf	0.80	3.52	5.01	0.81	3.52	5.01
Output Slope E to Q	op_slcr	1.01	5.51	8.00	1.01	5.62	7.83
	op_slcf	0.82	3.53	5.02	0.82	3.61	4.82
Output Slope F to Q	op_slfr	1.03	5.51	8.02	1.00	5.57	7.93
	op_slff	0.82	3.60	4.87	0.82	3.56	4.85
Output Slope G to Q	op_slgr	1.03	5.56	7.91	1.03	5.66	7.80
	op_slgf	0.82	3.53	4.80	0.80	3.55	4.90

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