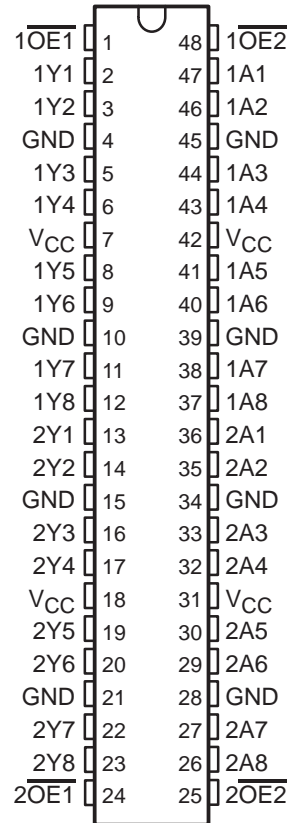


# SN54AHCT16541, SN74AHCT16541 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Inputs Are TTL-Voltage Compatible
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54AHCT16541 . . . WD PACKAGE  
SN74AHCT16541 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'AHCT16541 devices are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ( $1OE1$  and  $1OE2$  or  $2OE1$  and  $2OE2$ ) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHCT16541 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHCT16541 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each 8-bit buffer/driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



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 **TEXAS  
INSTRUMENTS**

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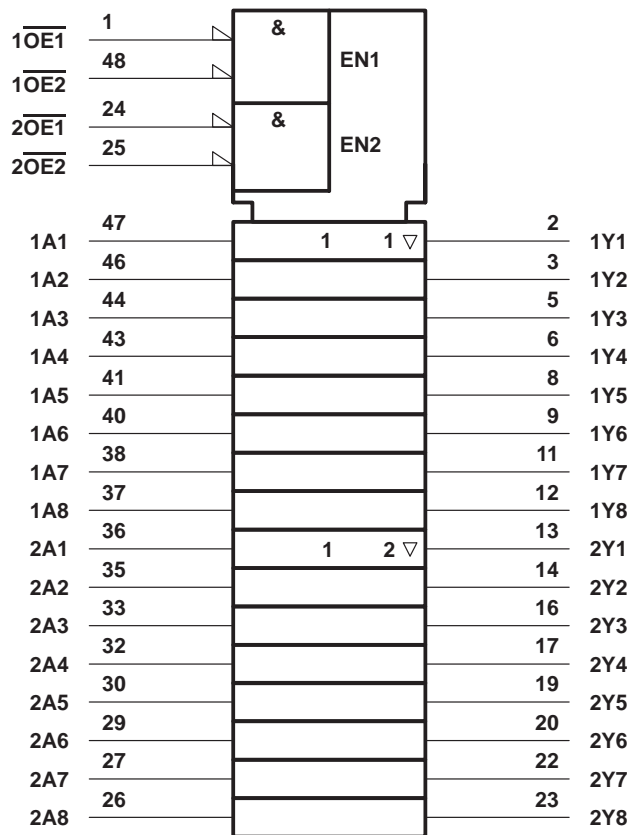
# SN54AHCT16541, SN74AHCT16541

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

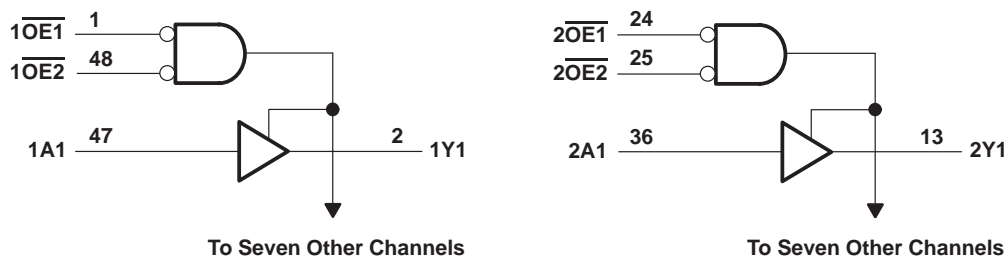
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#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



# SN54AHCT16541, SN74AHCT16541 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through each $V_{CC}$ or GND .....	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	70°C/W
DGV package .....	58°C/W
DL package .....	63°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

	SN54AHCT16541		SN74AHCT16541		UNIT
	MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		2		V
$V_{IL}$ Low-level input voltage		0.8		0.8	V
$V_I$ Input voltage	0	5.5	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–8		–8	mA
$I_{OL}$ Low-level output current		8		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20		20	ns/V
$T_A$ Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AHCT16541, SN74AHCT16541

## 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT16541		SN74AHCT16541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1			0.1	V	
	I <sub>OL</sub> = 8 mA				0.36		0.44	0.44		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	±2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40	40	μA	
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2	10		10	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			3				pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHCT16541		SN74AHCT16541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF		5.4**	8.5**	1**	10**	1	9.5	ns
t <sub>PHL</sub>					5.4**	8.5**	1**	10**	1	9.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		7.7**	10.4**	1**	12**	1	12	ns
t <sub>PZL</sub>					7.7**	10.4**	1**	12**	1	12	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 15 pF		4.5**	10.4**	1**	12**	1	12	ns
t <sub>PLZ</sub>					4.5**	10.4**	1**	12**	1	12	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF		6.2	9.5	1	11	1	10.5	ns
t <sub>PHL</sub>					6	9.5	1	11	1	10.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		7.5	11.4	1	13	1	13	ns
t <sub>PZL</sub>					7.5	11.4	1	13	1	13	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF		7	11.4	1	13	1	13	ns
t <sub>PLZ</sub>					7	11.4	1	13	1	13	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1***			1	ns	

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

\*\*\* On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER	SN74AHCT16541			UNIT
	MIN	TYP	MAX	
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		0.6		V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>		-0.3		V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>		4.6		V
V <sub>IH(D)</sub> High-level dynamic input voltage	2			V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

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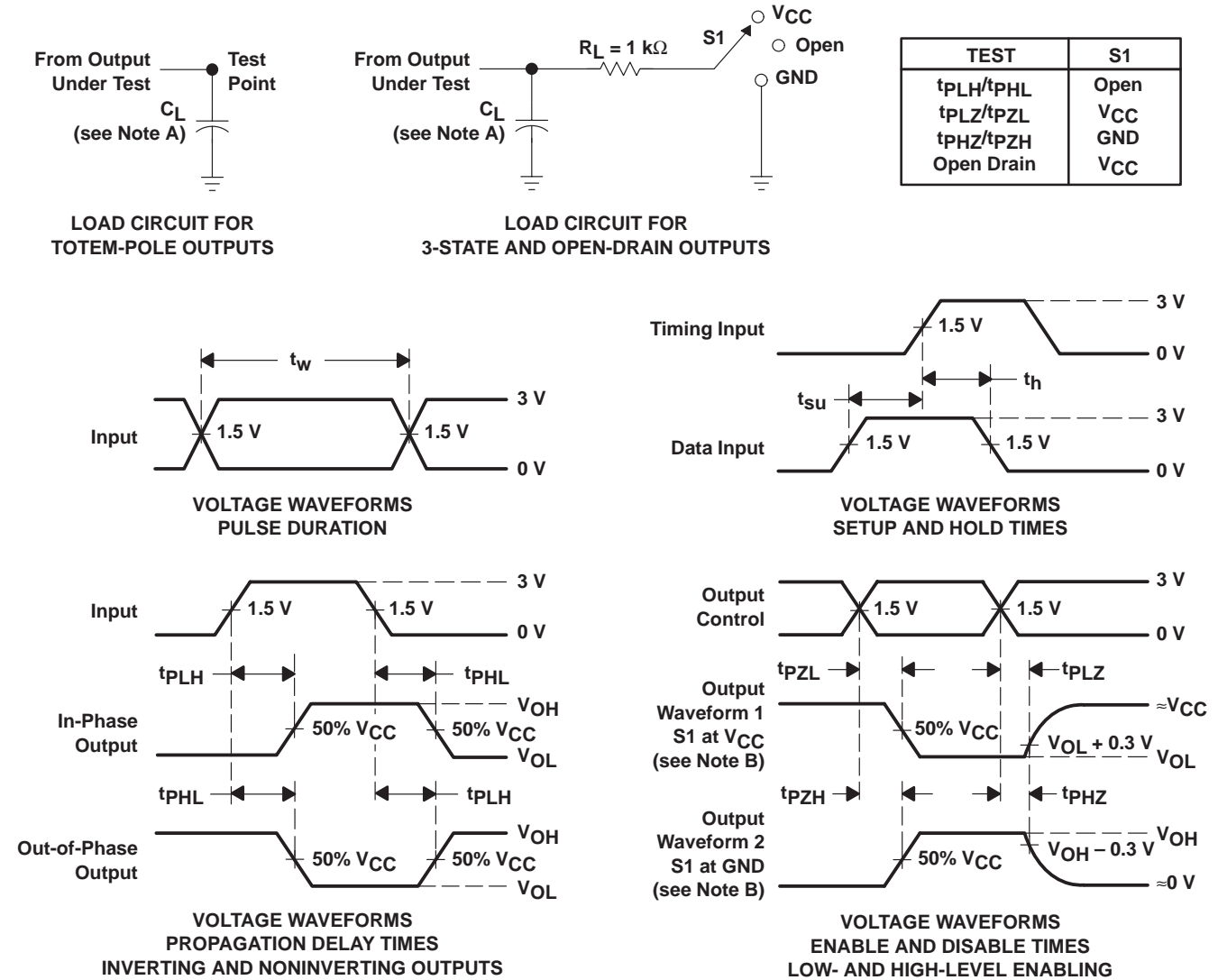


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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74AHCT16541DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16541DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16541DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16541DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHCT16541DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16541DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16541DGV	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16541DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16541DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT16541DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

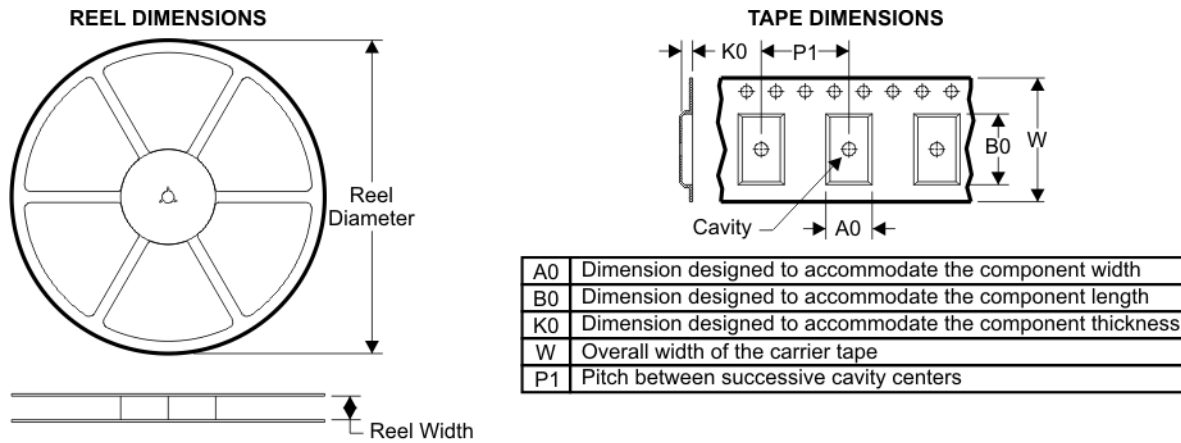
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

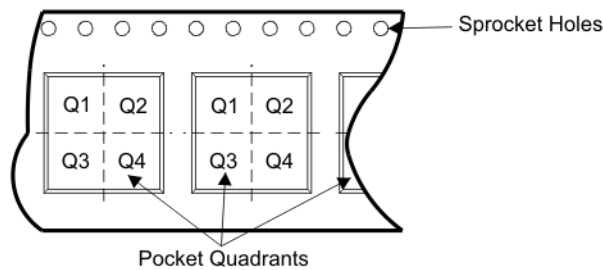
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**TAPE AND REEL BOX INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT16541DGGR	DGG	48	SITE 41	330	24	8.6	15.8	1.8	12	24	Q1
SN74AHCT16541DGVR	DGV	48	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1
SN74AHCT16541DLR	DL	48	SITE 41	330	32	11.35	16.2	3.1	16	32	Q1

**TAPE AND REEL BOX DIMENSIONS**



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AHCT16541DGGR	DGG	48	SITE 41	346.0	346.0	41.0
SN74AHCT16541DGVR	DGV	48	SITE 41	346.0	346.0	41.0
SN74AHCT16541DLR	DL	48	SITE 41	346.0	346.0	49.0



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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