

# 74LVC16245A; 74LVCH16245A

16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Rev. 08 — 6 November 2008

Product data sheet

## 1. General description

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The 74LVC16245A; 74LVCH16245A are 16-bit transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features two output enable ( $\overline{\text{OE}}$ ) inputs for easy cascading and two send/receive ( $\text{nDIR}$ ) inputs for direction control.  $\overline{\text{OE}}$  controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH16245A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features

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- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when  $V_{\text{CC}} = 0 \text{ V}$
- All data inputs have bus hold. (74LVCH16245A only)
- Complies with JEDEC standard JESD8-B / JESD36
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Specified from  $-40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$  and  $-40 \text{ }^\circ\text{C}$  to  $+125 \text{ }^\circ\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74LVC16245ADL 74LVCH16245ADL	-40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVC16245ADGG 74LVCH16245ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVC16245AEV 74LVCH16245AEV	-40 °C to +125 °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm	SOT702-1
74LVC16245ABQ 74LVCH16245ABQ	-40 °C to +125 °C	HUQFN60U	plastic thermal enhanced ultra thin quad flat package; no leads; 60 terminals; UTLF based; body 4 × 6 × 0.55 mm	SOT1025-1

## 4. Functional diagram

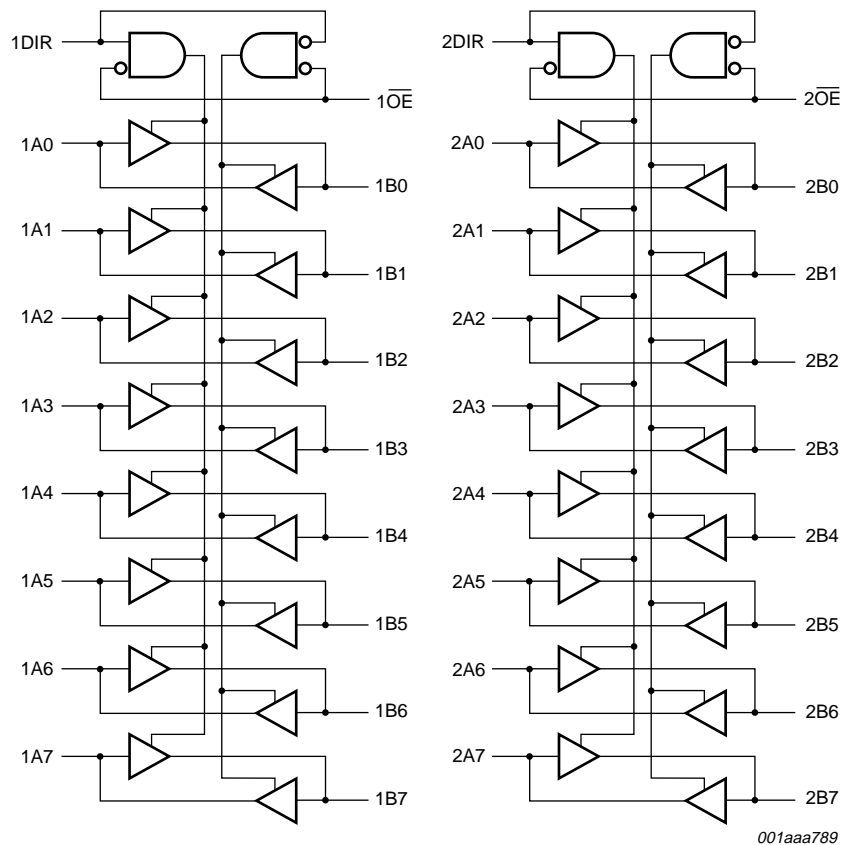


Fig 1. Logic symbol

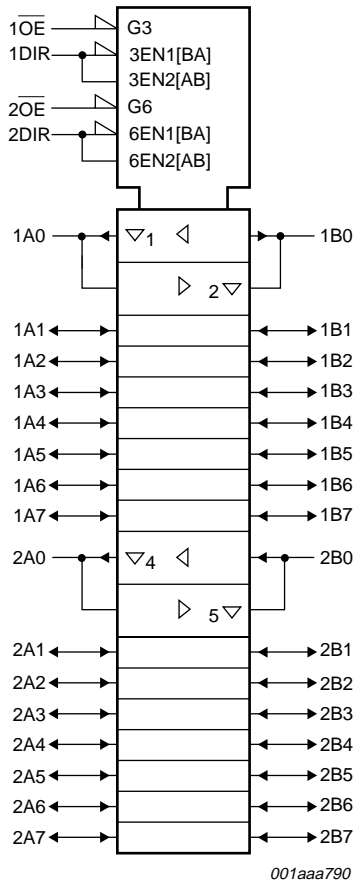


Fig 2. IEC logic symbol

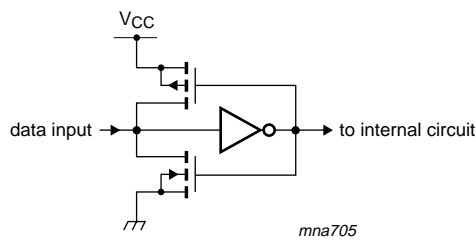
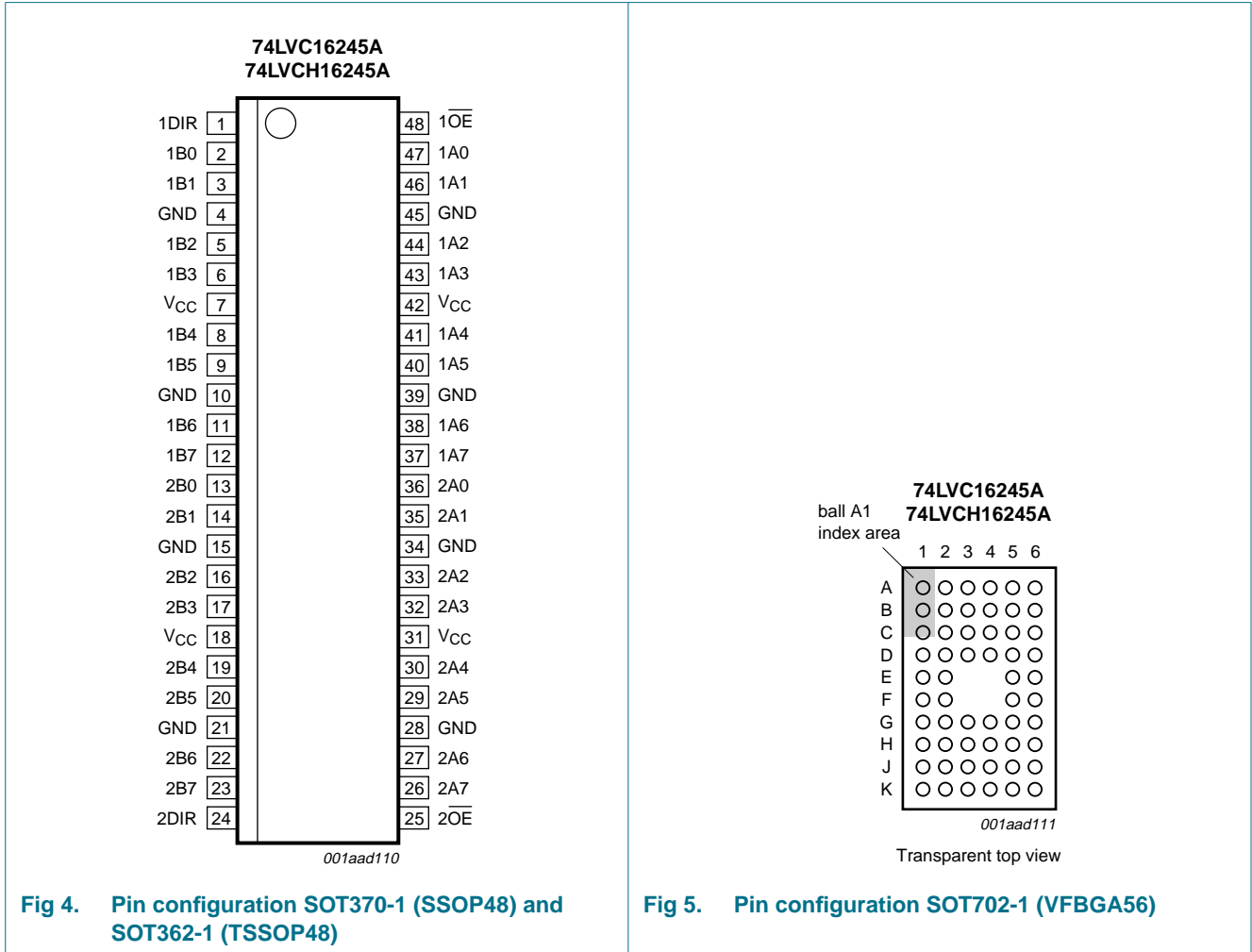
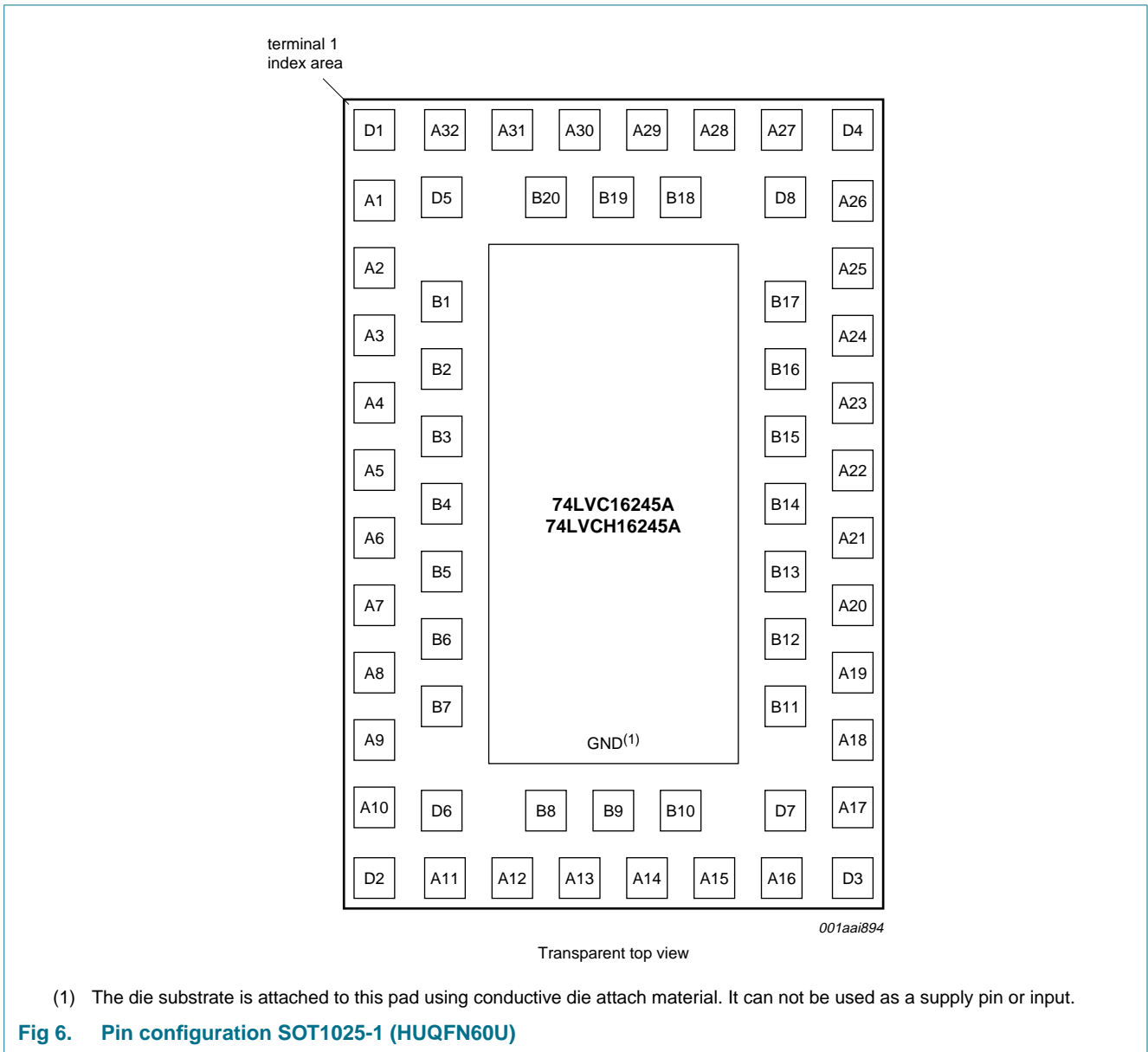


Fig 3. Bus hold circuit

## 5. Pinning information

### 5.1 Pinning





## 5.2 Pin description

Table 2. Pin description

Symbol	Pin			Description
	SOT370-1 and SOT362-1	SOT702-1	SOT1025-1	
1DIR, 2DIR	1, 24	A1, K1	A30, A13	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	B2, B1, C2, C1, D2, D1, E2, E1	B20, A31, D5, D1, A2, B2, B3, A5	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	F1, F2, G1, G2, H1, H2, J1, J2	A6, B5, B6, A9, D2, D6, A12, B8	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	B3, B4, D3, D4, G3, G4, J3, J4	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	C3, C4, H3, H4	A1, A10, A17, A26	supply voltage
1 $\overline{\text{OE}}$ , 2 $\overline{\text{OE}}$	48, 25	A6, K6	A29, A14	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	B5, B6, C5, C6, D5, D6, E5, E6	B18, A28, D8, D4, A25, B16, B15, A22	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	F6, F5, G6, G5, H6, H5, J6, J5	A21, B13, B12, A18, D3, D7, A15, B10	data input/output
n.c.	-	A2, A3, A4, A5, K2, K3, K4, K5	A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19	not connected

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs		Outputs	
n $\overline{\text{OE}}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage		[1] -0.5	+6.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW	[2] -0.5	V <sub>CC</sub> + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C;			
		(T)SSOP48 package	[3] -	500	mW
		VFBGA56 package	[4] -	1000	mW
		HUQFN60U package	[4] -	1000	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

[4] Above 70 °C the value of P<sub>tot</sub> derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage	maximum speed performance	2.7	-	3.6	V
		functional	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0	-	0	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	-	0	0.20	-	0.3	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.40	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V <sup>[2]</sup>	-	±0.1	±5	-	±20	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V <sup>[2][3]</sup>	-	±0.1	±5	-	±20	μA
I <sub>OFF</sub>	power-off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0.0 V	-	±0.1	±10	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.6 V	-	0.1	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.7 V to 3.6 V	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	10	-	-	-	pF
I <sub>BHL</sub>	bus hold current LOW	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V <sup>[4][5]</sup>	75	-	-	60	-	μA
I <sub>BHH</sub>	bus hold current HIGH	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V <sup>[4][5]</sup>	-75	-	-	-60	-	μA
I <sub>BHLO</sub>	bus hold overdrive current LOW	V <sub>CC</sub> = 3.6 V <sup>[4][6]</sup>	500	-	-	500	-	μA



**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
I <sub>BHHO</sub>	bus hold overdrive current HIGH	V <sub>CC</sub> = 3.6 V <sup>[4][6]</sup>	-500	-	-	-500	-	μA

- [1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.
- [2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.
- [3] For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.
- [4] Valid for data inputs of bus hold parts only (74LVCH16245A). Note that control inputs do not have a bus hold circuit.
- [5] The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
- [6] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nBn; nBn to nAn; see <a href="#">Figure 7</a> <sup>[1]</sup>	-	13.0	-	-	-	ns
		V <sub>CC</sub> = 1.2 V	-	13.0	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.7	4.7	1.0	6.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	1.0	2.2	4.5	1.0	6.0	ns
t <sub>en</sub>	enable time	n $\overline{O}E$ to nAn, nBn; see <a href="#">Figure 8</a> <sup>[1]</sup>	-	15.0	-	-	-	ns
		V <sub>CC</sub> = 1.2 V	-	15.0	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.6	6.7	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	1.0	2.8	5.5	1.0	7.0	ns
t <sub>dis</sub>	disable time	n $\overline{O}E$ to nAn, nBn; see <a href="#">Figure 8</a> <sup>[1]</sup>	-	11.0	-	-	-	ns
		V <sub>CC</sub> = 1.2 V	-	11.0	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	6.6	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	1.5	3.2	5.6	1.5	7.0	ns

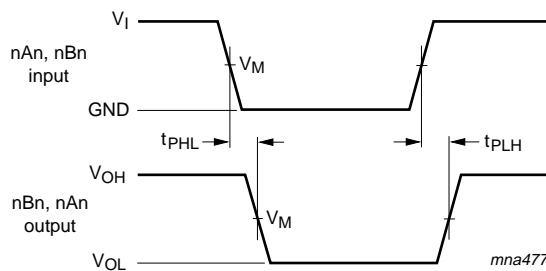
**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	per buffer; $V_I = \text{GND to } V_{CC}$ $V_{CC} = 3.3 \text{ V}$	-	30	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  
 $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [2] Typical values are measured at  $T_{amb} = 25 \text{ °C}$  and  $V_{CC} = 3.3 \text{ V}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in Volts  
 $N$  = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

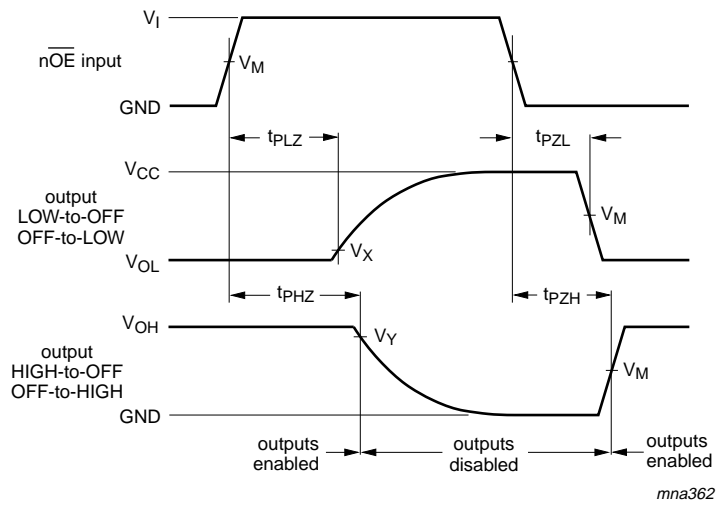
## 11. Waveforms



Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. The input (nAn, nBn) to output (nBn, nAn) propagation delays**



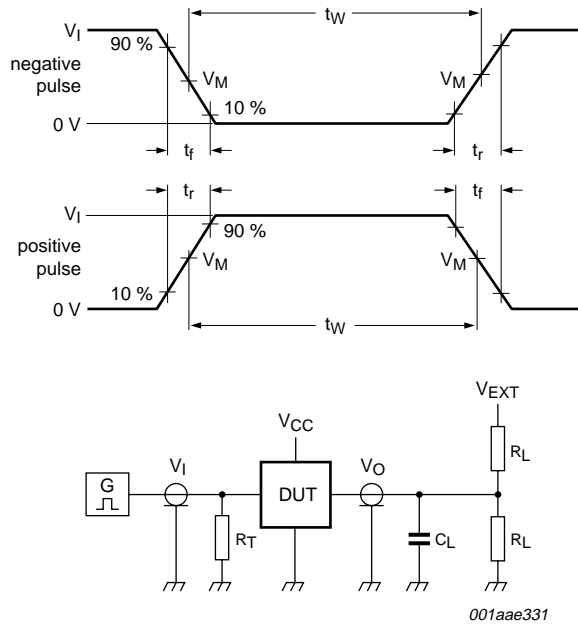
Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 8. 3-state enable and disable times.**

**Table 8. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \text{ V}$	$V_{OH} - 0.1 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 9. Load circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

[1] The circuit performs better when  $R_L = 1$  k $\Omega$ ,

## 12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

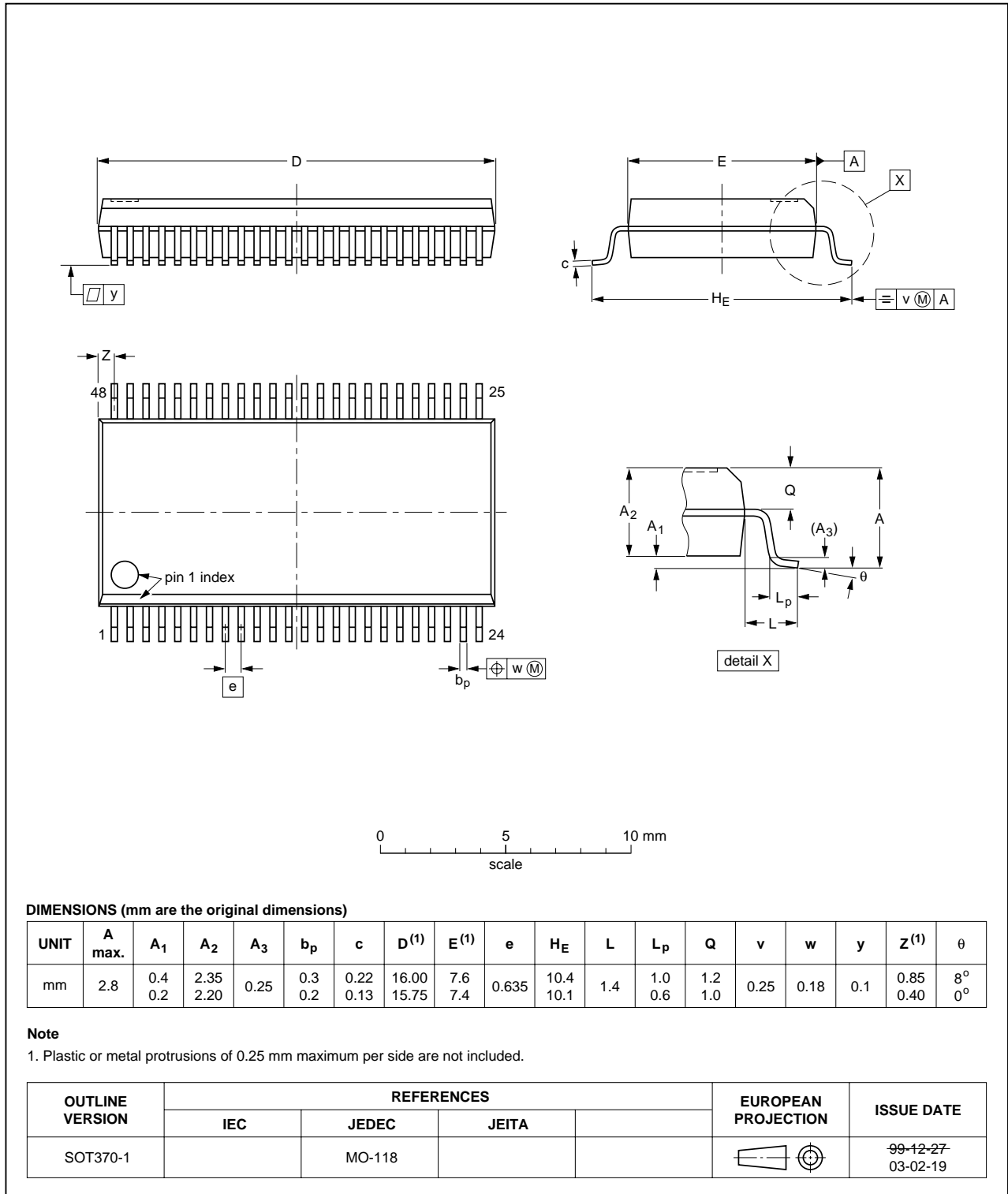


Fig 10. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

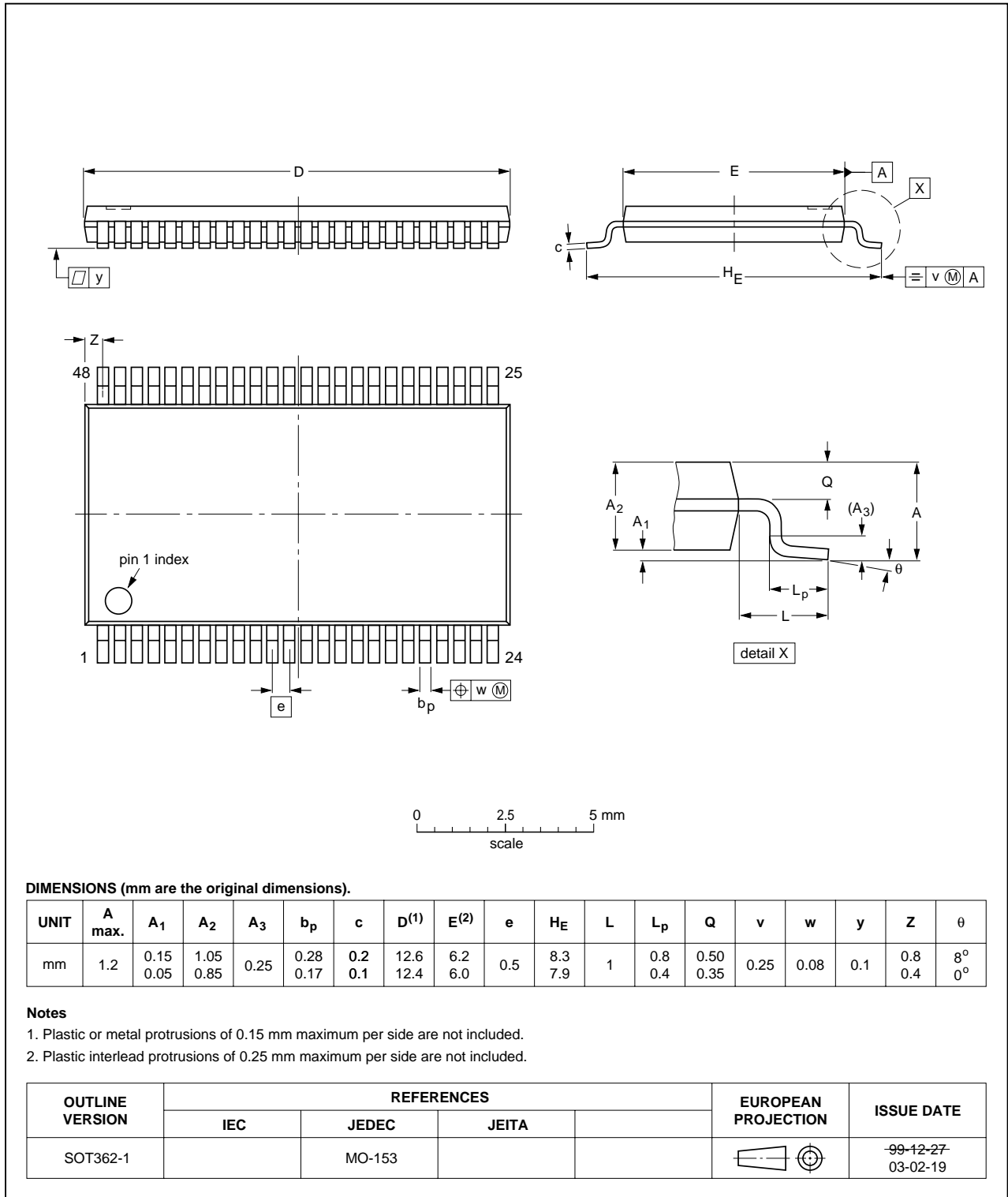


Fig 11. Package outline SOT362-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1

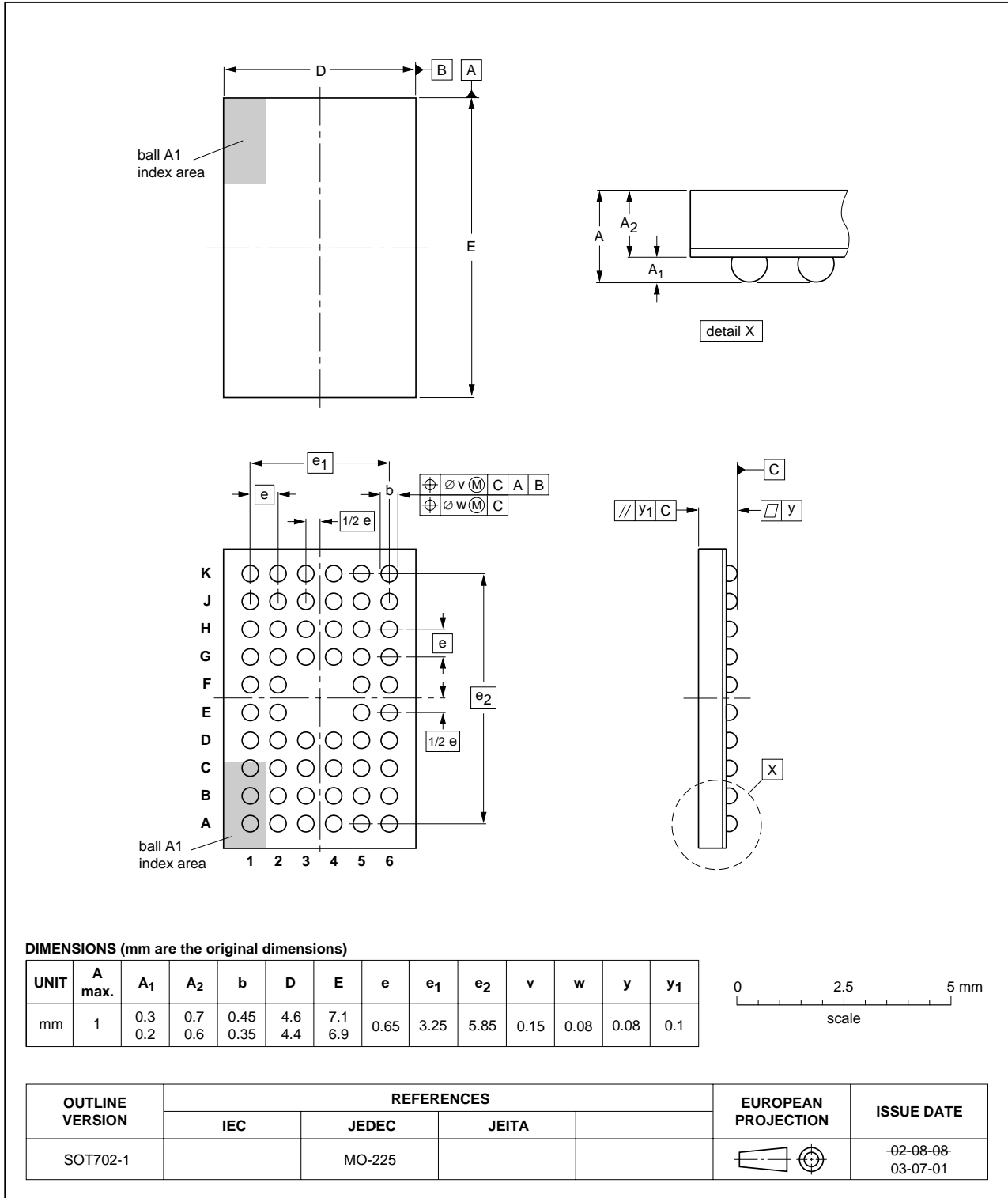


Fig 12. Package outline SOT702-1 (VFBGA56)

**HUQFN60U: plastic thermal enhanced ultra thin quad flat package; no leads**  
**60 terminals; UTLP based; body 4 x 6 x 0.55 mm**

SOT1025-1

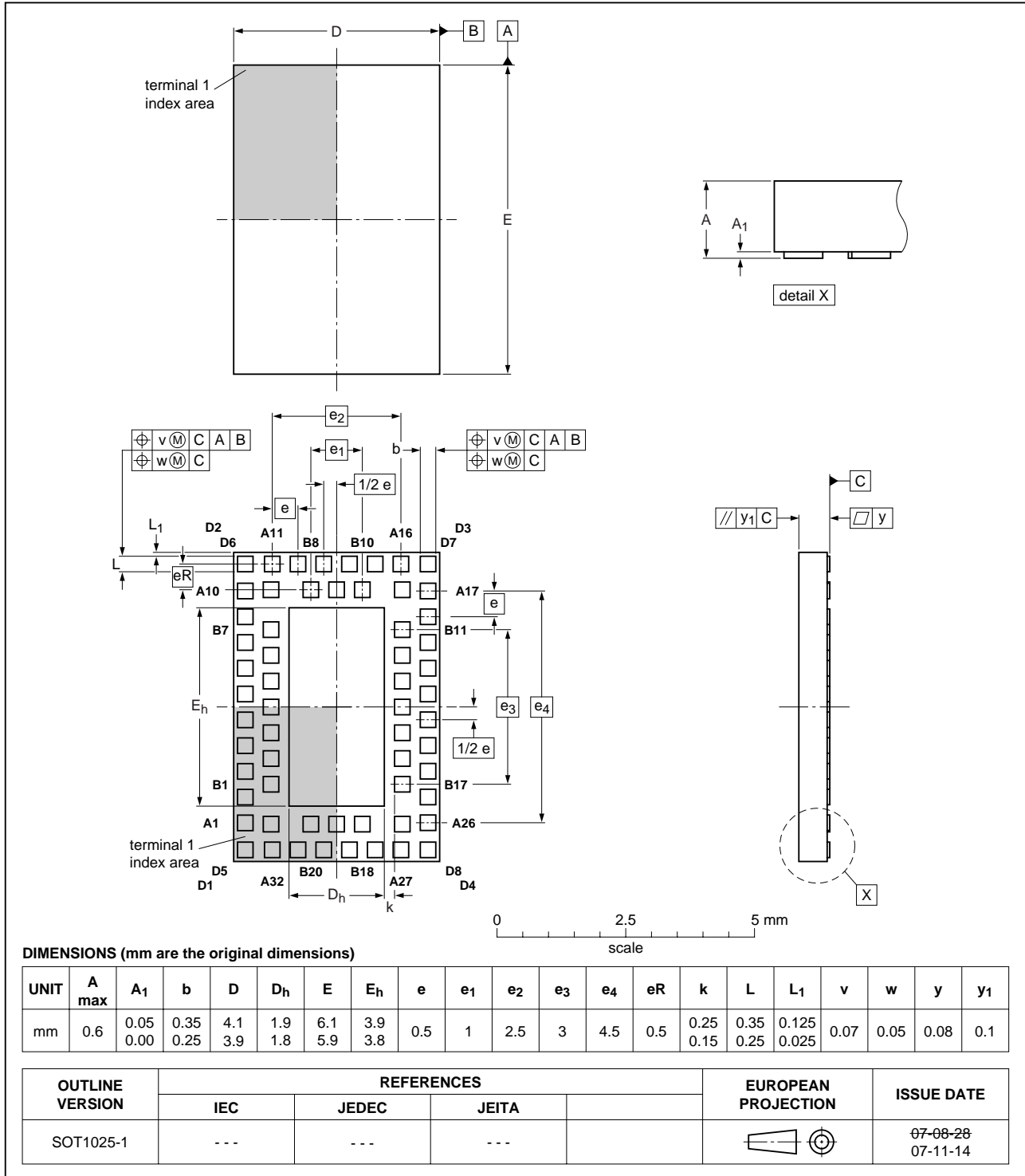


Fig 13. Package outline SOT1025-1 (HUQFN60U)



## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16245A_8	20081106	Preliminary data sheet	-	74LVC_LVCH16245A_7
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Added type number 74LVC16245ABQ and 74LVCH16245ABQ (HUQFN60U package)</li> </ul>		
74LVC_LVCH16245A_7	20031125	Product specification	-	74LVC_LVCH16245A_6
74LVC_LVCH16245A_6	20030130	Product specification	-	74LVC_LVCH16245A_5
74LVC_LVCH16245A_5	20021030	Product specification	-	74LVC_H16245A_4
74LVC_H16245A_4	19970925	Product specification	-	74LVC16245A_3 74LVCH16245A_3
74LVC16245A_3 74LVCH16245A_3	19970925	Product specification	-	74LVC16245A_2
74LVC16245A_2	19970801	Product specification	-	74LVC16245A_1
74LVC16245A_1	-	-	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

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