SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

MAY 1983 - REVISED MARCH 1988

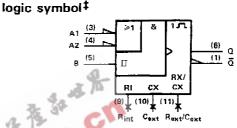
- Programmable Output Pulse Width With R_{int}...35 ns Typ With R_{ext}/C_{ext}...40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

SN54121 J OR W PACKAGE SN74121 N PACKAGE (TOP VIEW)							
Q 1 NC 2 A1 3 A2 4 B 5 Q 6 GND 7	14 VCC 13 NC 12 NC 11 Rext/Cext 10 Cext 9 Rint 8 NC						

NC - No internal connection.

OUTPUTS INPUTS ō O A1 A2 R н L х Н Lt нt Х L H х х н1 1 Н Н Н į. н ı X

FUNCTION TABLE



*This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

For explanation of function table symbols, see page

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to VCC noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

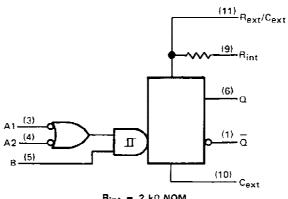
Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and VCC ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54121 and 2 k Ω to 40 k Ω for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{W(out)} = C_{ext}R_{T}\ln 2 \approx 0.7~C_{ext}R_{T}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25 °C. Duty cycles as high as 90% are achieved when using maximum recommended R_T'. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.



f These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

logic diagram (positive logic)



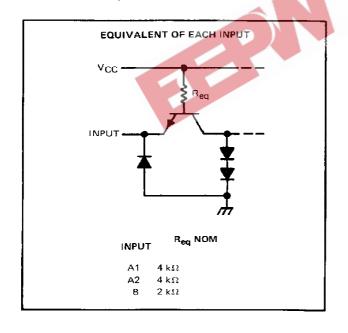
Rint = 2 k0 NOM

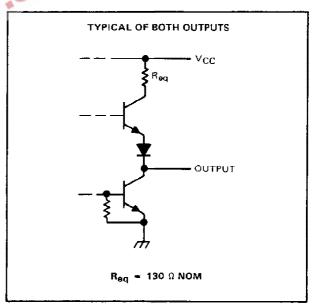
Pin numbers shown on logic notation are for J or N packages.

NOTES: 1. An external capacitor may be connected between $C_{\rm ext}$ (positive) and $R_{\rm ext}/C_{\rm ext}$.

2. To use the internal timing resistor, connect $R_{\rm int}$ to $V_{\rm CC}$. For improved pulse width accuracy and repeatability, connect an external resistor between $R_{\rm ext}/C_{\rm ext}$ and $V_{\rm CC}$ with $R_{\rm int}$ open-circuited.

schematics of inputs and outputs





SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

absolute maximum ratings over operating free-air temperature range (unless other	rwise noted)
Supply voltage, VCC (see Note 3)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54121	-55°C to 125°C
SN74121	0°C to 70°C
Storage temperature range	
NOTE 3: Voltage values are with respect to network ground terminal.	

recommended operating conditions

				MIN	NOM	MAX	UNIT
Vcc	Supply voltage	-	54 Family	4.5	5	5.5	v
·	Copply voltage		74 Family	4.75	5	5.25	, v
ЮН	High-level output current					-0.4	mΑ
l _{OL}	Low-level output current					16	mΑ
dv/dt	Rate of rise or fall of input pulse	Schmitt input, B		1			V/s
	Logic inputs, A1, A2		1			V/μs	
^t w(in)	Input pulse width		1 15 11	50			ns
я	R _{ext} External timing capacitance	1	54 Family	1.4	-	30	
''ext		Gr.	74 Family	1.4		40	kΩ
C _{ext}	External timing capacitance	26.13	-40°	0		1000	μF
	Duty cycle	$R_T = 2 k\Omega$				67	
Daty Cycle		$R_T = MAX R_{ext}$				90	%
T _A	Operating free-air temperature		54 Family	- 55		125	
'A	operating free-air temperature		74 Family	0		70	۵C

SN54121, SN74121 MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CO	MIN	TYP‡	MAX	UNIT	
VIH	High-level input voltage at B input	V _{CC} = MIN		2			V
VIL	Low-level input voltage at A input	VCC = MIN				0.8	٧
VŢ+	Positive-going threshold voltage at B input	VCC = MIN	*****		1.55	2	٧
VΤ_	Negative-going threshold voltage at B input	VCC = MIN		0.8	1.35		٧
Vik	Input clamp voltage	V _{CC} = MIN,	l _f = −12 mA			- 1.5	٧
ЮН	High-level output voltage	V _{CC} - MIN,	IOH = MAX	2.4	3.4		٧
VOL	Low-level output voltage	VCC = MIN,	IOL = MAX		0.2	0.4	V
Ιį	Input current at maximum input voltage	V _{CC} = MAX.	V _I = 5.5 V			1	mA
		V _{CC} = MAX,	A1 or A2			40	
ΉН	High-level input current	$V_1 = 2.4 \text{ V}$	В			80	μА
		VCC = MAX,	A1 or A2			- 1.6	mΑ
IIL	Low-level input current	V _I = 0.4 V	В			- 3.2	mA
	Short-circuit output current§	V MAAY	54 Family	- 20		- 55	4
OS Short-circ	Short-circuit output currents	VCC = MAX	74 Family	- 18		- 55	mA
ICC Sup	Supply current	U. MAY	Quiescent		13	25	^
		V _{CC} = MAX	Triggered		23	40	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. ‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C. † Not more than one output should be shorted at a time.

switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PLH	Propagation dalay time, low-to-high- level Q output from either A input			45	70	ns
tpLH	Propagation delay time, low-to-high- level Q output from B input	C _{ext} = 80 pF,		35	55	ns
^t PHL	Propagation delay time, high-to-low level Q output from either A input	R_{int} to V_{CC}		50	80	п\$
^t PHL	Propagation delay time, high-to-low level $\overline{\mathbf{Q}}$ output from B input	R _L = 400 Ω, See Note 4	-	40	65	ns
tw(out)	Pulse width obtained using internal timing resistor	$C_{ext} = 80 \rho F,$ $R_{int} \text{ to V}_{CC}$	70	110	150	ns
tw(out)	Pulse width obtained with zero timing capacitance	C _{ext} = 0. R _{int} to V _{CC}		30	50	ns
	Pulse width obtained using	$C_{\text{ext}} = 100 \text{ pF},$ $R_{\text{T}} = 10 \text{ k}\Omega$	600	700	800	ns
^t w(out)	external timing resistor	$C_{\text{ext}} = 1 \mu\text{F},$ $R_{\text{T}} = 10 \text{k}\Omega$	6	7	8	ms

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL CHARACTERISTICS[†]

DISTRIBUTION OF UNITS for OUTPUT PULSE WIDTH VCC = 5 V TA = 25°C Cext = 101 pF RT = 10 kΩ (External) Wedian +0.7 Cext RT

tw(out)-Output Pulse Width-ns

697

691

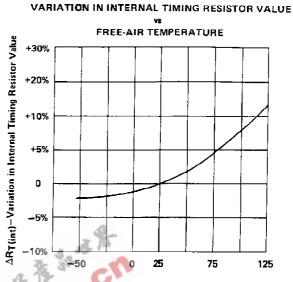
694

99% of Units

700

703

706



TA-Free-Air Temperature-°C

FIGURE 1

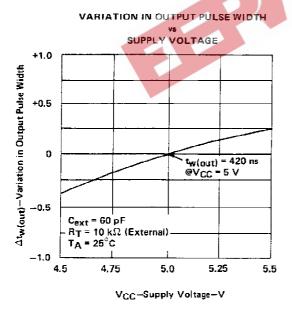


FIGURE 2

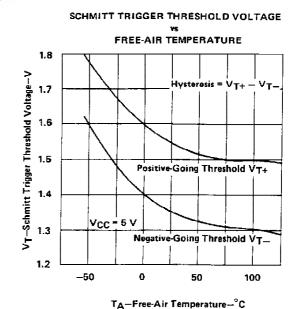


FIGURE 3

FIGURE 4

[†]Data for temperatures below 0°C and above 70°C are applicable for SN54121.



TYPICAL CHARACTERISTICS[†] (continued)

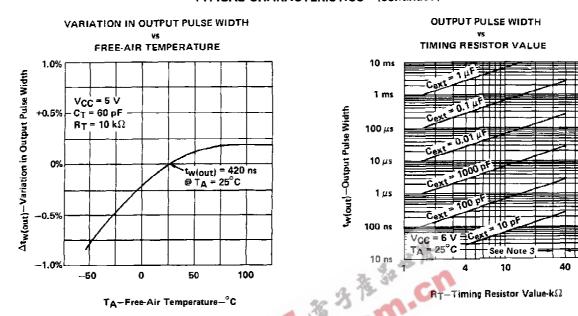


FIGURE 5 FIGURE 6

100

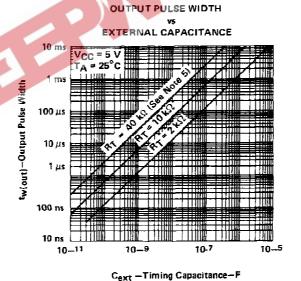


FIGURE 7

NOTE 5: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54121. †Data for temperatures below 0 °C and above 70 °C are applicable for SN54121.

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9755301QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9755301QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN74121D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74121DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74121DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74121DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74121N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74121NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74121NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74121NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54121J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54121WA	ACTIVE	CFP	WA	14	1	TBD	Call TI	Level-NC-NC-NC

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ACTIVE: Product device recommended for new designs.

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

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TBD: The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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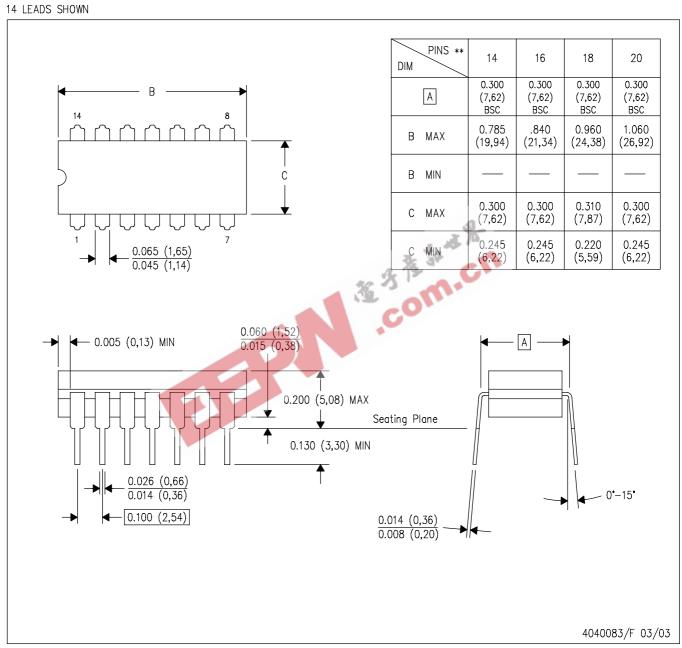




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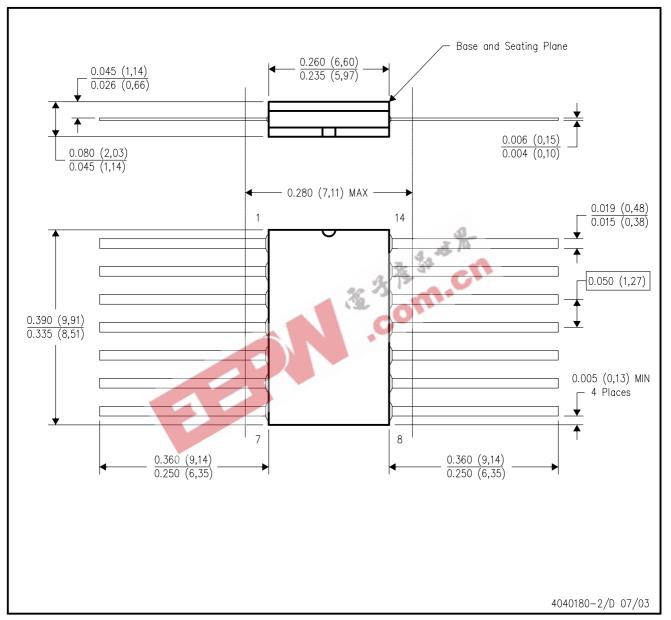




- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

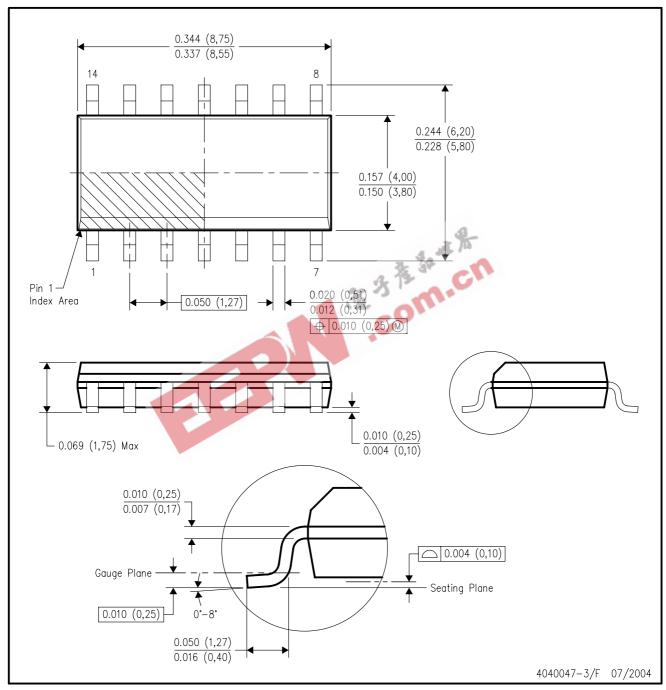


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AB.

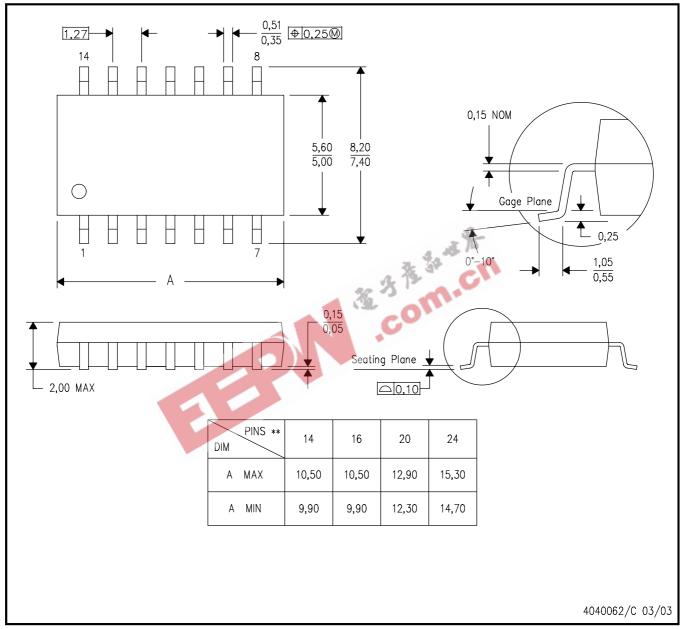


MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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