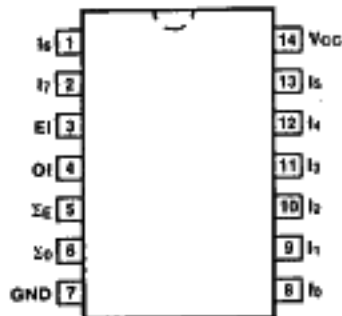


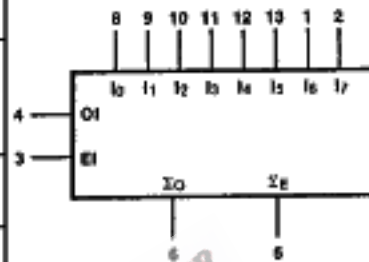
54/74180

8-BIT PARITY GENERATOR/CHECKER

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



DESCRIPTION—The '180 is a monolithic, 8-bit parity checker/generator which features control inputs and even/odd outputs to enhance operation in either odd or even parity applications. Cascading these circuits allows unlimited word length expansion. Typical application would be to generate and check parity on data being transmitted from one register to another. Typical power dissipation is 170 mW.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V, ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74180PC		9A
Ceramic DIP (D)	A	74180DC	54180DM	6A
Flatpak (F)	A	74180FC	54180FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
I ₀ - I ₇	Data Inputs	1.0/1.0
OI	Odd Input	2.0/2.0
EI	Even Input	2.0/2.0
Σ _O	Odd Parity Output	20/10
Σ _E	Even Parity Output	20/10

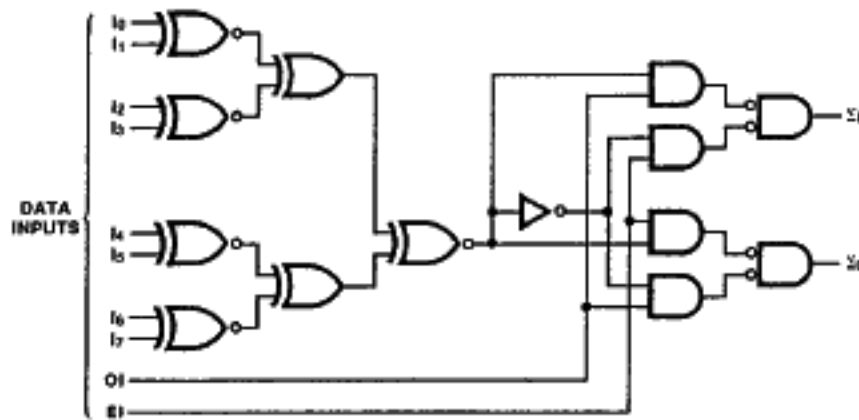
TRUTH TABLE

Σ OF 1's AT 0 THRU 7	INPUTS		OUTPUTS	
	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

4

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS	
		Min	Max			
I _{os}	Output Short Circuit Current	XM	-20	-55	mA	V _{CC} = Max
		XC	-18	-55		
I _{cc}	Power Supply Current	XM	49		mA	V _{CC} = Max, I _n = Open OI, EI = 4.5 V
		XC	56			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω			
		Min	Max		
I _{PLH} I _{PHL}	Propagation Delay I _n to ΣE		60 68	ns	Figs. 3-1, 3-5 OI = Gnd
I _{PLH} I _{PHL}	Propagation Delay I _n to ΣO		48 38	ns	Figs. 3-1, 3-4 OI = Gnd
I _{PLH} I _{PHL}	Propagation Delay I _n to ΣE		48 38	ns	Figs. 3-1, 3-5 EI = Gnd
I _{PLH} I _{PHL}	Propagation Delay I _n to ΣO		60 68	ns	Figs. 3-1, 3-4 EI = Gnd
I _{PLH} I _{PHL}	Propagation Delay EI or OI to ΣE		20 10	ns	Figs. 3-1, 3-5
I _{PLH} I _{PHL}	Propagation Delay EI or OI to ΣO		20 10	ns	Figs. 3-1, 3-4