SDLS078

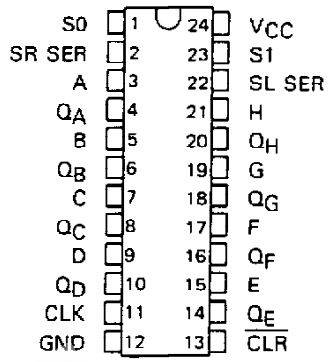
DECEMBER 1972—REVISED MARCH 1988

description

These 8-bit shift registers are compatible with most other TTL and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 devices are characterized for operation from 0°C to 70°C.

SN54198 . . . J OR W PACKAGE
SN74198 . . . N PACKAGE
(TOP VIEW)



SN54198 and SN74198

These bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contain 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit Clock (Do nothing)
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Parallel (Broadside) Load

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

'198
FUNCTION TABLE

INPUTS							OUTPUTS
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL	Q_A Q_B . . . Q_G Q_H
	S_1	S_0		LEFT	RIGHT	A . . . H	
L	X	X	X	X	X	X	L L L L
H	X	X	L	X	X	X	Q_{A0} Q_{B0} Q_{G0} Q_{H0}
H	H	H	↑	X	X	a . . . h	a b g h
H	L	H	↑	X	H	X	H Q_{An} Q_{Fn} Q_{Gn}
H	L	H	↑	X	L	X	L Q_{An} Q_{Fn} Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn} Q_{Cn} Q_{Hn} H
H	H	L	↑	L	X	X	Q_{Bn} Q_{Cn} Q_{Hn} L
H	L	L	X	X	X	X	Q_{A0} Q_{B0} Q_{G0} Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = the level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

SN54198, SN54199 SN74198, SN74199
8-BIT SHIFT REGISTERS

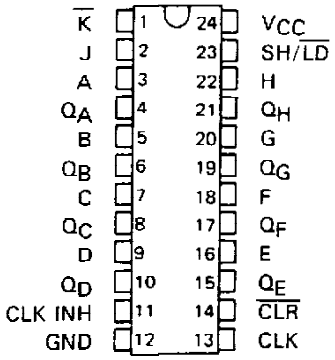
SN54199 and SN74199

These registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Inhibit Clock (Do nothing)
Shift (In the direction Q_A toward Q_H)
Parallel (Broadside) Load

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

SN54199 . . . J OR W PACKAGE
SN74199 . . . N PACKAGE
(TOP VIEW)



Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the function table for levels required to enter serial data into the first flip-flop.

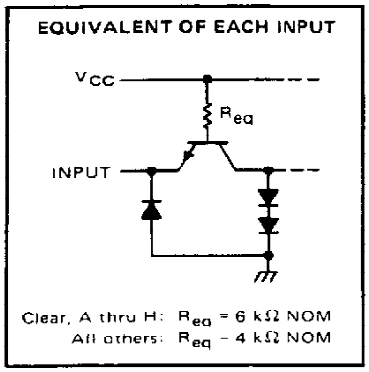
Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

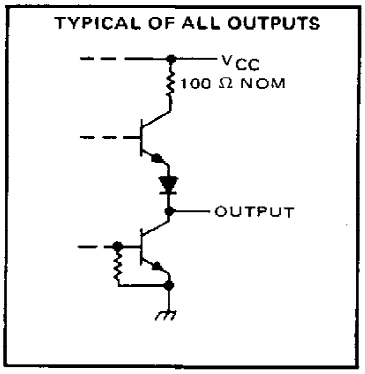
These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

'199
FUNCTION TABLE

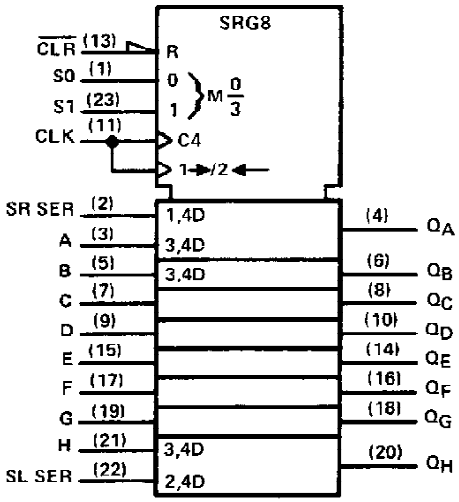
INPUTS							OUTPUTS			
CLEAR	SHIFT/$\overline{\text{LOAD}}$	CLOCK INHIBIT	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL A . . . H	Q_A	Q_B	Q_C . . .	Q_H
L	X	X	X	X	X	X	L	L	L	L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}
H	L	L	↑	X	X	a . . . h	a	b	c	h
H	H	L	↑	L	H	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}	Q_{H0}

schematics of inputs and outputs



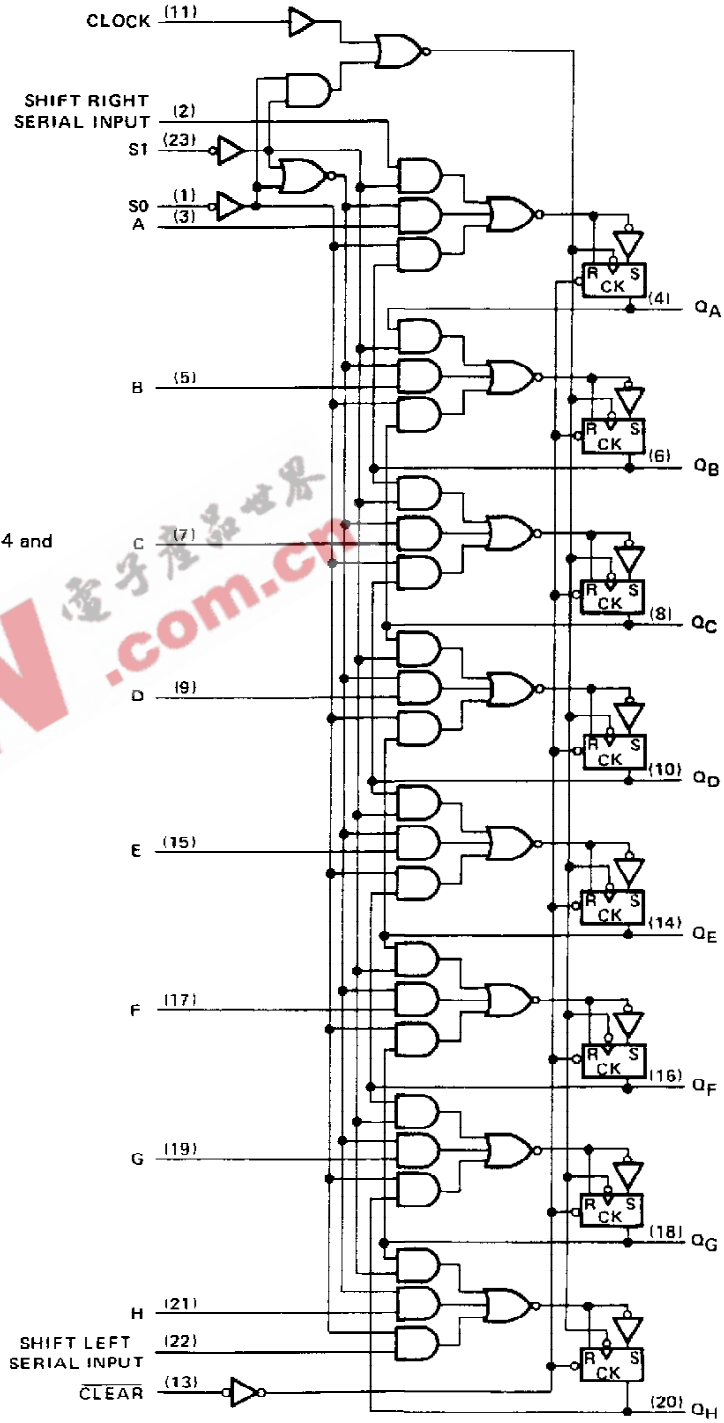


logic symbol†

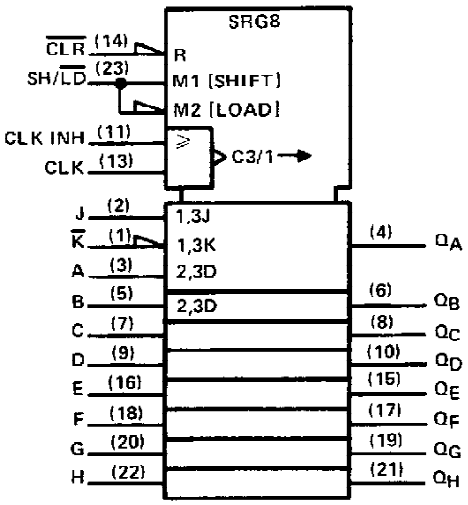


† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



logic symbol†



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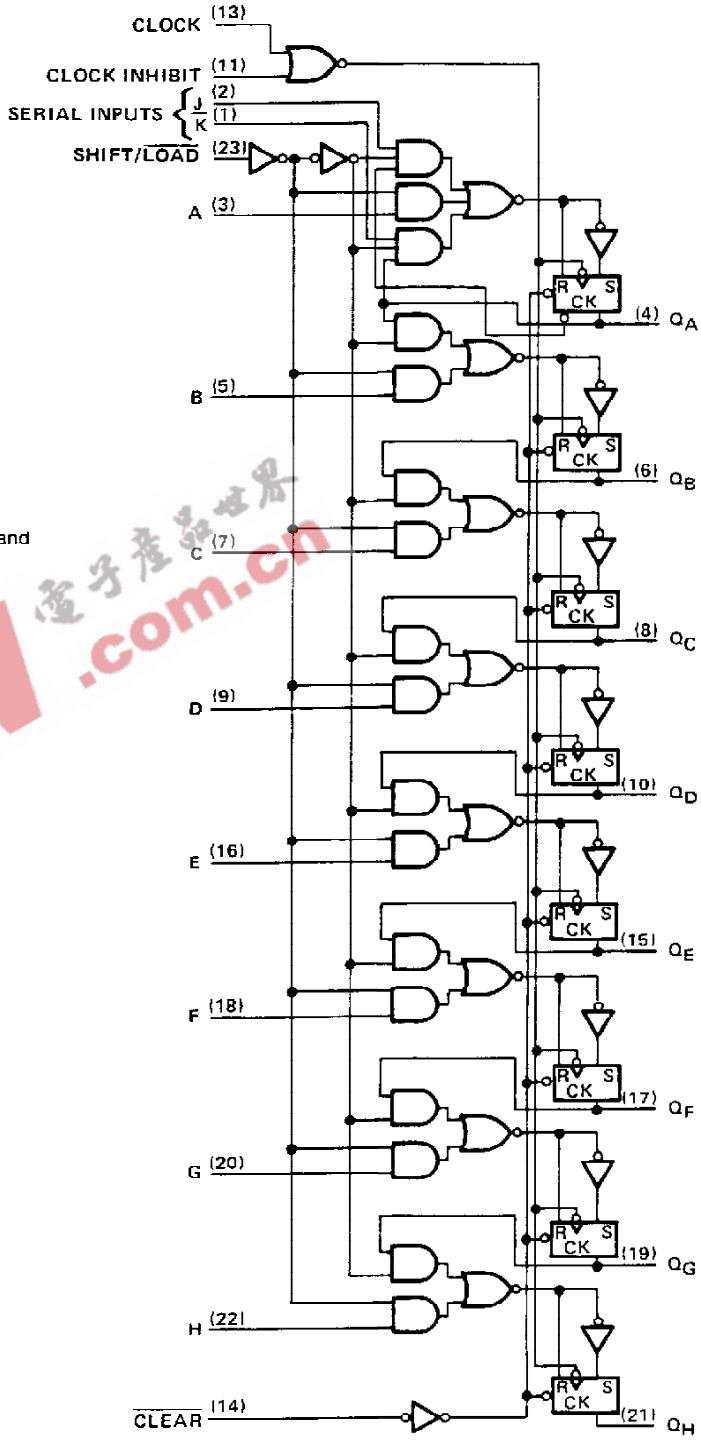
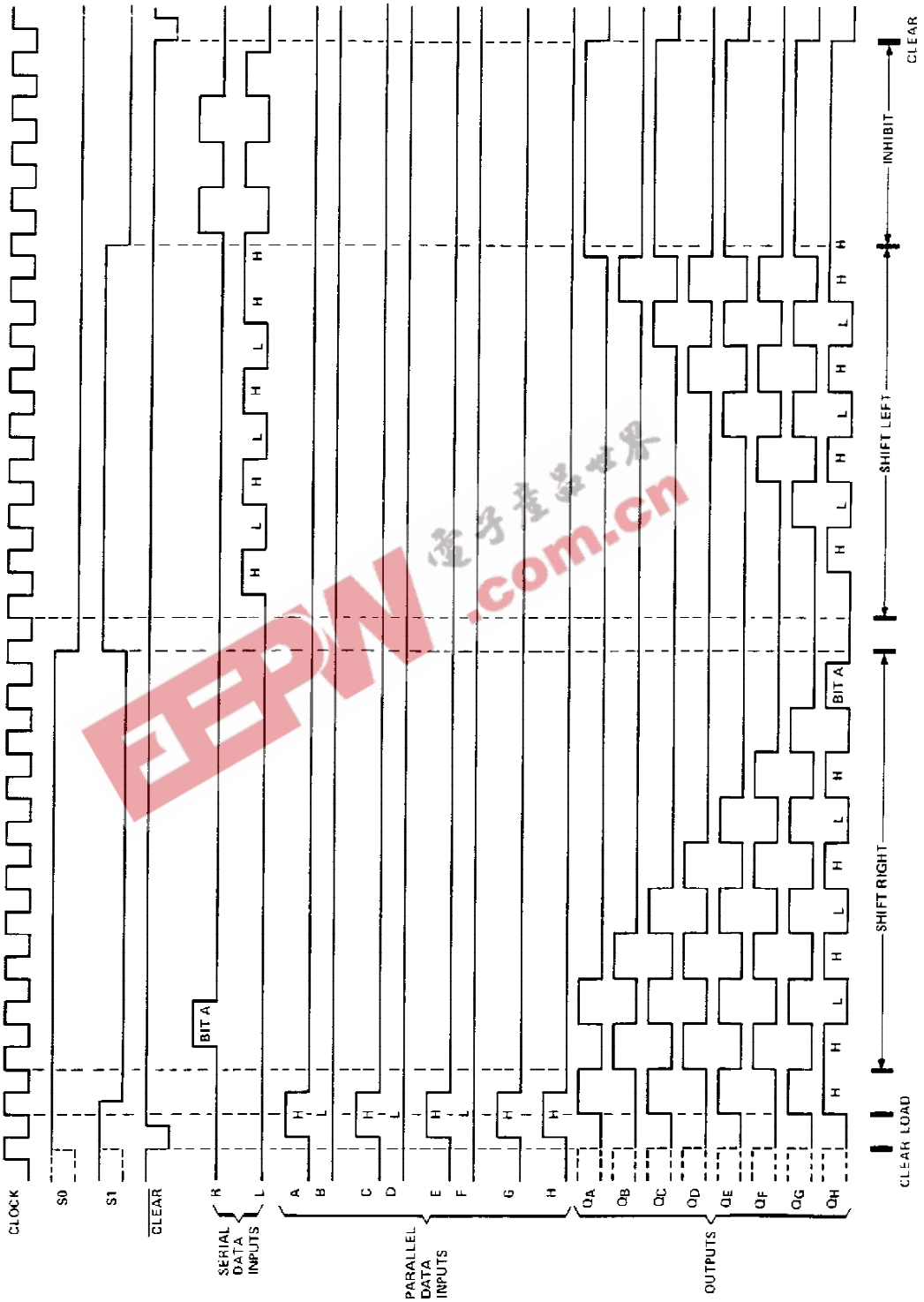
logic diagram (positive logic)



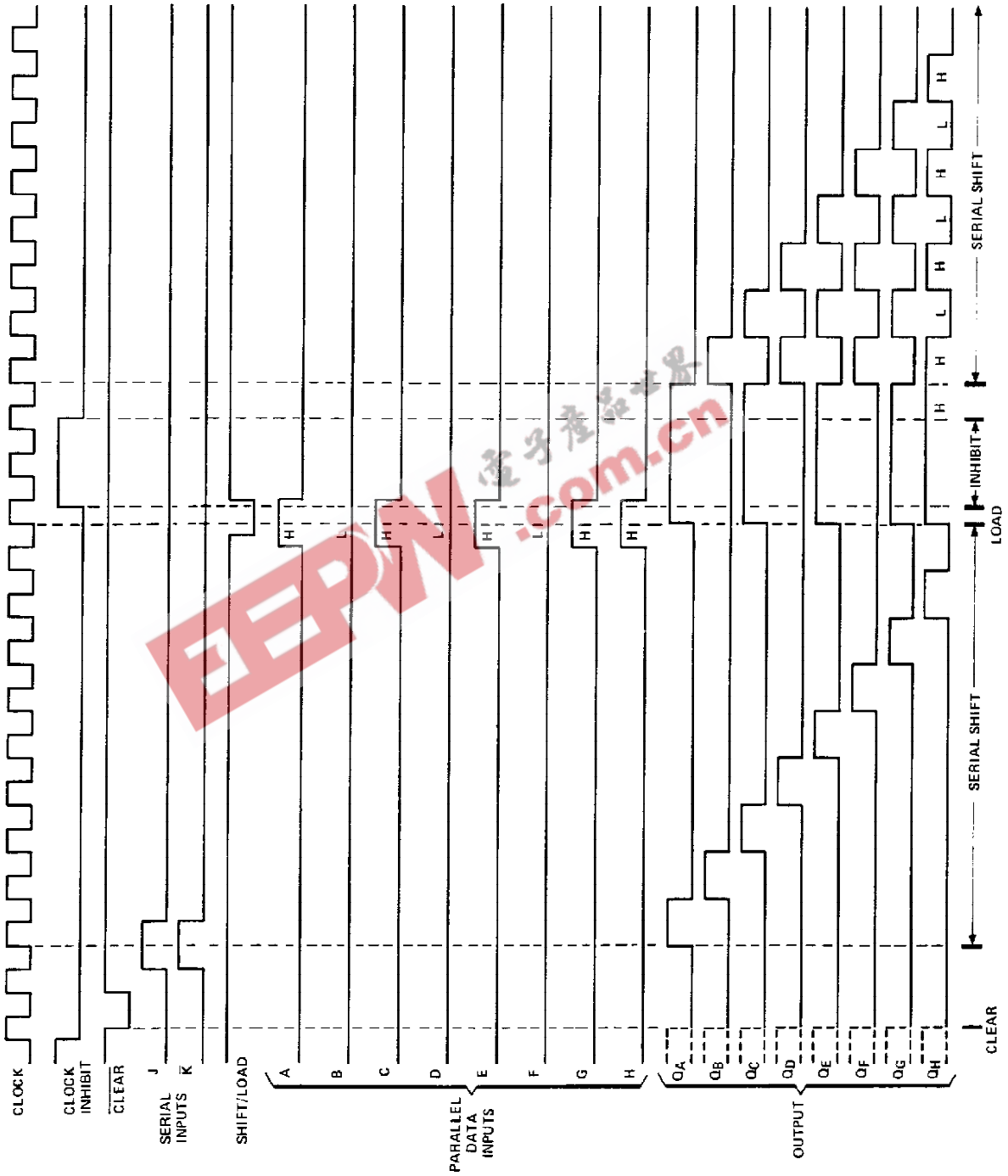
SN54198, SN74198

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



SN54199, SN74199

typical clear, shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54198 SN54199			SN74198 SN74199			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)	20			20			ns
Mode-control setup time, t_{su}	30			30			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Hold time at any input, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54198 SN54199			SN74198 SN74199			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Table Below		90	127		90	127	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC}
(ALL OUTPUTS ARE OPEN)

TYPE	APPLY 4.5 V	FIRST GROUND, THEN APPLY 4.5 V	GROUND
SN54198, SN74198	Serial Input, S_0, S_1	Clock	$\overline{\text{Clear}}$, Inputs A thru H
SN54199, SN74199	J, K, Inputs A thru H	Clock	Clock inhibit, Clear, Shift/Load

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	26	ns

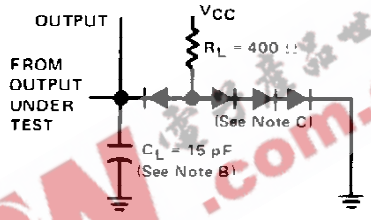
PARAMETER MEASUREMENT INFORMATION

SN54198, SN74198
TEST TABLE FOR SYNCHRONOUS INPUTS

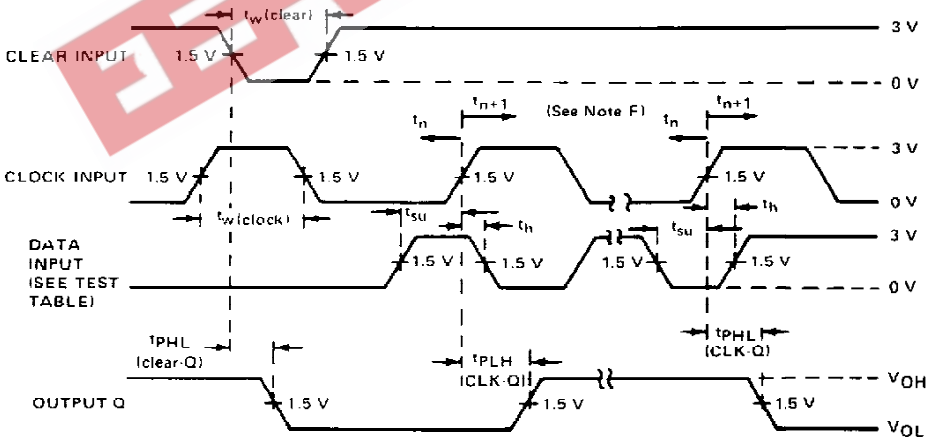
DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
E	4.5 V	4.5 V	Q_E at t_{n+1}
F	4.5 V	4.5 V	Q_F at t_{n+1}
G	4.5 V	4.5 V	Q_G at t_{n+1}
H	4.5 V	4.5 V	Q_H at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+8}
R Serial Input	0 V	4.5 V	Q_H at t_{n+8}

SN54199, SN74199
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/$\overline{\text{LOAD}}$	OUTPUT TESTED (SEE NOTE E)
A	0 V	Q_A at t_{n+1}
B	0 V	Q_B at t_{n+1}
C	0 V	Q_C at t_{n+1}
D	0 V	Q_D at t_{n+1}
E	0 V	Q_E at t_{n+1}
F	0 V	Q_F at t_{n+1}
G	0 V	Q_G at t_{n+1}
H	0 V	Q_H at t_{n+1}
J and $\overline{\text{K}}$	4.5 V	Q_H at t_{n+8}



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)}$ = 20 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)}$ = 20 ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

F. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

FIGURE 1

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