National Semiconductor

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ADC0881
8-Bit 20 MSPS Flash A/D Converter

General Description

The ADC0881 is a monolithic flash Analog-to-Digital converter capable of converting a video signal into a stream of 8-bit digital words at 20 MegaSamples Per Second (MSPS). Since the ADC0881 is a flash converter, a sample-and-hold circuit is not required.

The ADC0881 consists of 255 clocked latching comparators, precision resistive divider, encoding logic, and an output register. A single convert clock controls the conversion operation. The unit can be configured to give either true or inverted outputs, in binary or offset two's complement coding. All digital I/O is TTL compatible.

Key Specifications

■ Resolution	8 bits
■ Conversion rate	DC to 20 MSPS (min)
■ Full power bandwidth	7 MHz (min)
■ Small signal bandwidth (−3 dB)	60 MHz (min)
■ Linearity error	½ LSB (max)
■ Analog input range	+3 to +5V
■ Differential gain	1%
■ Differential phase	0.5°
■ Power dissipation (V_{CC} = +5V)	600 mW
■ Power supply	+5V

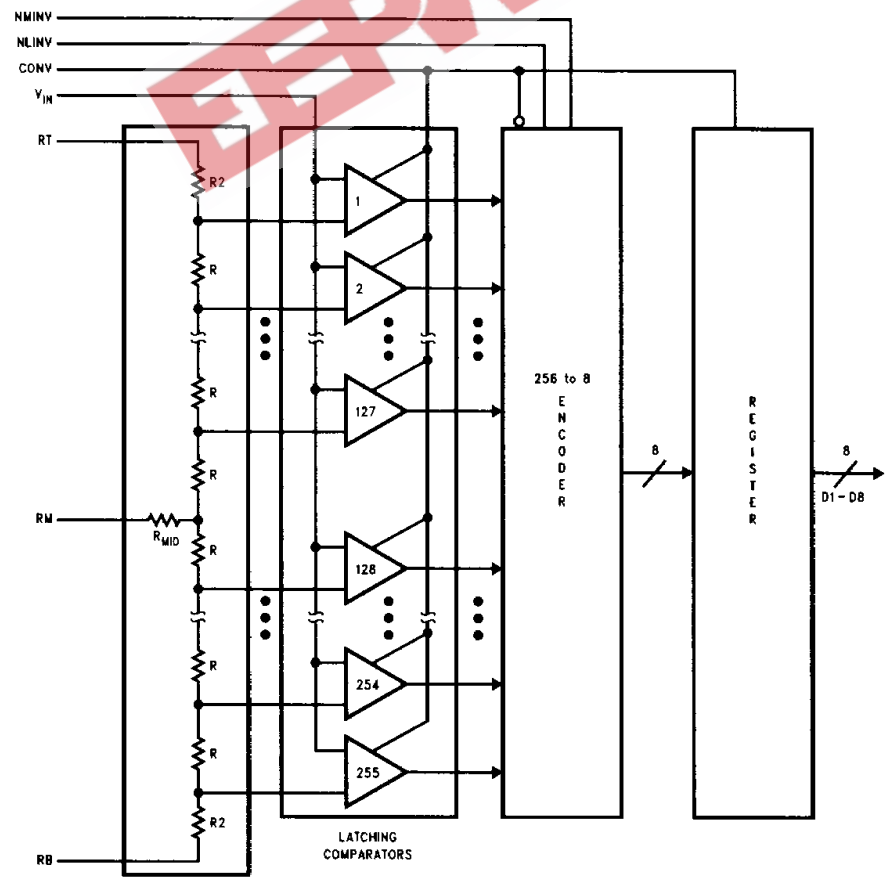
Applications

- Video digitizing
- Medical imaging
- High energy physics
- Digital television
- Radar
- High speed data links

Features

- Drop-in replacement for TDC1058
- Pin for pin replacement for CXA1096P and ADC-304
- No sample-and-hold circuit required
- Selectable data format
- Available in plastic DIP, CERDIP and PLCC
- Single supply operation

Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA}, V_{CCD})	−0.5V to +7.0V
$V_{CCA}-V_{CCD}$	±0.5V
AGND−DGND	±0.5V
Voltage at Logic Control Inputs (CONV, NMINV, NLINV) (Note 3)	−0.5V to (V_{CC} +0.5V)
Voltage at Digital Outputs (D1−D8) (Note 3)	−0.5V to (V_{CC} +0.5V)
Voltage at Analog Inputs (V_{IN}, V_{RT}, V_{RB}) (Note 3)	−0.5V to (V_{CC} +0.5V)
$V_{RT}-V_{RB}$	±2.2V
Applied Current at Digital Outputs (Note 4)	±50 mA
Input Current at Logic Control Inputs (Note 4)	±50 mA
Input Current for V_{IN}, V_{RT}, V_{RB} (Note 4)	±100 mA
Power Dissipation at T_A = 25°C	(Note 5)
ESD Rating	500V
Storage Temperature Range	−65°C to +150°C
Soldering Temperature All Packages (10 seconds)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0881CCJ/TDC1058B6C	0°C ≤ T_A ≤ +70°C
ADC0881CCN/TDC1058N6C	0°C ≤ T_A ≤ +70°C
ADC0881CCV/TDC1058R3C	0°C ≤ T_A ≤ +70°C
Supply Voltages (V_{CCA} = V_{CCD} = V_{CC})	4.75V to 5.25V
AGND−DGND Voltage	±0.1V
V_{RT} Most Positive Reference Voltage (Note 6)	5.0V to (V_{CCA} +0.1V)
V_{RB} Most Negative Reference Voltage (Note 6)	3.0V to 2.65V
$V_{RT}-V_{RB}$	1.8V to 2.2V
Analog Input Voltage (V_{IN})	V_{RT} to V_{RB}
t_{PWL}	≥ 19 ns
t_{PWH}	≥ 27 ns

Converter Electrical Characteristics

The following specifications apply for V_{CCA} = V_{CCD} = V_{CC} = +5.25V, V_{RB} = 3.0V, V_{RT} = 5.0V, V_{AGND} = V_{DGND} = GND, t_{PWL} = 19 ns and t_{PWH} = 27 ns unless otherwise specified. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions		Typical	Limit	Units (Limit)
STATIC CHARACTERISTICS						
	Resolution				**8**	Bits(min)
	Integral Linearity Error				**0.2**	%FS(max)
	Differential Linearity Error				**0.2**	%FS(max)
	Code Size (Note 7)			100	**25** **175**	%LSB %LSB(min) %LSB(max)
	Offset Error, Top	V_{IN} = V_{RT}			**±10**	mV(max)
	Offset Error, Bottom	V_{IN} = V_{RB}			**−15**	mV(max)
	Offset Error Temperature Coefficient				**±20**	µV/°C(max)
I_{REF}	Reference Current				**30**	mA(max)
R_{REF}	Total Reference Resistance				**67**	Ω(min)
V_{IN}	Analog Input Voltage Range				**V_{RB}** **V_{RT}**	V(min) V(max)
I_{IN}	Analog Input Constant Bias Current				**250**	µA(max)
R_{IN}	Analog Input Equivalent Resistance	V_{IN} = V_{RB}			**80**	kΩ(min)
C_{IN}	Analog Input Capacitance	V_{IN} = V_{RB}			**50**	pF(max)
DYNAMIC CHARACTERISTICS						
S/(N+D)	Signal-to-Noise+Distortion Ratio Peak-to-Peak Signal/RMS Noise	V_{IN} = 2.0 V_{p-p}, 10 MHz BW	f_{IN} = 1.248 MHz		**54**	dB(min)
			f_{IN} = 2.438 MHz		**53**	dB(min)
S/(N+D)	Signal-to-Noise+Distortion Ratio RMS Signal/RMS Noise	V_{IN} = 2.0 V_{p-p}, 10 MHz BW	f_{IN} = 1.248 MHz		**45**	dB(min)
			f_{IN} = 2.438 MHz		**44**	dB(min)

Converter Electrical Characteristics

The following specifications apply for $V_{CCA} = V_{CCD} = V_{CC} = +5.25V$, $V_{RB} = 3.0V$, $V_{RT} = 5.0V$, $V_{AGND} = V_{DGND} = GND$, $t_{PWL} = 19$ ns and $t_{PWH} = 27$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
DYNAMIC CHARACTERISTICS					
BW	Bandwidth, Full Scale Input	$V_{IN} = 2.0\ V_{p-p}$, No Spurious or Missing Codes		**7**	MHz(min)
BW_{SS}	−3 dB Small Signal Bandwidth	$V_{IN} = -20$ dB, FS = $0.2\ V_{p-p}$		**60**	MHz(min)
	Full Scale Transient Response			**70**	ns(min)
t_{STO}	Sampling Time Offset	$V_{CC} = +4.75V$		**−2** **10**	ns(min) ns(max)
	Aperture Jitter			**60**	ps_{rms}(max)
	Differential Phase Error	$f_S = 4 \times NTSC$	0.5	**1.0**	Degree(max)
	Differential Gain Error	$f_S = 4 \times NTSC$	1.0	**2.0**	%(max)

DC Electrical Characteristics

The following specifications apply for $V_{CCA} = V_{CCD} = V_{CC} = +5.25V$, $V_{RB} = 3.0V$, $V_{RT} = 5.0V$, $V_{AGND} = V_{DGND} = GND$, $t_{PWL} = 19$ ns and $t_{PWH} = 27$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit	Units (Limit)
$V_{IN(1)}$	Logical "1" Input Voltage			**2.4**	V(min)
$V_{IN(0)}$	Logical "0" Input Voltage			**0.4**	V(max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 2.4V$		**50** **−200**	μA(max) μA(min)
		$V_{IN} = V_{CC} = +5.25V$		**1.0**	mA(max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0.4V$		**−0.6**	mA(max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = -400\ \mu A$		**2.4**	V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = 4.0$ mA		**0.5**	V(max)
	Short-Circuit Output Current	Output High, One Pin to Ground, One Second Duration Max		**−40**	mA(max)
C_I	Digital Input Capacitance	f = 1 MHz		15	pF(max)
I_{CC}	V_{CCA} and V_{CCD} Supply Current	(Note 8)		**160**	mA(max)

AC Electrical Characteristics

The following specifications apply for $V_{CCA} = V_{CCD} = V_{CC} = +5.25V$, $V_{RB} = 3.0V$, $V_{RT} = 5.0V$, $V_{AGND} = V_{DGND} = GND$, $t_{PWL} = 19$ ns, and $t_{PWH} = 27$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit	Units (Limit)
f_S	Maximum Conversion Rate	$V_{CC} = +4.75V$		**20**	MSPS(min)
t_{PWL}	Convert (CONV) Pulse Width, Low			**19**	ns(min)
t_{PWH}	Convert (CONV) Pulse Width, High			**27**	ns(min)
t_D	Output Delay	$V_{CC} = +4.75V$, Load 1, *Figure 4*		**35**	ns(max)
t_{HO}	Output Hold Time	Load 1, *Figure 4*		**5**	ns(min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 3: Applied voltage must be current-limited to the specified range.

Note 4: Forcing voltage must be limited to specified range.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), θ_{JC} (package junction to case thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax)} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 175°C$, and the typical thermal resistances (θ_{JA} and θ_{JC}) of the ADC0881 follow:

Suffixes	Package Number	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CCJ	J28A	50	12
CCN	N28A	45	17
CCV	V28A	65	14

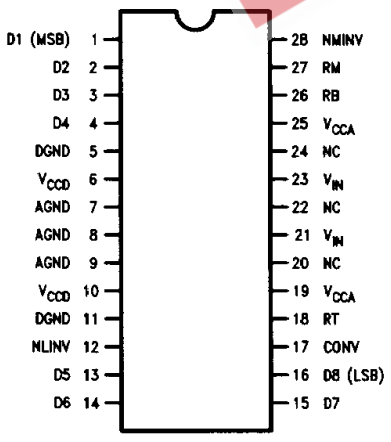
Note 6: V_{RT} must be more positive than V_{RB}, and the voltage reference differential must be within the specified range.

Note 7: Code size is the size of the individual codes, from code transition to code transition. It is often expressed as a percentage of the ideal code size. The ideal code size is given by: Input Voltage Range/2^N. Where N is the number of bits of resolution of the A/D converter.

Note 8: Worst case, all digital inputs and outputs LOW.

Connection Diagrams

28-Lead CERDIP—J Package
28-Lead Plastic DIP—N Package



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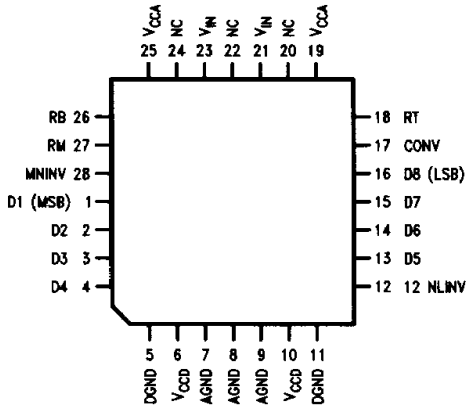
Top View

28-Lead Plastic Chip Carrier—V Package



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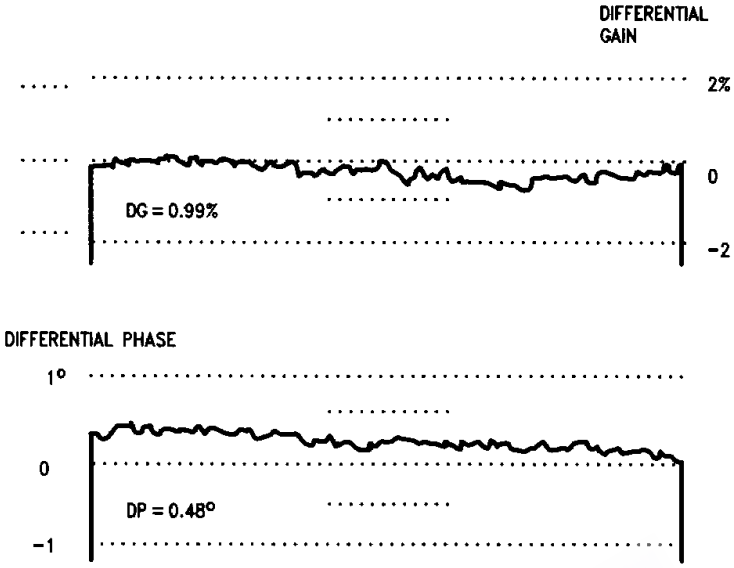
Top View

Ordering Information

Commercial ($0°C \le T_A \le 70°C$)	Package
ADC0881CCN/TDC1058N6C	N28B, 28-Pin Plastic
ADC0881CCJ/TDC1058B6C	J28A, 28-Pin CERDIP
ADC0881CCV/TDC1058R3C	V28A, 28-Lead Plastic Chip Carrier

Typical Performance Characteristics (T_A = 25°C, V_{CC} = +5V)

Differential Phase and Gain



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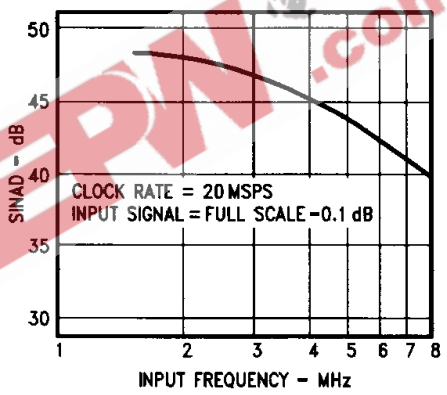
Convert Frequency = 14.3181800 MHz
Analog Input = 3.57954550 MHz

SINAD (Signal to Noise + Distortion Ratio) vs Input Frequency



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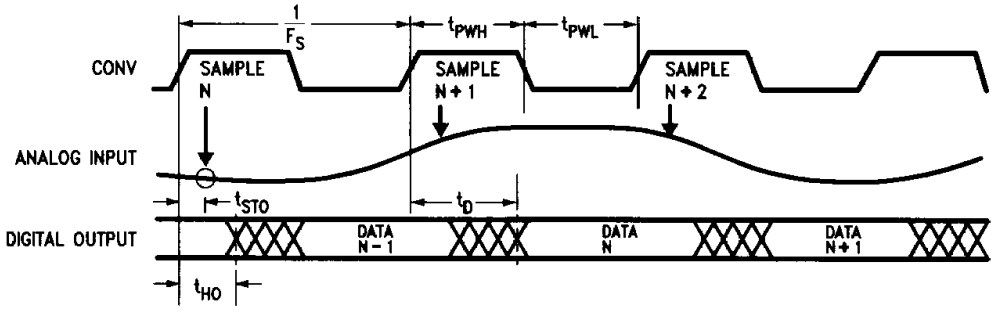

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FIGURE 1. Timing Diagram

Typical Performance Characteristics (Continued)

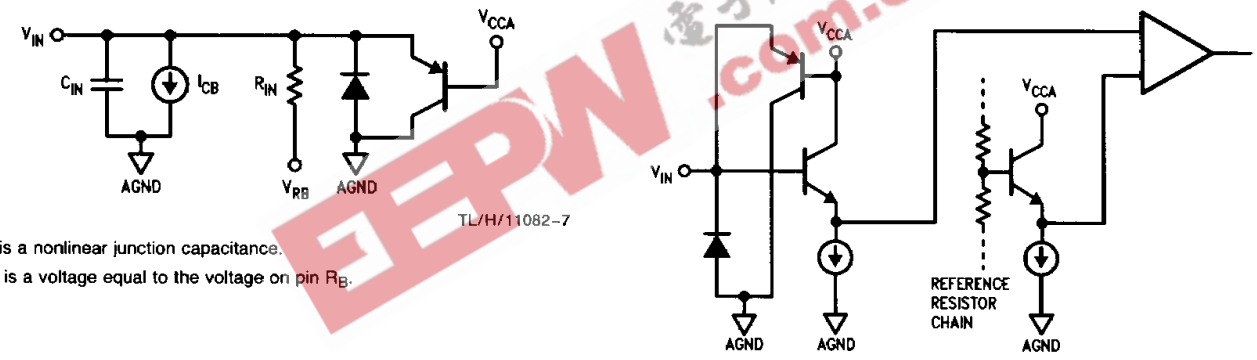
TABLE I. Output Coding Table

Input Voltage	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = HIGH NLINV = HIGH	NMINV = LOW NLINV = LOW	NMINV = LOW NLINV = HIGH	NMINV = HIGH NLINV = LOW
5.0000V	0000 0000	1111 1111	1000 0000	0111 1111
4.9922V	0000 0001	1111 1110	1000 0001	0111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
4.0078V	0111 1111	1000 0000	1111 1111	0000 0000
4.0000V	1000 0000	0111 1111	0000 0000	1111 1111
3.9922V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3.0156V	1111 1110	0000 0001	0111 1110	1000 0001
3.0078V	1111 1111	0000 0000	0111 1111	1000 0000

Note 1: NMINV and NLINV are to be considered DC controls, they may be tied to V_{CC} for a logic "1" or to ground for a logic "0".

Note 2: Voltages are code midpoints.

Simplified Input and Output Circuits



C_{IN} is a nonlinear junction capacitance.

V_{RB} is a voltage equal to the voltage on pin R_B.

FIGURE 2. Simplified Analog Input Circuits

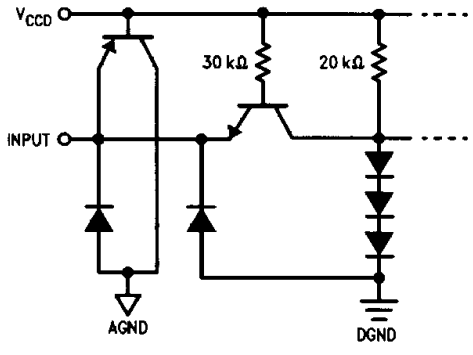


FIGURE 3. Simplified Digital Convert Input Circuit

Simplified Input and Output Circuits (Continued)

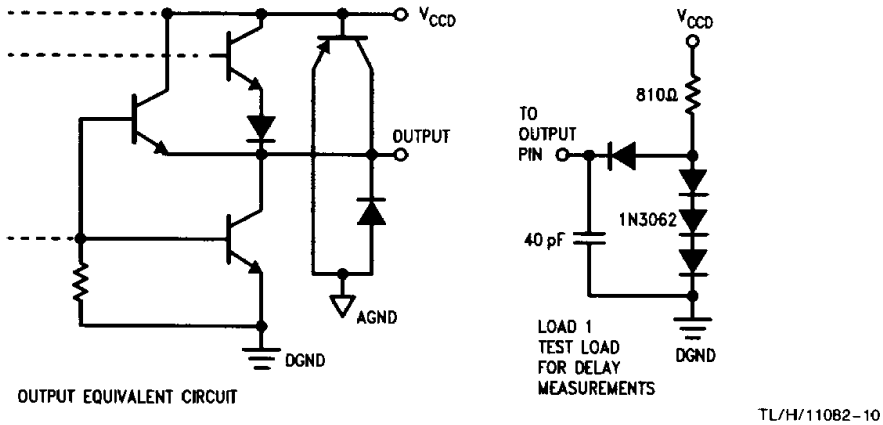


FIGURE 4. Simplified Digital Output Circuit

Pin Descriptions

V_{CCD} (6,10) These are the digital power supply pins. Normally, +5 V_{DC} should be applied and bypassed to digital ground with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

V_{CCA} (19,25) These are the analog power supply pins. Normally, +5 V_{DC} should be applied and bypassed to analog ground with a 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor.

AGND (7,8,9) Analog ground pins.

DGND (5,11) Digital ground pins.

RT (18) This pin connects to the top of the reference resistor. Normally this pin is connected to +5 V_{DC} reference and should be bypassed to AGND with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

RM (27) This pin is connected to the middle of the reference resistor. A voltage may be applied to this pin to trim the converter's integral linearity (see text).

RB (26) This pin is connected to the bottom of the reference resistor. Normally +3V is applied to this pin and should be bypassed to analog ground with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.

V_{IN} (21,23) These are the analog signal input pins, the two pins are internally connected. The input signal range is from +3V to +5V.

CONV (17) A TTL convert signal is applied to this pin. A conversion is initiated at the rising edge of the signal.

NMINV (28) This is the Not Most Significant Bit Invert pin. A TTL signal at this pin controls the format of the output data (see Table I).

NLINV (12) This is the Not Least Significant Bit Invert pin. A TTL signal at this pin controls the format of the output data (see Table I).

D1–D8 These are the digital output pins. D1 outputs the MSB data while D8 outputs the LSB data.

NC No connection.

Application Hints

OPERATION

The ADC0881 has three functional sections: a resistor/comparator array, encoding logic, and output registers. The resistor/comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (or thermometer code, since all the comparators whose reference is more negative than the input signal will be in logic "1" state and all those whose reference is more positive will be in logic "0" state). The encoding logic converts the N-of-255 code into the user's choice of coding. The output register holds the output constant between updates.

REFERENCE

The ADC0881 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. Nominally, V_{RB} is set to 3V and V_{RT} is set to 5V. However, the specifications of the ADC0881 are guaranteed as long as the following three reference operating conditions are met:

1. the voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) is within the range of 1.8V to 2.2V,
2. $V_{RT} \leq (V_{CCA} + 0.1V)$
3. $V_{RB} \geq 2.65V$.

Therefore, if the supply voltage is expected to drop below 4.9V, the reference voltages should be lowered accordingly. For instance, if the system design allows the supply voltage to drop to the minimum recommended value of 4.75V, V_{RT} should be set to 4.75V and V_{RB} should be set to 2.75V. At worst case, V_{RT} may be set at 4.85V and V_{RB} set at 2.85V. This assumes a 2 V_{p-p} maximum input signal that spans from $V_{IN} = V_{RB}$ to $V_{IN} = V_{RT}$. These reference voltages will allow the ADC0881 to give fully guaranteed performance over the full supply range. See the "Electrical Characteristics" table for further information.

Linearity is guaranteed with no adjustment; however, a midpoint tap, R_M, allows trimming of converter integral linearity as well as the creation of a nonlinear transfer function. Note that ADC0881's integral nonlinearity is ±½ LSB maximum. If the maximum non-linearity occurs at midscale then the circuit of *Figure 5* will allow the user to null out the linearity error at midscale. This adjustment may improve the overall integral linearity of the converter to less than ±½ LSB.

Application Hints (Continued)

The characteristic impedance seen at this node is approximately 220Ω and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and any noise introduced at this point will degrade the overall quantization Signal to Noise Ratio. Due to the slight variation in the reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor (0.01 μF to 0.1 μF) to ground is recommended. If the reference inputs are exercised dynamically (as in an automatic gain control circuit) a low-impedance reference source is required. The reference voltages may be varied dynamically at up to 5 MHz; however, device performance is specified with fixed reference voltages as defined in the "Electrical Characteristics" tables.

ANALOG INPUT AND SOURCE IMPEDANCE CONSIDERATIONS

For precise quantization, the ADC0881 uses latching comparators. For optimum overall system performance the source impedance of the driving circuit must be less than 25Ω. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number from 0 to 255. When a signal outside the recommended input voltage range is applied, the output will remain at either full-scale value. The input signal will not damage the ADC0881 if it remains within the range specified in the "Absolute Maximum Ratings" table. Both analog input pins (V_{IN}) are connected together internally and therefore either one or both may be used.

CONVERT

The ADC0881 requires an external convert (CONV) signal. Because the ADC0881 is a flash converter it does not require a track-and-hold circuit. A sample is taken (the outputs of the comparators are latched) within t_{STO} (Sampling Time Offset) after a rising edge on the CONV pin. The result is encoded on the falling edge, and then transferred to the output registers on the next rising edge. The output becomes valid t_D (Output Delay Time) after the rising edge of CONV and remains valid for at least t_{HO} (Output Hold Time) after the rising edge of CONV. Therefore, the value of sample N becomes valid t_D after the rising edge of clock N+1 and remains valid until t_{HO} after the rising edge of clock N+2. (See *Figure 1,* Timing Diagram.)

OUTPUT FORMAT CONTROL

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the "Output Coding Table". (See Table I.) These active low pins may be tied to V_{CC} (through a 4.7k resistor) for a logic "1" or DGND for a logic "0".

OUTPUTS

The outputs of the ADC0881 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) loads or the equivalent. The outputs hold the previous data for a minimum of t_{HO} after the rising edge of the convert signal.

POWER SUPPLIES

The ADC0881 operates from a single +5V supply voltage. All power and ground pins must be connected. V_{CCA} and V_{CCD} should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor to the analog and digital grounds respectively. A ferrite bead may be used to provide high frequency isolation between the two supply pins.

TYPICAL INTERFACE CIRCUIT

A typical interface circuit *(Figure 6)* shows an example of a high-performance application circuit for the ADC0881. The wideband analog input operational amplifier drives the A/D converter directly. Bipolar inputs to the op amp can be accommodated by adjusting the offset control. A band-gap reference diode provides a stable reference for both the offset and gain controls. All V_{IN} pins are connected close to the device package and the input amplifier's feedback loop should be closed at this point. The buffer has an inverting gain of two, increasing a 1 V_{p-p} video input signal to the recommended 2 V_{p-p} input for the ADC0881. Proper decoupling is recommended for all systems.

A variable capacitor permits amplifier optimization for either step response or frequency response. This may be replaced with a fixed value capacitor as determined by evaluation of the final PC board layout.

The bottom reference voltage (V_{RB}) is supplied by an inverting amplifier, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain.

The Inexpensive Interface Circuit shown in *Figure 7* offers considerable parts reduction for cost-sensitive applications where DC response is not required and loss of some power supply rejection is tolerable. The 200Ω resistors bias the input to +4V and provide the current to the Zener diode to provide the reference bottom voltage. The 1 μF capacitor decouples the input signal from the DC voltage present at the input of the ADC0881. The 10 μF and 0.1 μF capacitors, as well as the ferrite bead, provide power supply decoupling. The 1N5711 Schottky diodes are for protection against overvoltages at the input and are not required if these precautions are taken elsewhere in the circuit.

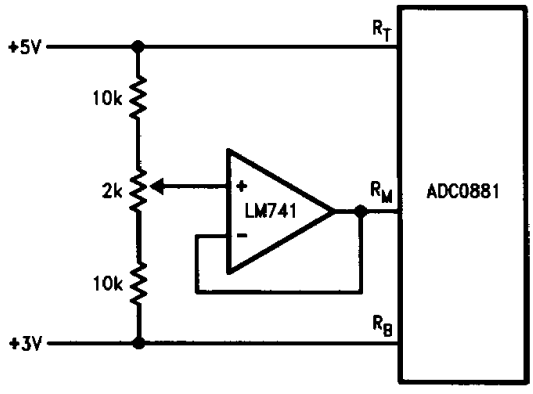


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FIGURE 5. Optional Midscale Linearity Adjust

Application Hints (Continued)

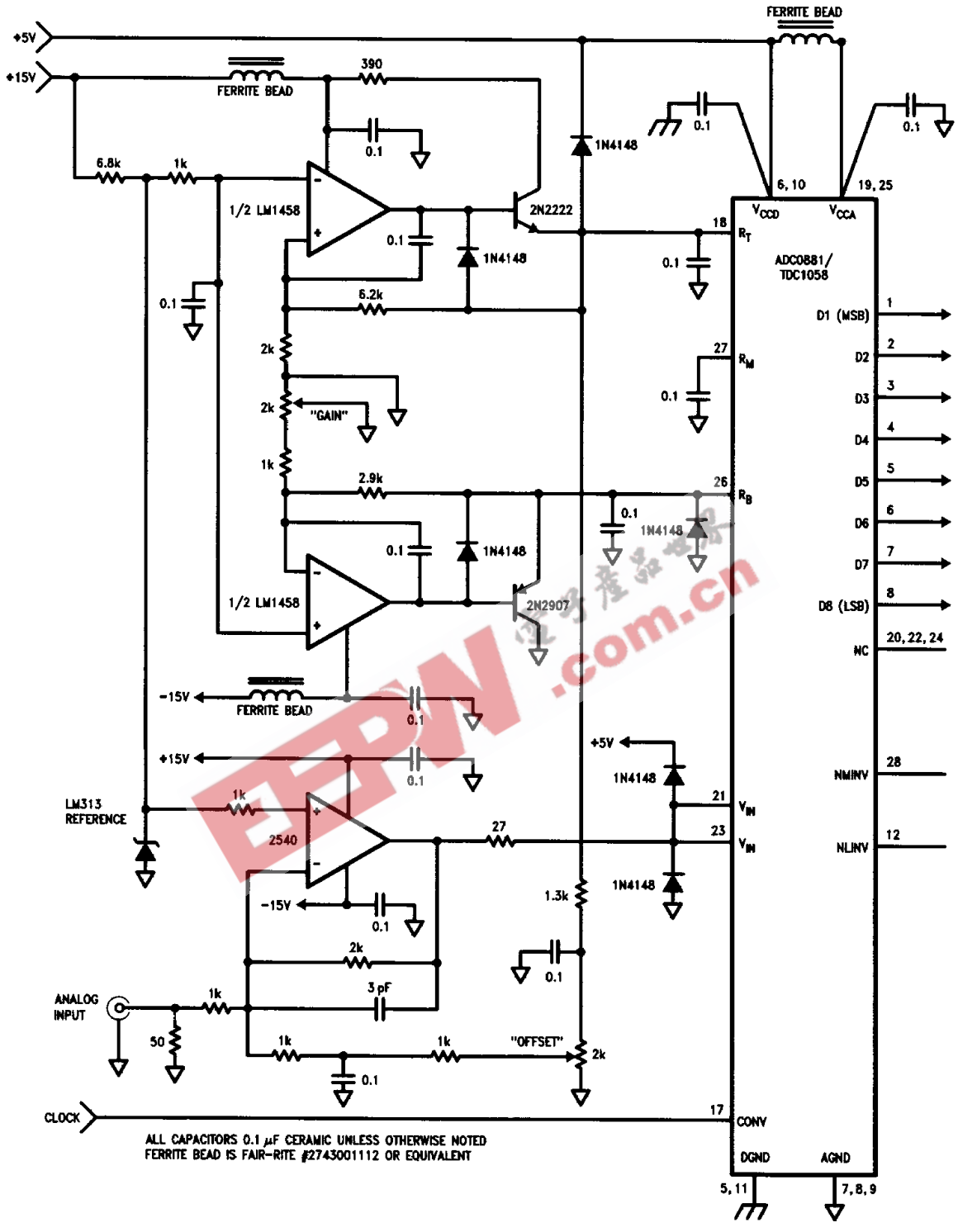

FIGURE 6. Typical Interface Circuit

Application Hints (Continued)

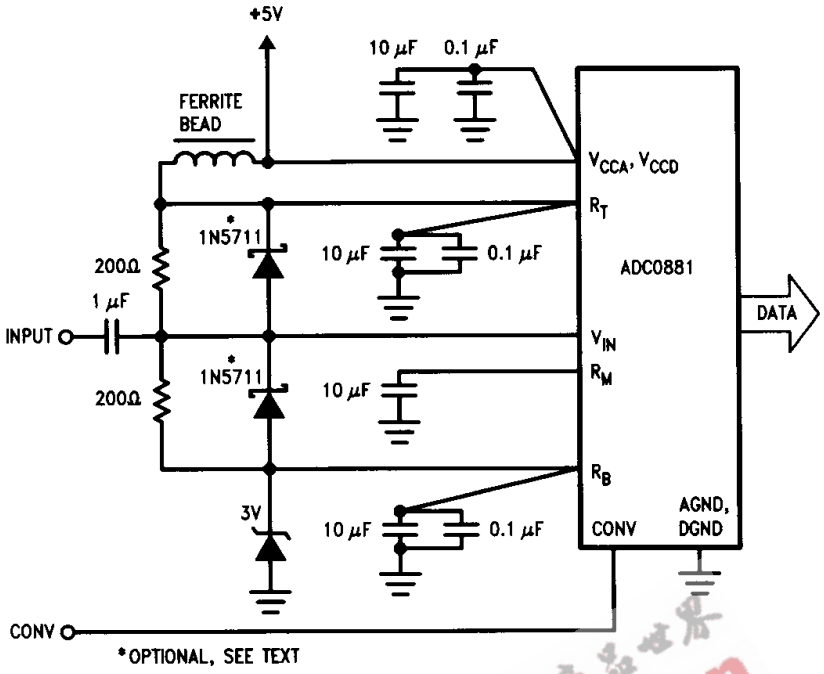

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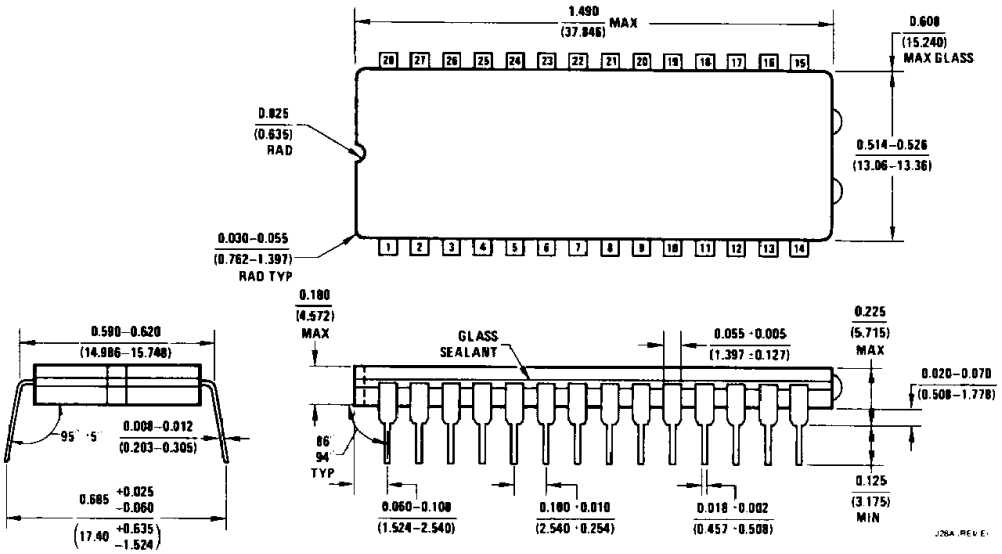
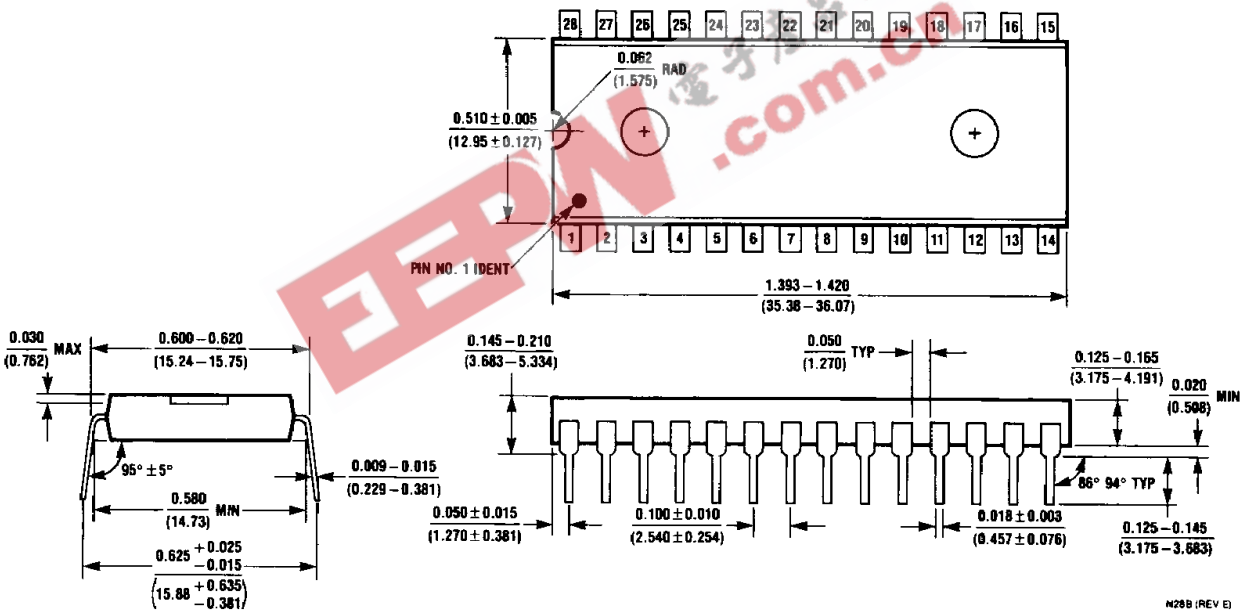
FIGURE 7. Inexpensive Interface Circuit

Physical Dimensions inches (millimeters)

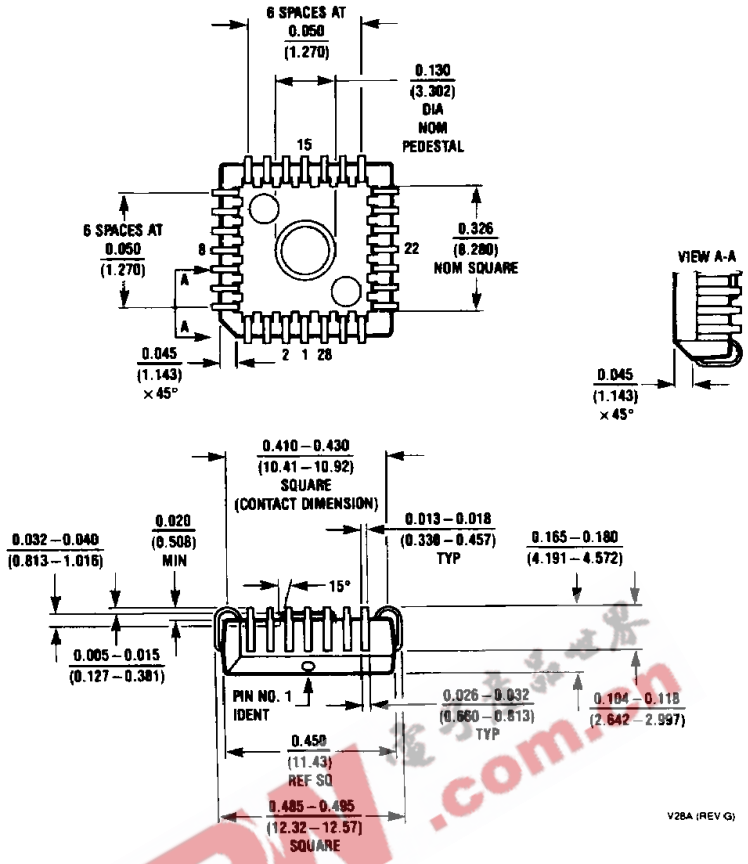


28-Pin CERDIP (J)
Order Number ADC0881CCJ or TDC1058B6C
NS Package Number J28A



28-Pin Plastic DIP (N)
Order Number ADC0881CCN or TDC1058N6C
NS Package Number N28B

Physical Dimensions inches (millimeters) (Continued)



28-Lead Plastic Chip Carrier (V)
Order Number ADC0881CCV or TDC1058R3C
NS Package Number V28A

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