DATA SHEET

ADC0803/0804
CMOS 8-bit A/D converters

Product data
Supersedes data of 2001 Aug 03

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Philips
Semiconductors

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CMOS 8-bit A/D converters ADC0803/0804

DESCRIPTION

The ADC0803 family is a series of three CMOS 8-bit successive approximation A/D converters using a resistive ladder and capacitive array together with an auto-zero comparator. These converters are designed to operate with microprocessor-controlled buses using a minimum of external circuitry. The 3-State output data lines can be connected directly to the data bus.

The differential analog voltage input allows for increased common-mode rejection and provides a means to adjust the zero-scale offset. Additionally, the voltage reference input provides a means of encoding small analog voltages to the full 8 bits of resolution.

FEATURES

- Compatible with most microprocessors
- Differential inputs
- 3-State outputs
- Logic levels TTL and MOS compatible
- Can be used with internal or external clock
- Analog input range 0 V to V_{CC}
- Single 5 V supply
- Guaranteed specification with 1 MHz clock

PIN CONFIGURATION

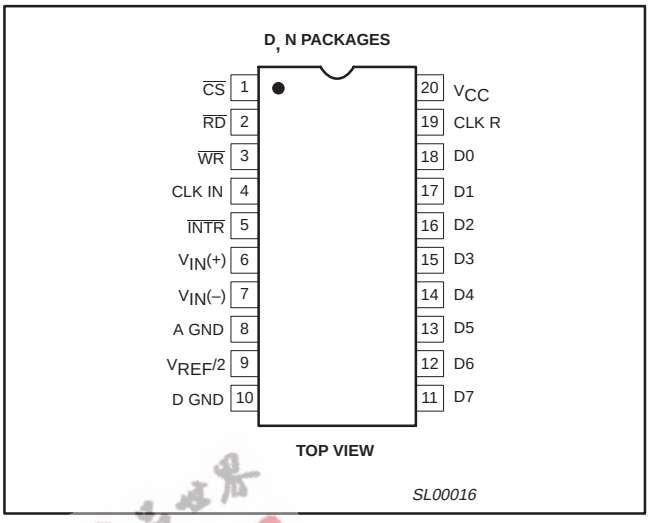


Figure 1. Pin configuration

APPLICATIONS

- Transducer-to-microprocessor interface
- Digital thermometer
- Digitally-controlled thermostat
- Microprocessor-based monitoring and control systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARKING	DWG #
20-pin plastic small outline (SO) package	0 to 70 °C	ADC0803CD, ADC0804CD	ADC0803-1CD, ADC0804-1CD	SOT163-1
20-pin plastic small outline (SO) package	–40 to 85 °C	ADC0803LCD, ADC0804LCD	ADC0803-1LCD, ADC0804-1LCD	SOT163-1
20-pin plastic dual in-line package (DIP)	0 to 70 °C	ADC0803CN, ADC0804CN	ADC0803-1CN, ADC0804-1CN	SOT146-1
20-pin plastic dual in-line package (DIP)	–40 to +85 °C	ADC0803LCN, ADC0804LCN	ADC0803-1LCN, ADC0804-1LCN	SOT146-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	Supply voltage		6.5	V
	Logic control input voltages		–0.3 to +16	V
	All other input voltages		–0.3 to (V_{CC} +0.3)	V
T_{amb}	Operating temperature range			
	ADC0803LCD/ADC0804LCD		–40 to +85	°C
	ADC0803LCN/ADC0804LCN		–40 to +85	°C
	ADC0803CD/ADC0804CD		0 to +70	°C
	ADC0803CN/ADC0804CN		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C
T_{sld}	Lead soldering temperature (10 seconds)		230	°C
P_D	Maximum power dissipation[1]	T_{amb} = 25 °C (still air)		
	N package		1690	mW
	D package		1390	mW

NOTE:
1. Derate above 25 °C, at the following rates: N package at 13.5 mW/°C; D package at 11.1 mW/°C.

BLOCK DIAGRAM

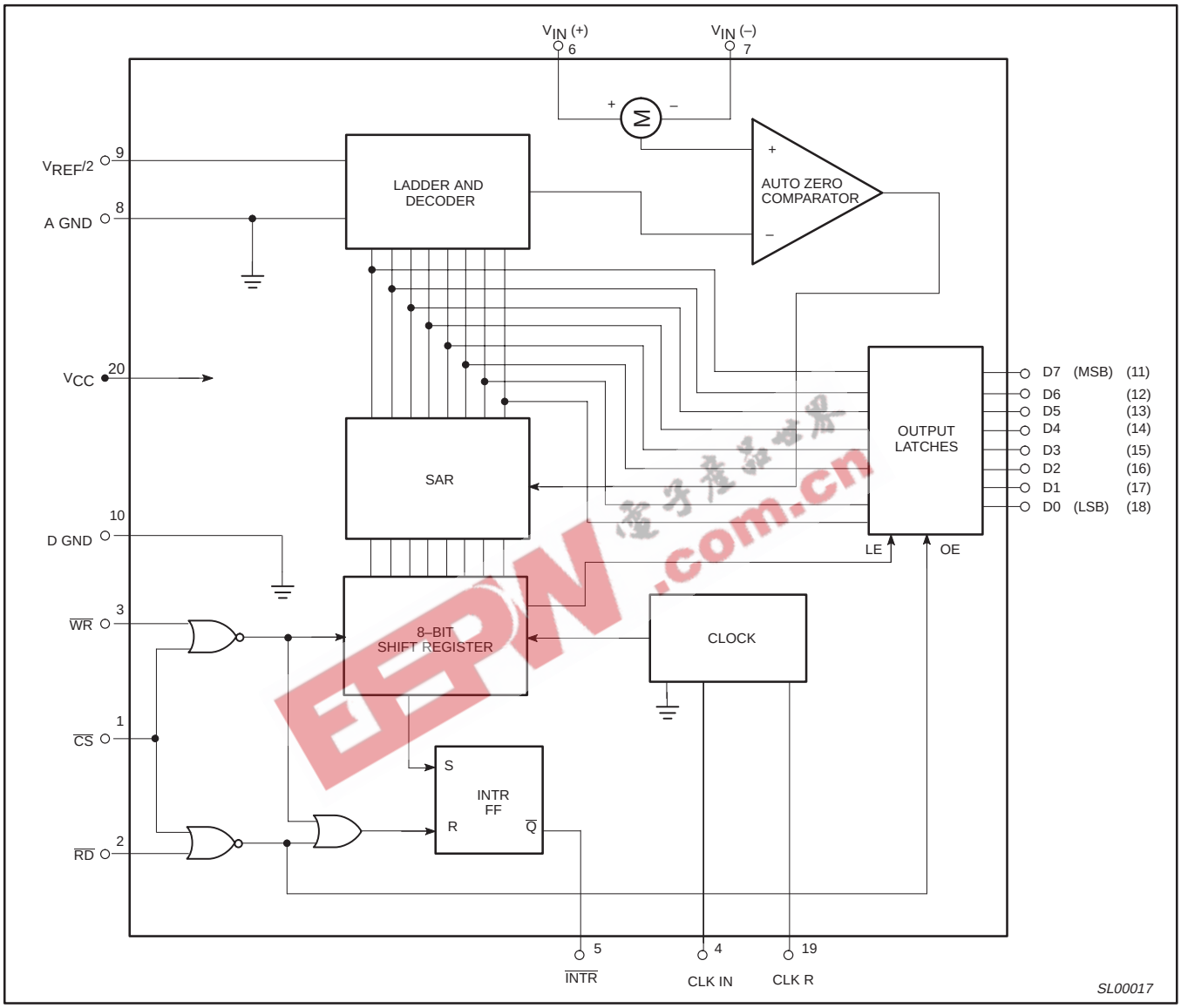


Figure 2. Block diagram

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V, f_{CLK} = 1 MHz, $T_{min} \le T_{amb} \le T_{max}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	ADC0803 relative accuracy error (adjusted)	Full-Scale adjusted			0.50	LSB
	ADC0804 relative accuracy error (unadjusted)	$V_{REF}/2$ = 2.500 V_{DC}			1	LSB
R_{IN}	$V_{REF}/2$ input resistance[3]	V_{CC} = 0 V[2]	400	680		Ω
	Analog input voltage range[3]		–0.05		V_{CC}+0.05	V
	DC common-mode error	Over analog input voltage range		1/16	1/8	LSB
	Power supply sensitivity	V_{CC} = 5V ±10%[1]		1/16		LSB
Control inputs						
V_{IH}	Logical “1” input voltage	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}
V_{IL}	Logical “0” input voltage	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
I_{IH}	Logical “1” input current	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_{IL}	Logical “0” input current	V_{IN} = 0 V_{DC}	–1	–0.005		μA_{DC}
Clock in and clock R						
V_T+	Clock in positive-going threshold voltage		2.7	3.1	3.5	V_{DC}
V_T–	Clock in negative-going threshold voltage		1.5	1.8	2.1	V_{DC}
V_H	Clock in hysteresis (V_T+)–(V_T–)		0.6	1.3	2.0	V_{DC}
V_{OL}	Logical “0” clock R output voltage	I_{OL} = 360 µA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OH}	Logical “1” clock R output voltage	I_{OH} = –360 µA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
Data output and $\overline{INTR}$						
V_{OL}	Logical “0” output voltage					
	Data outputs	I_{OL} = 1.6 mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
	$\overline{INTR}$ outputs	I_{OL} = 1.0 mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OH}	Logical “1” output voltage	I_{OH} = –360 µA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
		I_{OH} = –10 µA, V_{CC} = 4.75 V_{DC}	4.5			
I_{OZL}	3-State output leakage	V_{OUT} = 0 V_{DC}, $\overline{CS}$ = logical “1”	–3			μA_{DC}
I_{OZH}	3-State output leakage	V_{OUT} = 5 V_{DC}, $\overline{CS}$ = logical “1”			3	μA_{DC}
I_{SC}	+Output short-circuit current	V_{OUT} = 0 V, T_{amb} = 25 °C	4.5	12		mA_{DC}
I_{SC}	–Output short-circuit current	V_{OUT} = V_{CC}, T_{amb} = 25 °C	9.0	30		mA_{DC}
I_{CC}	Power supply current	f_{CLK} = 1 MHz, $V_{REF}/2$ = OPEN, $\overline{CS}$ = Logical “1”, T_{amb} = 25 °C		3.0	3.5	mA

NOTES:
1. Analog inputs must remain within the range: $-0.05 \le V_{IN} \le V_{CC} + 0.05$ V.
2. See typical performance characteristics for input resistance at V_{CC} = 5 V.
3. $V_{REF}/2$ and V_{IN} must be applied after the V_{CC} has been turned on to prevent the possibility of latching.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Conversion time			f_{CLK} = 1 MHz[1]	66		73	µs
f_{CLK}	Clock frequency[1]				0.1	1.0	3.0	MHz
	Clock duty cycle[1]				40		60	%
CR	Free-running conversion rate			$\overline{CS}$ = 0, f_{CLK} = 1 MHz $\overline{INTR}$ tied to $\overline{WR}$			13690	conv/s
$t_{W(\overline{WR})L}$	Start pulse width			$\overline{CS}$ = 0	30			ns
t_{ACC}	Access time	Output	$\overline{RD}$	$\overline{CS}$ = 0, C_L = 100 pF		75	100	ns
t_{1H}, t_{0H}	3-State control	Output	$\overline{RD}$	C_L = 10 pF, R_L = 10 kΩ See 3-State test circuit		70	100	ns
t_{W1}, t_{R1}	$\overline{INTR}$ delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
C_{IN}	Logic input=capacitance					5	7.5	pF
C_{OUT}	3-State output capacitance					5	7.5	pF

NOTE:
1. Accuracy is guaranteed at f_{CLK} = 1 MHz. Accuracy may degrade at higher clock frequencies.

FUNCTIONAL DESCRIPTION

These devices operate on the Successive Approximation principle. Analog switches are closed sequentially by successive approximation logic until the input to the auto-zero comparator [$V_{IN}(+)–V_{IN}(–)$] matches the voltage from the decoder. After all bits are tested and determined, the 8-bit binary code corresponding to the input voltage is transferred to an output latch. Conversion begins with the arrival of a pulse at the $\overline{WR}$ input if the $\overline{CS}$ input is low. On the High-to-Low transition of the signal at the WR or the CS input, the SAR is initialized, the shift register is reset, and the $\overline{INTR}$ output is set high. The A/D will remain in the reset state as long as the $\overline{CS}$ and $\overline{WR}$ inputs remain low. Conversion will start from one to eight clock periods after one or both of these inputs makes a Low-to-High transition. After the conversion is complete, the $\overline{INTR}$ pin will make a High-to-Low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion result. A read ($\overline{RD}$) operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line and enable the output latches. The device may be run in the free-running mode as described later. A conversion in progress can be interrupted by issuing another start command.

Digital Control Inputs

The digital control inputs (CS, WR, $\overline{RD}$) are compatible with standard TTL logic voltage levels. The required signals at these inputs correspond to Chip Select, START Conversion, and Output Enable control signals, respectively. They are active-Low for easy interface to microprocessor and microcontroller control buses. For applications not using microprocessors, the $\overline{CS}$ input (Pin 1) can be grounded and the A/D START function is achieved by a negative-going pulse to the $\overline{WR}$ input (Pin 3). The Output Enable function is achieved by a logic low signal at the $\overline{RD}$ input (Pin 2), which may be grounded to constantly have the latest conversion present at the output.

ANALOG OPERATION

Analog Input Current

The analog comparisons are performed by a capacitive charge summing circuit. The input capacitor is switched between $V_{IN(+)}$4 and $V_{IN(–)}$, while reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the most recent total value set by the successive approximation register.

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(–)}$ input. These transient currents occur at the leading edge of the internal clock pulses. They decay rapidly so do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors and Source Resistance

Bypass capacitors at the input will average the charges mentioned above, causing a DC and an AC current to flow through the output resistance of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input at full scale. This current can be a few microamps, so bypass capacitors should NOT be used at the analog inputs of the $V_{REF}/2$ input for high resistance sources (> 1 kΩ). If input bypass capacitors are desired for noise filtering and a high source resistance is desired to minimize capacitor size, detrimental effects of the voltage drop across the input resistance can be eliminated by adjusting the full scale with both the input resistance and the input bypass capacitor in place. This is possible because the magnitude of the input current is a precise linear function of the differential voltage.

Large values of source resistance where an input bypass capacitor is not used will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (< 1 kΩ) for a passive RC section or add an op amp active filter (low pass). For applications with source resistances at or below 1 kΩ, a 0.1 µF bypass capacitor at the inputs will prevent pickup due to series lead inductance or a long wire. A 100 Ω series resistor can be used to isolate this capacitor (both the resistor and capacitor should be placed out of the feedback loop) from the output of the op amp, if used.

Analog Differential Voltage Inputs and Common-Mode Rejection

These A/D converters have additional flexibility due to the analog differential voltage input. The $V_{IN(-)}$ input (Pin 7) can be used to subtract a fixed voltage from the input reading (tare correction). This is also useful in a 4/20 mA current loop conversion. Common-mode noise can also be reduced by the use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4.5 clock periods. The maximum error due to this time difference is given by:

$$V(max) = (V_P)\ (2f_{CM})\ (4.5/f_{CLK}),$$

where:

V = error voltage due to sampling delay

V_P = peak value of common-mode voltage

f_{CM} = common mode frequency

For example, with a 60 Hz common-mode frequency, f_{cm}, and a 1 MHz A/D clock, f_{CLK}, keeping this error to 1/4 LSB (about 5 mV) would allow a common-mode voltage, V_P, which is given by:

$$V_P = \frac{[V(max)\ (f_{CLK})}{(2f_{CM})(4.5)}$$

or

$$V_P = \frac{(5\ x\ 10^{-3})\ (10^4)}{(6.28)\ (60)\ (4.5)} = 2.95V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode voltage levels than this, however.

An analog input span less than the full 5 V capability of the device, together with a relatively large zero offset, can be easily handled by use of the differential input. (See Reference Voltage Span Adjust).

Noise and Stray Pickup

The leads of the analog inputs (Pins 6 and 7) should be kept as short as possible to minimize input noise coupling and stray signal pick-up. Both EMI and undesired digital signal coupling to these inputs can cause system errors. The source resistance for these inputs should generally be below 5 kΩ to help avoid undesired noise pickup. Input bypass capacitors at the analog inputs can create errors as described previously. Full scale adjustment with any input bypass capacitors in place will eliminate these errors.

Reference Voltage

For application flexibility, these A/D converters have been designed to accommodate fixed reference voltages of 5V to Pin 20 or 2.5 V to Pin 9, or an adjusted reference voltage at Pin 9. The reference can be set by forcing it at $V_{REF}/2$ input, or can be determined by the supply voltage (Pin 20). Figure 6 indicates how this is accomplished.

Reference Voltage Span Adjust

Note that the Pin 9 ($V_{REF}/2$) voltage is either 1/2 the voltage applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. In addition to allowing for flexible references and full span voltages, this also allows for a ratiometric voltage reference. The internal gain of the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at Pin 9.

For example, a dynamic voltage range of the analog input voltage that extends from 0 to 4 V gives a span of 4 V (4–0), so the $V_{REF}/2$ voltage can be made equal to 2 V (half of the 4 V span) and full scale output would correspond to 4 V at the input.

On the other hand, if the dynamic input voltage had a range of 0.5 to 3.5 V, the span or dynamic input range is 3 V (3.5–0.5). To encode this 3 V span with 0.5 V yielding a code of zero, the minimum expected input (0.5 V, in this case) is applied to the $V_{IN}(-)$ pin to account for the offset, and the $V_{REF}/2$ pin is set to 1/2 the 3 V span, or 1.5 V. The A/D converter will now encode the $V_{IN}(+)$ signal between 0.5 and 3.5 V with 0.5 V at the input corresponding to a code of zero and 3.5 V at the input producing a full scale output code. The full 8 bits of resolution are thus applied over this reduced input voltage range. The required connections are shown in Figure 7.

Operating Mode

These converters can be operated in two modes:

1) absolute mode
2) ratiometric mode

In absolute mode applications, both the initial accuracy and the temperature stability of the reference voltage are important factors in the accuracy of the conversion. For $V_{REF}/2$ voltages of 2.5 V, initial errors of ±10 mV will cause conversion errors of ±1 LSB due to the gain of 2 at the $V_{REF}/2$ input. In reduced span applications, the initial value and stability of the $V_{REF}/2$ input voltage become even more important as the same error is a larger percentage of the $V_{REF}/2$ nominal value. See Figure 8.

In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter, and, therefore, cancels out in the final digital code. See Figure 9.

Generally, the reference voltage will require an initial adjustment. Errors due to an improper reference voltage value appear as full-scale errors in the A/D transfer function.

ERRORS AND INPUT SPAN ADJUSTMENTS

There are many sources of error in any data converter, some of which can be adjusted out. Inherent errors, such as relative accuracy, cannot be eliminated, but such errors as full-scale and zero scale offset errors can be eliminated quite easily. See Figure 7.

Zero Scale Error

Zero scale error of an A/D is the difference of potential between the ideal 1/2 LSB value (9.8 mV for $V_{REF}/2$=2.500 V) and that input voltage which just causes an output transition from code 0000 0000 to a code of 0000 0001.

If the minimum input value is not ground potential, a zero offset can be made. The converter can be made to output a digital code of 0000 0000 for the minimum expected input voltage by biasing the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(+)$ input. This uses the differential mode of the converter. Any offset adjustment should be done prior to full scale adjustment.

Full Scale Adjustment

Full scale gain is adjusted by applying any desired offset voltage to $V_{IN}(-)$, then applying the $V_{IN}(+)$ a voltage that is $1\text{-}^1/_2$ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of $V_{REF}/2$ input voltage (or the V_{CC} supply if there is no $V_{REF}/2$ input connection) for a digital output code which just changes from 1111 1110 to 1111 1111. The ideal $V_{IN}(+)$ voltage for this full-scale adjustment is given by:

$$V_{IN}(+) = V_{IN}(-) - 1.5 \times \frac{V_{MAX} - V_{MIN}}{255}$$

where:

V_{MAX} = high end of analog input range (ground referenced)

V_{MIN} = low end (zero offset) of analog input (ground referenced)

CLOCKING OPTION

The clock signal for these A/Ds can be derived from external sources, such as a system clock, or self-clocking can be accomplished by adding an external resistor and capacitor, as shown in Figure 11.

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF are allowed. This permits driving up to seven A/D converter CLK IN pins of this family from a single CLK R pin of one converter. For larger loading of the clock line, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin.

Restart During a Conversion

A conversion in process can be halted and a new conversion began by bringing the $\overline{CS}$ and $\overline{WR}$ inputs low and allowing at least one of them to go high again. The output data latch is not updated if the conversion in progress is not completed; the data from the previously completed conversion will remain in the output data latches until a subsequent conversion is completed.

Continuous Conversion

To provide continuous conversion of input data, the $\overline{CS}$ and $\overline{RD}$ inputs are grounded and $\overline{INTR}$ output is tied to the $\overline{WR}$ input. This $\overline{INTR}/\overline{WR}$ connection should be momentarily forced to a logic low upon power-up to insure circuit operation. See Figure 10 for one way to accomplish this.

DRIVING THE DATA BUS

This CMOS A/D converter, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry tied to the data bus will add to the total capacitive loading, even in the high impedance mode.

There are alternatives in handling this problem. The capacitive loading of the data bus slows down the response time, although DC specifications are still met. For systems with a relatively low CPU clock frequency, more time is available in which to establish proper logic levels on the bus, allowing higher capacitive loads to be driven (see Typical Performance Characteristics).

At higher CPU clock frequencies, time can be extended for I/O reads (and/or writes) by inserting wait states (8880) or using clock-extending circuits (6800, 8035).

Finally, if time is critical and capacitive loading is high, external bus drivers must be used. These can be 3-State buffers (low power Schottky is recommended, such as the N74LS240 series) or special higher current drive products designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended as the PNP input offers low loading of the A/D output, allowing better response time.

POWER SUPPLIES

Noise spikes on the V_{CC} line can cause conversion errors as the internal comparator will respond to them. A low inductance filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. A separate 5 V regulator for the converter (and other 5 V linear circuitry) will greatly reduce digital noise on the V_{CC} supply and the attendant problems.

WIRING AND LAYOUT PRECAUTIONS

Digital wire-wrap sockets and connections are not satisfactory for breadboarding this (or any) A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped or kept as far as possible from the analog signal leads. Single wire analog input leads may pick up undesired hum and noise, requiring the use of shielded leads to the analog inputs in many applications.

A single-point analog ground separate from the logic or digital ground points should be used. The power supply bypass capacitor and the self-clocking capacitor, if used, should be returned to digital ground. Any $V_{REF}/2$ bypass capacitor, analog input filter capacitors, and any input shielding should be returned to the analog ground point. Proper grounding will minimize zero-scale errors which are present in every code. Zero-scale errors can usually be traced to improper board layout and wiring.

APPLICATIONS

Microprocessor Interfacing

This family of A/D converters was designed for easy microprocessor interfacing. These converters can be memory mapped with appropriate memory address decoding for $\overline{CS}$ (read) input. The active-Low write pulse from the processor is then connected to the $\overline{WR}$ input of the A/D converter, while the processor active-Low read pulse is fed to the converter $\overline{RD}$ input to read the converted data. If the clock signal is derived from the microprocessor system clock, the designer/programmer should be sure that there is no attempt to read the converter until 74 converter clock pulses after the start pulse goes high. Alternatively, the $\overline{INTR}$ pin may be used to interrupt the processor to cause reading of the converted data. Of course, the converter can be connected and addressed as a peripheral (in I/O space), as shown in Figure 12. A bus driver should be used as a buffer to the A/D output in large microprocessor systems where the data leaves the PC board and/or must drive capacitive loads in excess of 100 pF. See Figure 14.

Interfacing the SCN8048 microcomputer family is pretty simple, as shown in Figure 13. Since the SCN8048 family has 24 I/O lines, one of these (shown here as bit 0 or port 1) can be used as the chip select signal to the converter, eliminating the need for an address decoder. The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing to a dummy address.

Digitizing a Transducer Interface Output

Circuit Description

Figure 15 shows an example of digitizing transducer interface output voltage. In this case, the transducer interface is the NE5521, an LVDT (Linear Variable Differential Transformer) Signal Conditioner. The diode at the A/D input is used to insure that the input to the A/D does not go excessively beyond the supply voltage of the A/D. See the NE5521 data sheet for a complete description of the operation of that part.

Circuit Adjustment

To adjust the full scale and zero scale of the A/D, determine the range of voltages that the transducer interface output will take on. Set the LVDT core for null and set the Zero Scale Scale Adjust Potentiometer for a digital output from the A/D of 1000 000. Set the LVDT core for maximum voltage from the interface and set the Full Scale Adjust potentiometer so the A/D output is just barely 1111 1111.

A Digital Thermostat

Circuit Description

The schematic of a Digital Thermostat is shown in Figure 16. The A/D digitizes the output of the LM35, a temperature transducer IC with an output of 10 mV per °C. With $V_{REF}/2$ set for 2.56 V, this 10 mV corresponds to 1/2 LSB and the circuit resolution is 2 °C. Reducing $V_{REF}/2$ to 1.28 yields a resolution of 1 °C. Of course, the lower $V_{REF}/2$ is, the more sensitive the A/D will be to noise.

The desired temperature is set by holding either of the set buttons closed. The SCC80C451 programming could cause the desired (set) temperature to be displayed while either button is depressed and for a short time after it is released. At other times the ambient temperature could be displayed.

The set temperature is stored in an SCN8051 internal register. The A/D conversion is started by writing anything at all to the A/D with port pin P10 set high. The desired temperature is compared with the digitized actual temperature, and the heater is turned on or off by clearing setting port pin P12. If desired, another port pin could be used to turn on or off an air conditioner.

The display drivers are NE587s if common anode LED displays are used. Of course, it is possible to interface to LCD displays as well.

TYPICAL PERFORMANCE CHARACTERISTICS

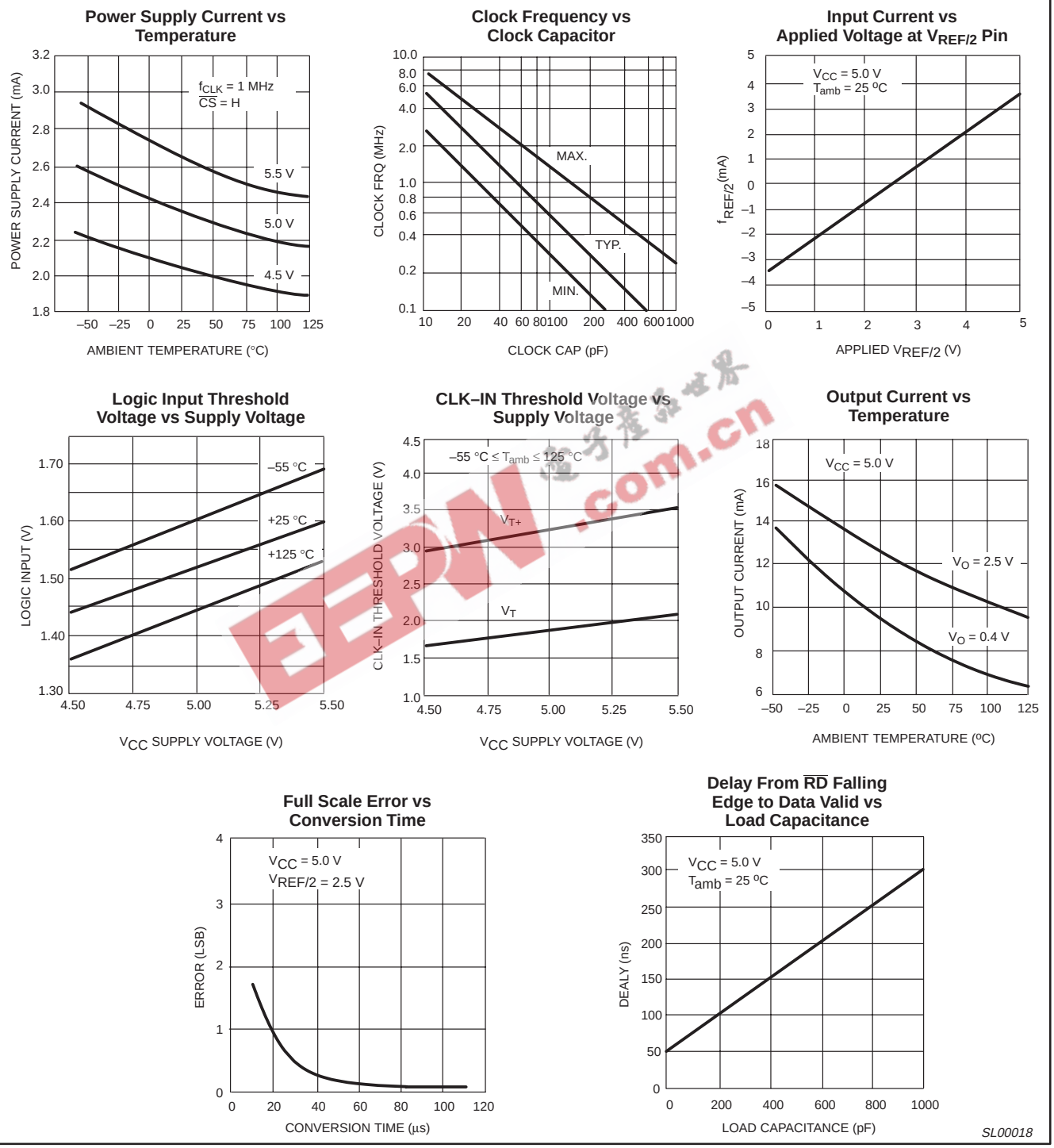


Figure 3. Typical Performance Characteristics

3-STATE TEST CIRCUITS AND WAVEFORMS (ADC0801-1)

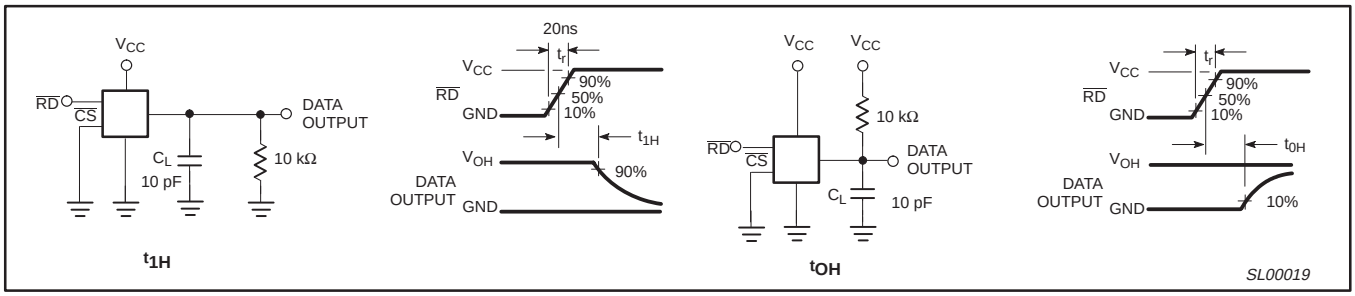
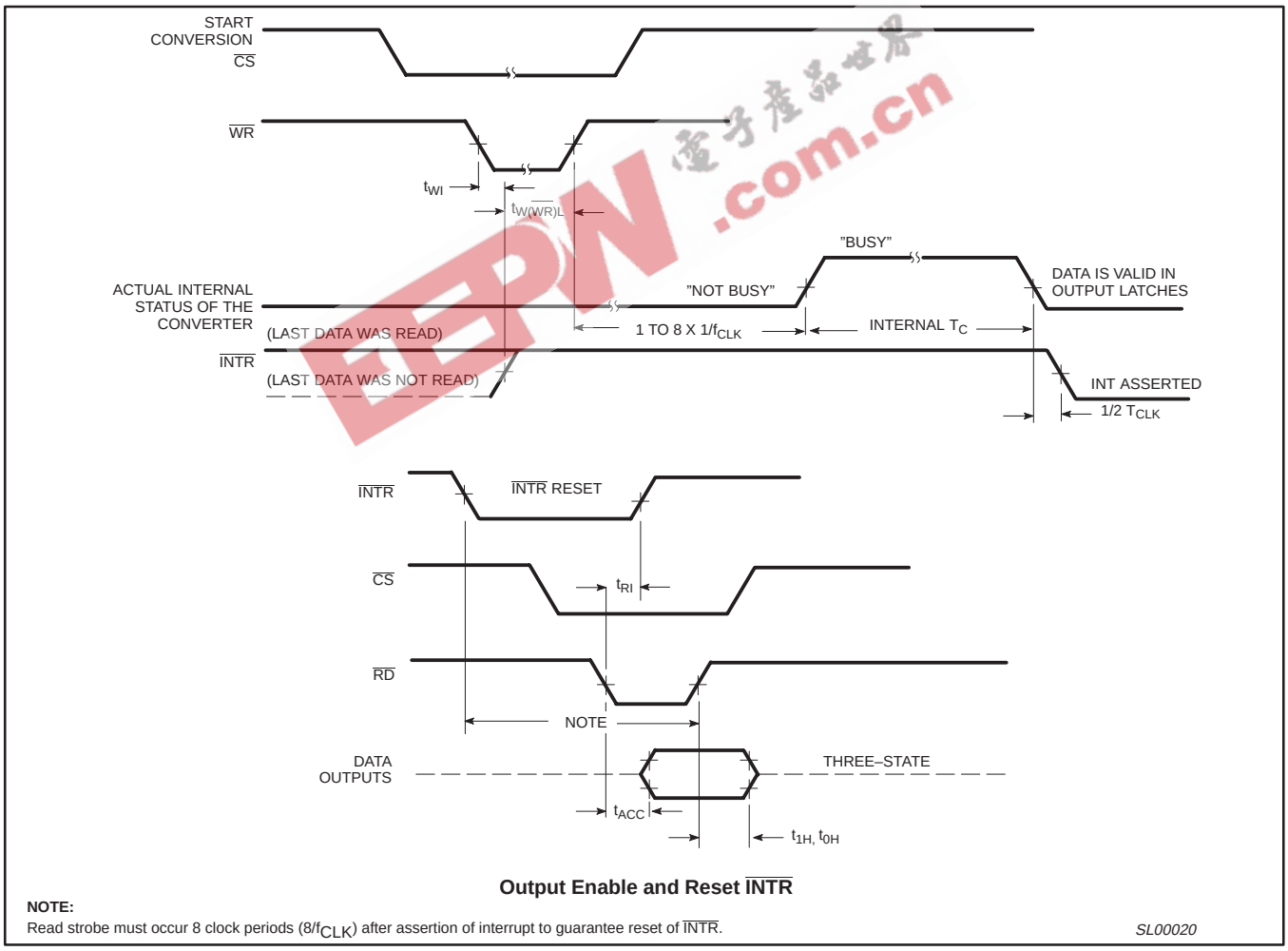


Figure 4. 3-State Test Circuits and Waveforms (ADC0801-1)

TIMING DIAGRAMS (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$

NOTE:
Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

SL00020

Figure 5. Timing Diagrams

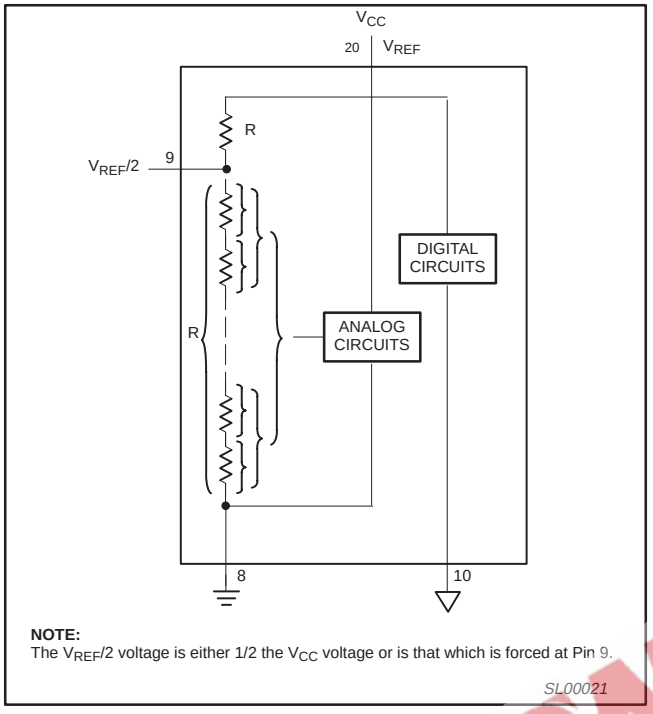


Figure 6. Internal Reference Design

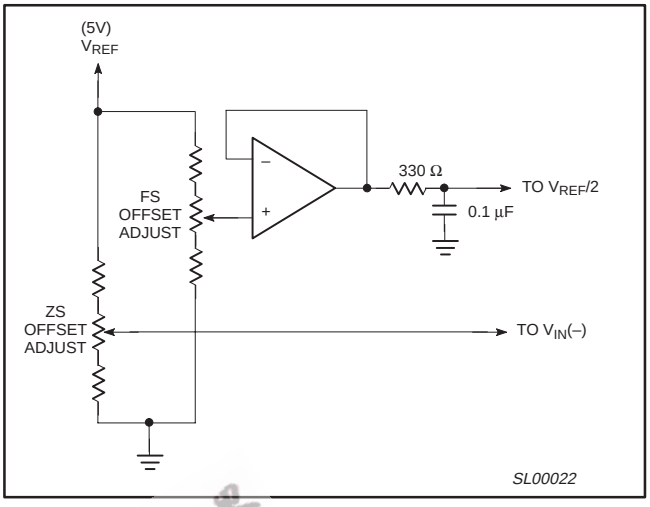


Figure 7. Offsetting the Zero Scale and Adjusting the Input Range (Span)

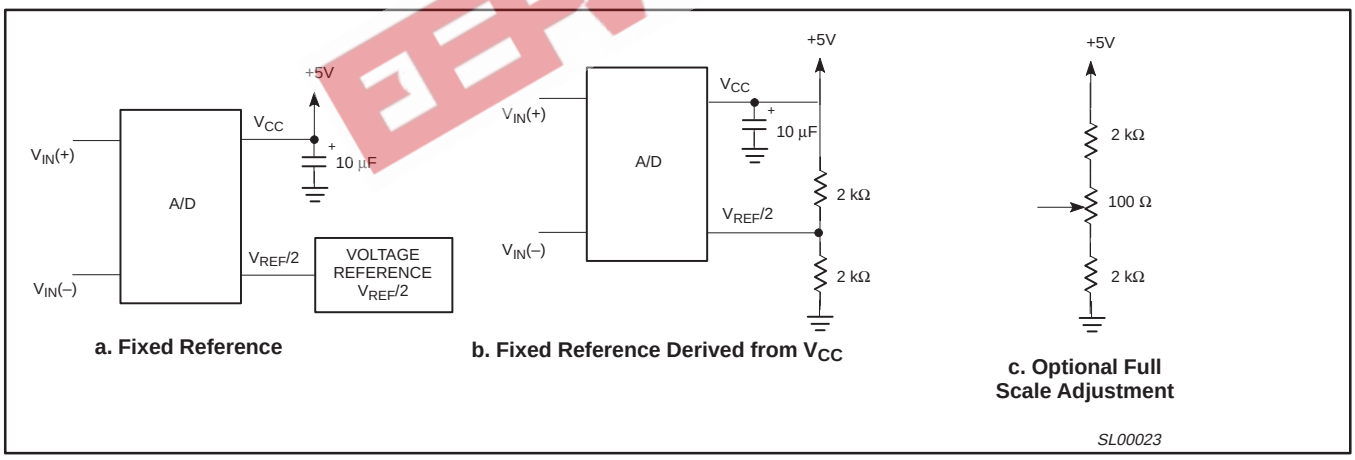


Figure 8. Absolute Mode of Operation

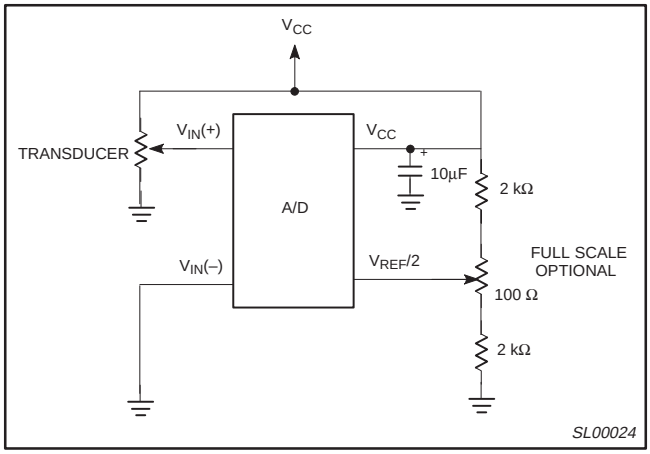


Figure 9. Ratiometric Mode of Operation with Optional Full Scale Adjustment

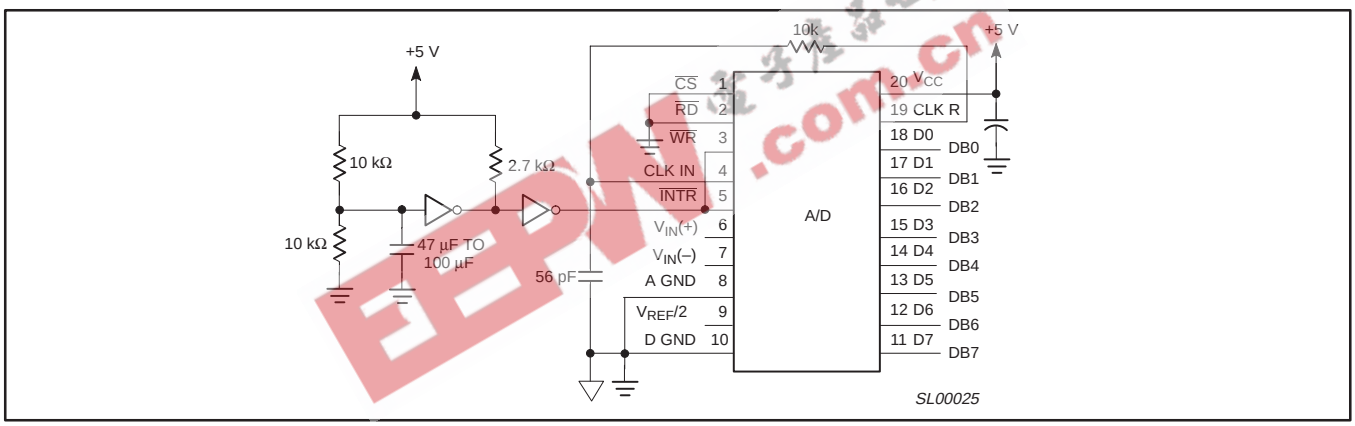


Figure 10. Connection for Continuous Conversion

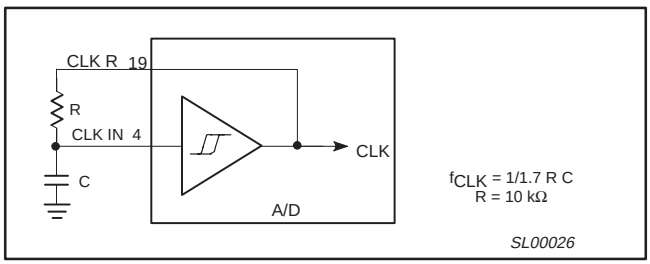


Figure 11. Self-Clocking the Converter

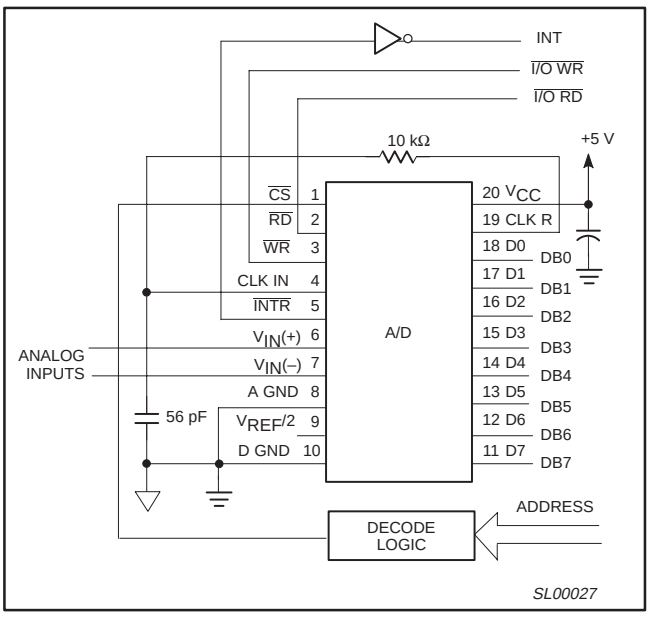


Figure 12. Interfacing to 8080A Microprocessor

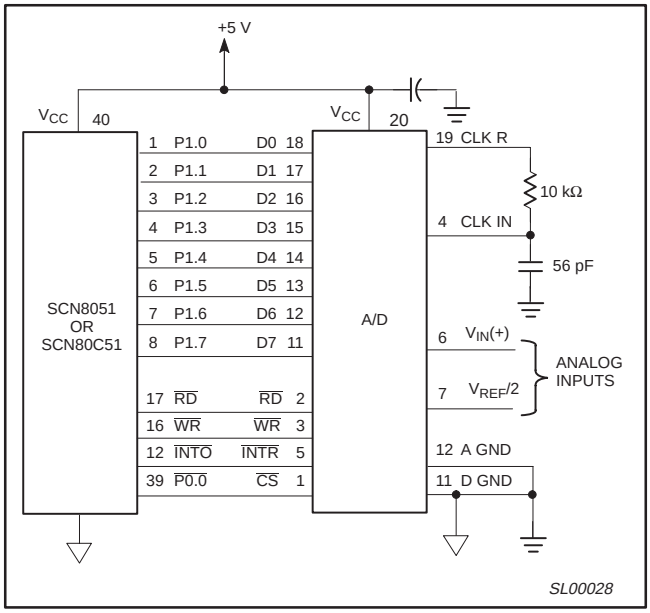


Figure 13. SCN8051 Interfacing

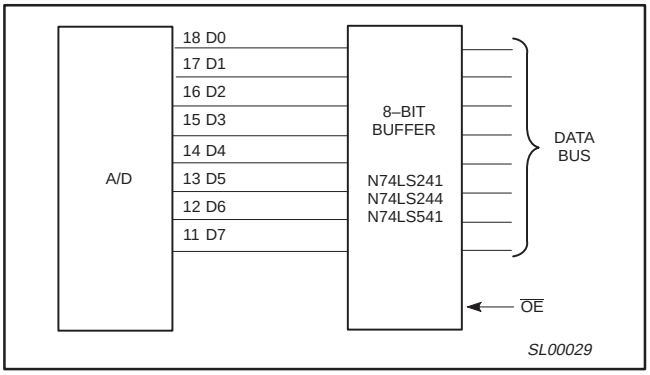


Figure 14. Buffering the A/D Output to Drive High Capacitance Loads and for Driving Off-Board Loads

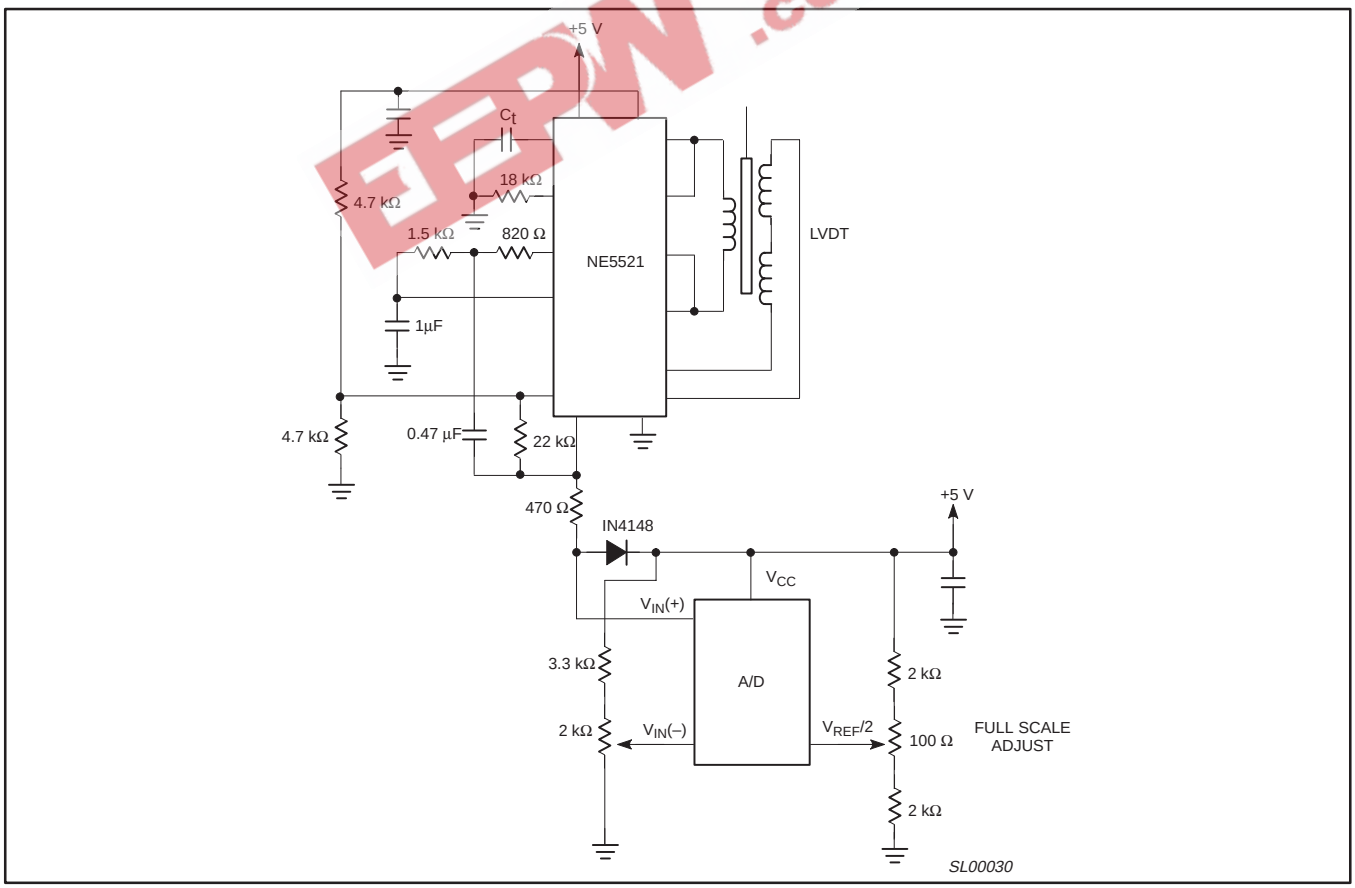


Figure 15. Digitizing a Transducer Interface Output

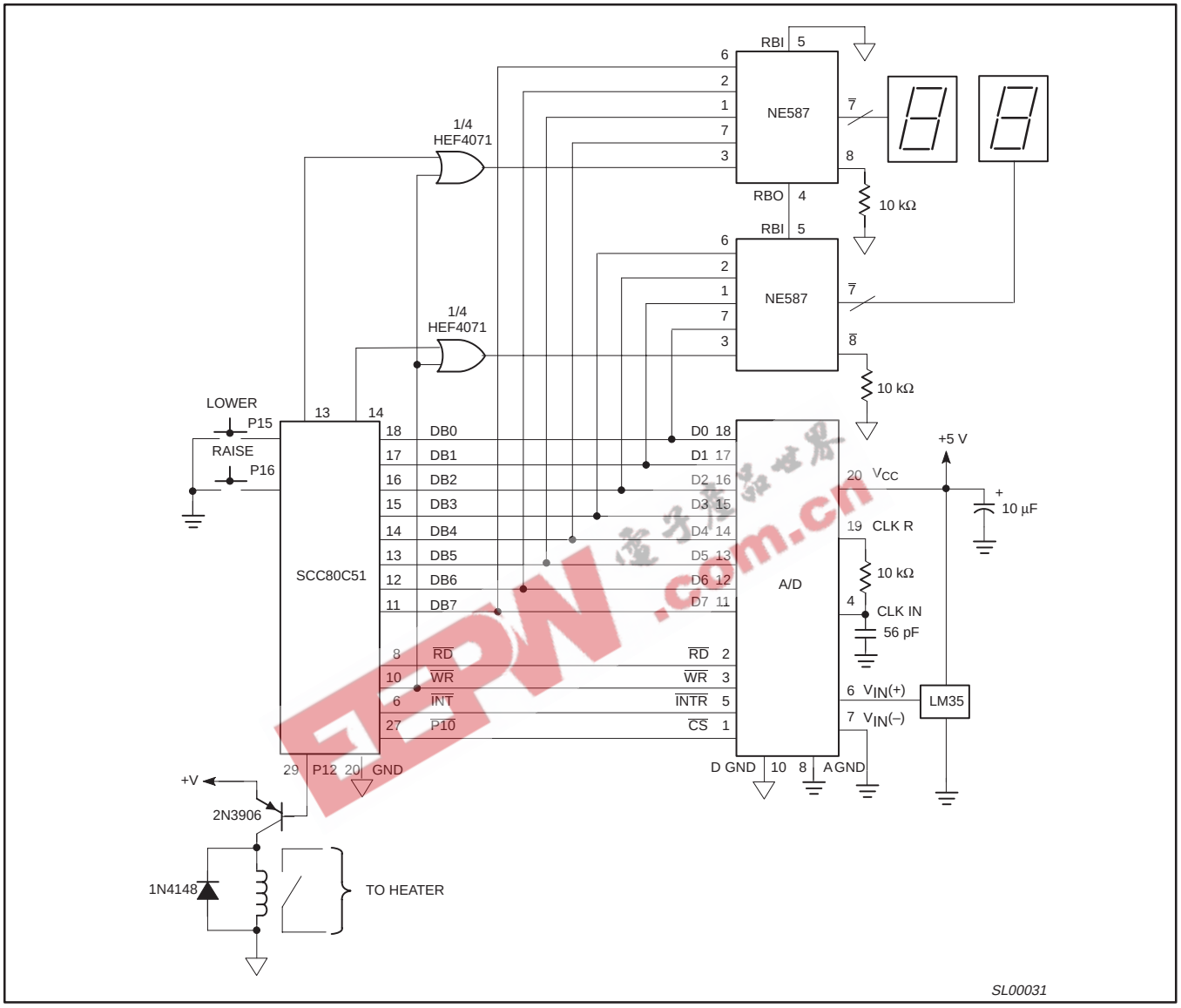
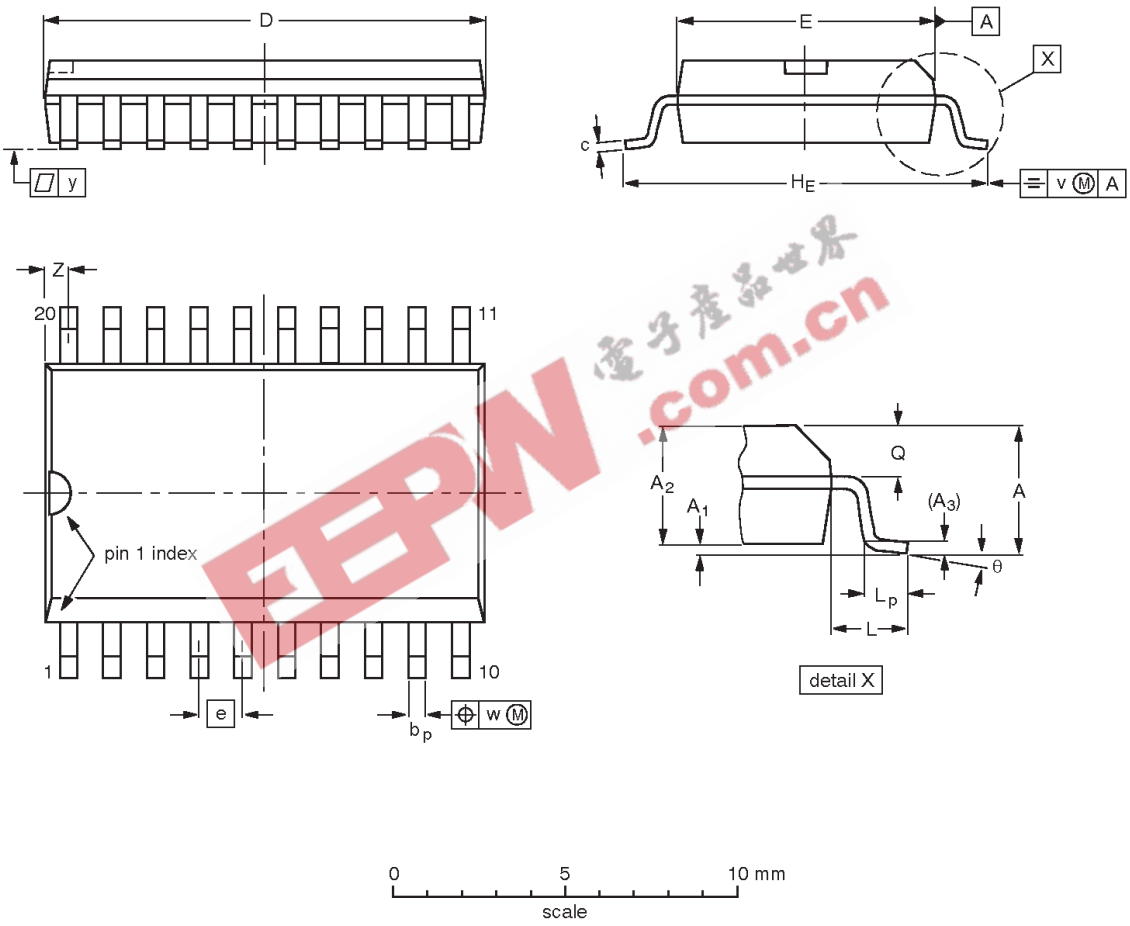


Figure 16. Digital Thermostat

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

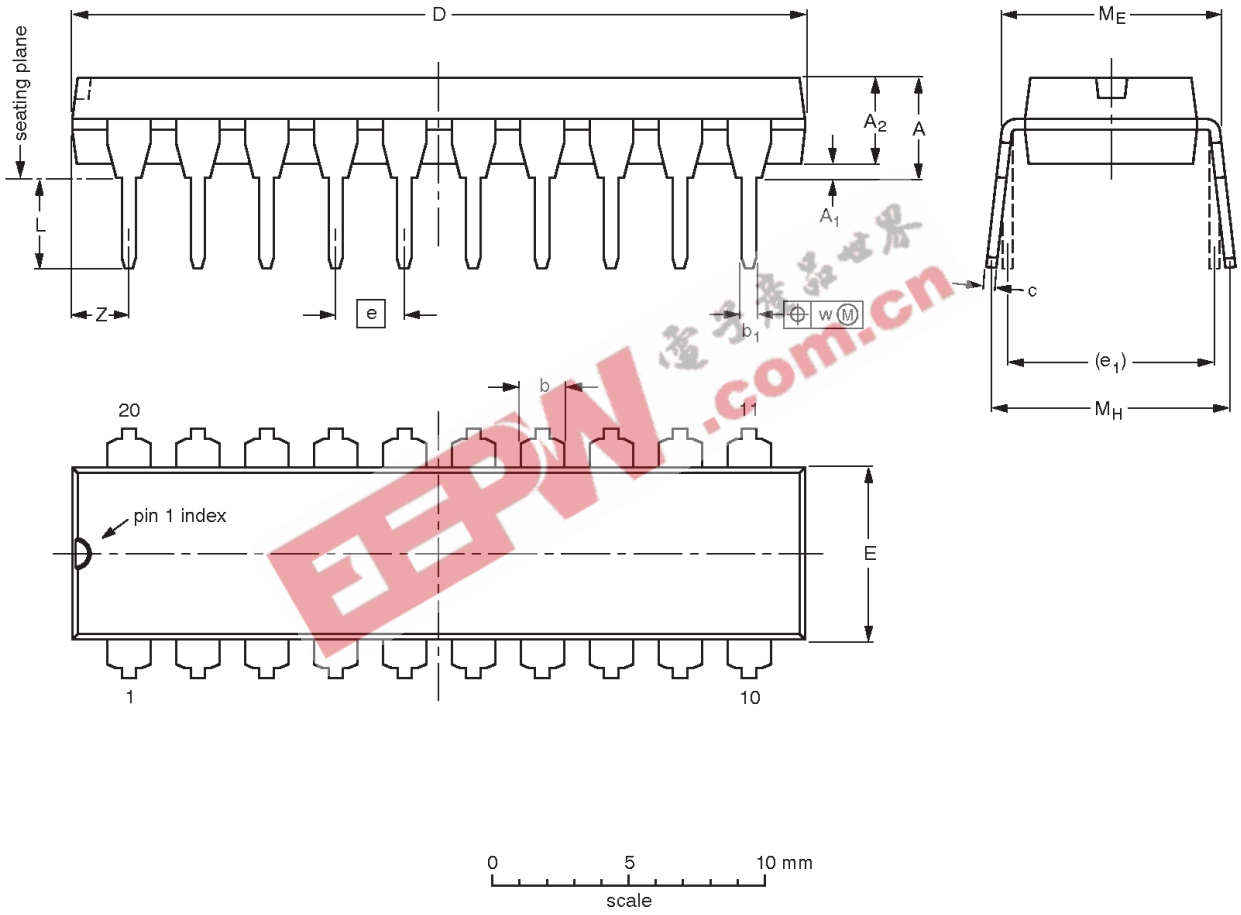
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			~~95-05-24~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20021017	**Product data; third version; supersedes data of 2001 Aug 03.** Engineering Change Notice 853–0034 28949 (date: 20020916). **Modifications:** ● Add “Topside Marking” column to Ordering Information table.
_2	20010803	**Product data; second version (9397 750 08926).** Engineering Change Notice 853–0034 26832 (date: 20010803).
_1	19940831	**Product data; initial version.** Engineering Change Notice 853–0034 13721 (date: 19940831).

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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