National Semiconductor

April 1995

ADC0852/ADC0854
Multiplexed Comparator with 8-Bit Reference Divider

General Description

The ADC0852 and ADC0854 are CMOS devices that combine a versatile analog input multiplexer, voltage comparator, and an 8-bit DAC which provides the comparator's threshold voltage (V_{TH}). The comparator provides a "1-bit" output as a result of a comparison between the analog input and the DAC's output. This allows for easy implementation of set-point, on-off or "bang-bang" control systems with several advantages over previous devices.

The ADC0854 has a 4 input multiplexer that can be software configured for single ended, pseudo-differential, and full-differential modes of operation. In addition the DAC's reference input is brought out to allow for reduction of the span.

The ADC0852 has a two input multiplexer that can be configured as 2 single-ended or 1 differential input pair. The DAC reference input is internally tied to V_{CC}.

The multiplexer and 8-bit DAC are programmed via a serial data input word. Once programmed the output is updated once each clock cycle up to a maximum clock rate of 400 kHz.

Features

- 2 or 4 channel multiplexer
- Differential or Single-ended input, software controlled
- Serial digital data interface
- 256 programmable reference voltage levels
- Continuous comparison after programming
- Fixed, ratiometric, or reduced span reference capability (ADC 0854)

Key Specifications

- Accuracy, ± ½ LSB or ± 1 LSB of Reference (0.2%)
- Single 5V power supply
- Low Power, 15 mW

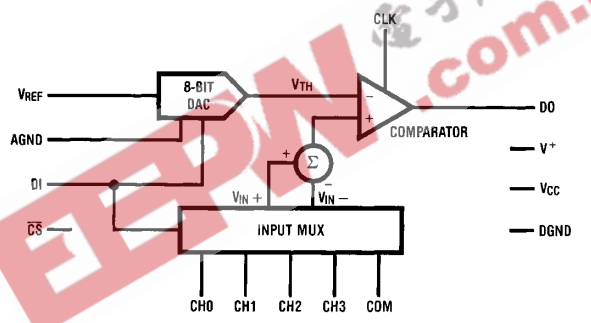

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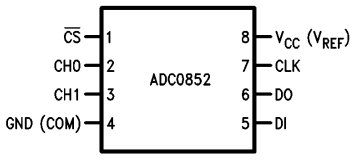
FIGURE 1. ADC0854 Simplified Block Diagram (ADC0852 has 2 input channels, COM tied to GND, V_{REF} tied to V_{CC}, V+ omitted, and one GND connection)

2 Channel and 4 Channel Pin Out

ADC0852 2-CHANNEL MUX
Dual-In-Line Package



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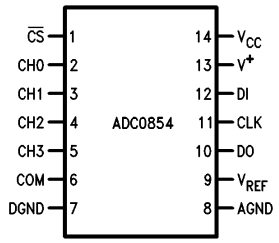
Top View

AGND and COM internally connected to GND

V_{REF} internally connected to V_{CC}

Order Number ADC0852
See NS Package Number N08E

ADC0854 4-CHANNEL MUX
Dual-In-Line Package



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Top View

Order Number ADC0854
See NS Package Number N14A

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RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic and Analog Inputs	−0.3V to V_{CC} +0.3V
Input Current per Pin	±5 mA
Input Current per Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
ESD Susceptibility (Note 14)	2000V

Operating Conditions

Supply Voltage, V_{CC}	$4.5V_{DC}$ to $6.3V_{DC}$
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0854CCN, ADC0852CCN	0°C ≤ T_A ≤ 70°C

Electrical Characteristics

The following specifications apply for V_{CC} = V+ = 5V (no V+ on ADC0852), $V_{REF} \le V_{CC}$ + 0.1V, f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Parameter	Conditions	ADC0852CCN ADC0854CCN			Units
		Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Total Unadjusted Error (Note 7) ADC0852/4/CCN	V_{REF} Forced to 5.000 V_{DC}		±1	**±1**	LSB
Comparator Offset ADC0852/4/CCN		2.5		**20**	mV
Minimum Total Ladder Resistance	ADC0854 (Note 15)	3.5	1.3	**1.3**	kΩ
Maximum Total Ladder Resistance	ADC0854 (Note 15)	3.5	5.4	**5.9**	kΩ
Minimum Common-Mode Input (Note 8)	All MUX Inputs and COM Input		GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input (Note 8)	All MUX Inputs and COM Input		V_{CC} + 0.05	**V_{CC} + 0.05**	V
DC Common-Mode Error		±1/16	±1/4	**±1/4**	LSB
Power Supply Sensitivity	V_{CC} = 5V ±5%	±1/16	±1/4	**±1/4**	LSB
V_Z, Internal diode breakdown at V+ (Note 3) MIN MAX	15 mA into V+		6.3 8.5		V V
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		−200	**−1**	µA nA
	On Channel = 0V, Off Channel = 5V		+200	**+1**	µA nA

Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = V^+ = 5V$ (no V^+ on ADC0852), $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Parameter	Conditions	ADC0852CCN ADC0854CCN			Units
		Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		+200	**+1**	μA nA
	On Channel = 0V, Off Channel = 5V		−200	**−1**	μA nA
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$		2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$		0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$	0.005	1	**1**	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$	−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$ $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		2.4 4.5	**2.4** **4.5**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{CC} = 4.75V$		0.4	**0.4**	V
I_{OUT}, TRI-STATE® Output Current (DO)	$\overline{CS}$ = Logical "1" $V_{OUT} = 0.4V$ $V_{OUT} = 5V$	−0.1 0.1	−3 3	**−3** **3**	μA μA
I_{SOURCE}	V_{OUT} Short to GND	−14	−7.5	**−6.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}	16	9.0	**8.0**	mA
I_{CC} Supply Current ADC0852	Includes DAC Ladder Current	2.7	6.5	**6.5**	mA
I_{CC} Supply Current ADC0854 (Note 3)	Does not Include DAC Ladder Current	0.9	2.5	**2.5**	mA

AC Characteristics $t_r = t_f = 20$ ns, $T_A = 25°C$

Symbol	Parameter		Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
f_{CLK}	Clock Frequency (Note 12)	MIN MAX			10	 400	kHz kHz
t_{D1}	Rising Edge of Clock to "DO" Enabled		$C_L = 100$ pF	650		1000	ns
t_r	Comparator Response Time (Note 13)		Not Including Addressing Time			$2 + 1\ \mu s$	$1/f_{CLK}$
	Clock Duty Cycle (Note 10)	MIN MAX			40 60		% %
t_{SET-UP}	CS Falling Edge or Data Input Valid to CLK Rising Edge	MAX				250	ns
t_{HOLD}	Data Input Valid after CLK Rising Edge	MIN				90	ns
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 11)	MAX	$C_L = 100$ pF	650		1000	ns
t_{1H}, t_{0H}	Rising Edge of CS to Data Output Hi-Z	MAX	$C_L = 10$ pF, $R_L = 10$k $C_L = 100$ pF, $R_L = 2$k (see TRI-STATE Test Circuits)	125	 500	250 500	ns ns
C_{IN}	Capacitance of Logic Input			5			pF
C_{OUT}	Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Internal zener diodes (approx. 7V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode ensures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+.

Note 4: Typicals are at 25°C and represent most likely parametric norm.

Note 5: Tested and guaranteed to National AOQL (Average Outgoing Quality Level).

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Total unadjusted error includes comparator offset, DAC linearity, and multiplexer error. It is expressed in LSBs of the threshold DAC's input code.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the output will be 0. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range ensures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits then 1.6 μS $\leq$ CLK Low $\leq$ 60 μS and 1.6 μS $\leq$ CLK HIGH $\leq \infty$.

Note 11: With $\overline{CS}$ low and programming complete, D0 is updated on each falling CLK edge. However, each new output is based on the comparison completed 0.5 clock cycles prior (see *Figure 5*).

Note 12: Error specs are not guaranteed at 400 kHz (see graph: Comparator Error vs. f_{CLK}).

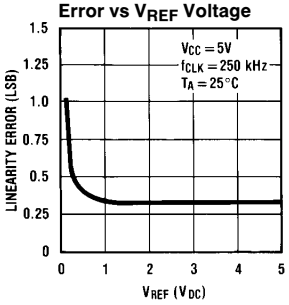
Note 13: See text, section 1.2.

Note 14: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

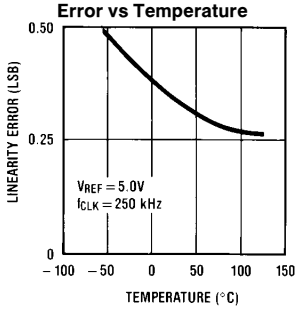
Note 15: Because the reference ladder of the ADC0852 is internally connected to V_{CC}, ladder resistance cannot be directly tested for the ADC0852. Ladder current is included in the ADC0852's supply current specification.

Typical Performance Characteristics

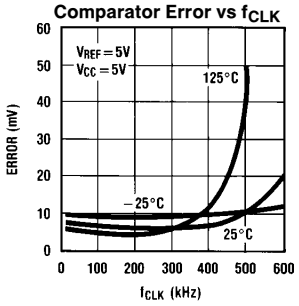
Internal DAC Linearity Error vs V_{REF} Voltage



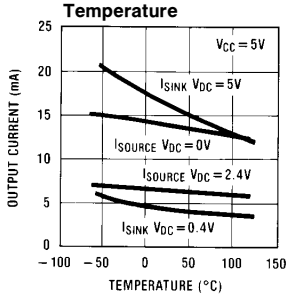
Internal DAC Linearity Error vs Temperature



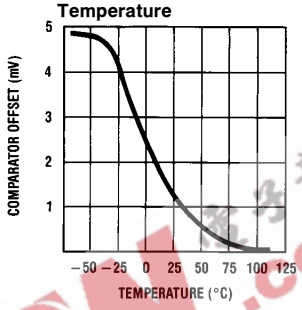
Comparator Error vs f_{CLK}



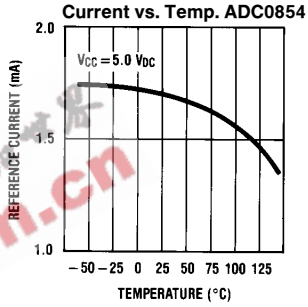
Output Current vs Temperature



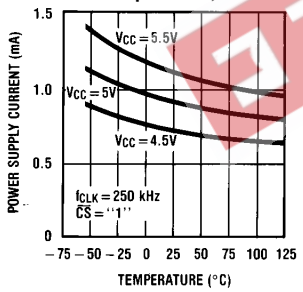
Comparator Offset vs Temperature



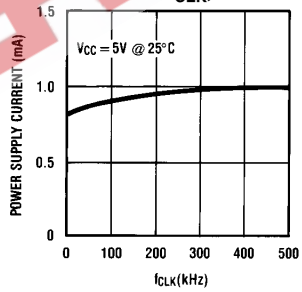
I_{REF}, Reference Current vs. Temp. ADC0854



I_{CC}, Power Supply Current vs. Temperature, ADC0854*



I_{CC}, Power Supply Current vs. f_{CLK}, ADC0854*



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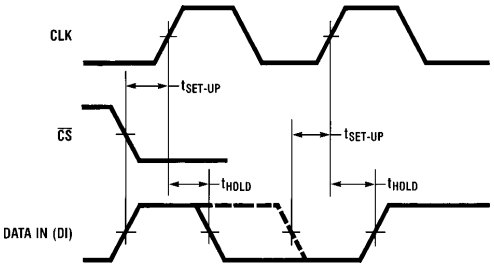
*For ADC0852 add I_{REF}

Timing Diagrams

Data Input Timing



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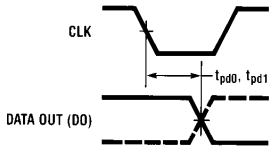
Data Output Timing



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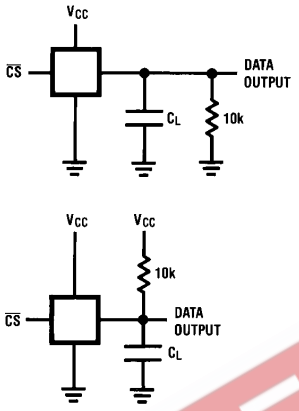
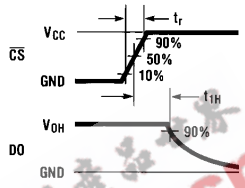
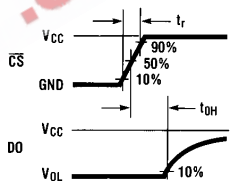
TRI-STATE Test Circuits and Waveforms







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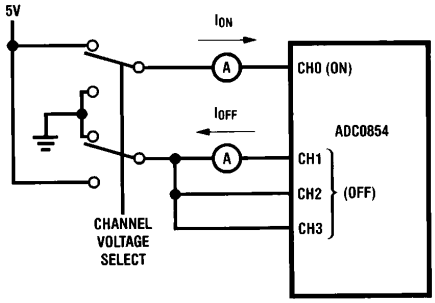
Leakage Test Circuit



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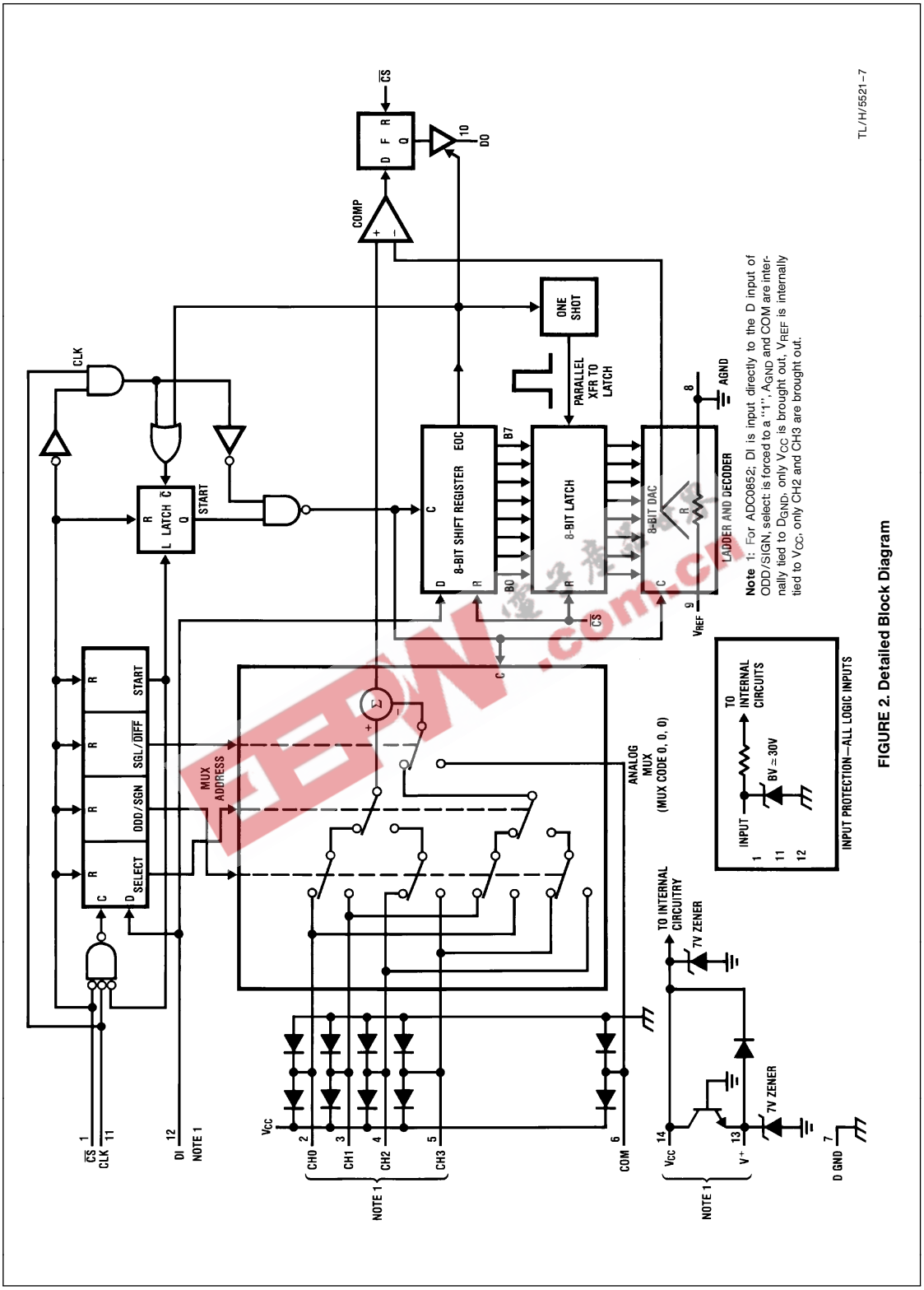

Note 1: For ADC0852; DI is input directly to the D input of ODD/SIGN select; is forced to a "1"; A_{GND} and COM are internally tied to D_{GND}, only V_{CC} is brought out, V_{REF} is internally tied to V_{CC}, only CH2 and CH3 are brought out.

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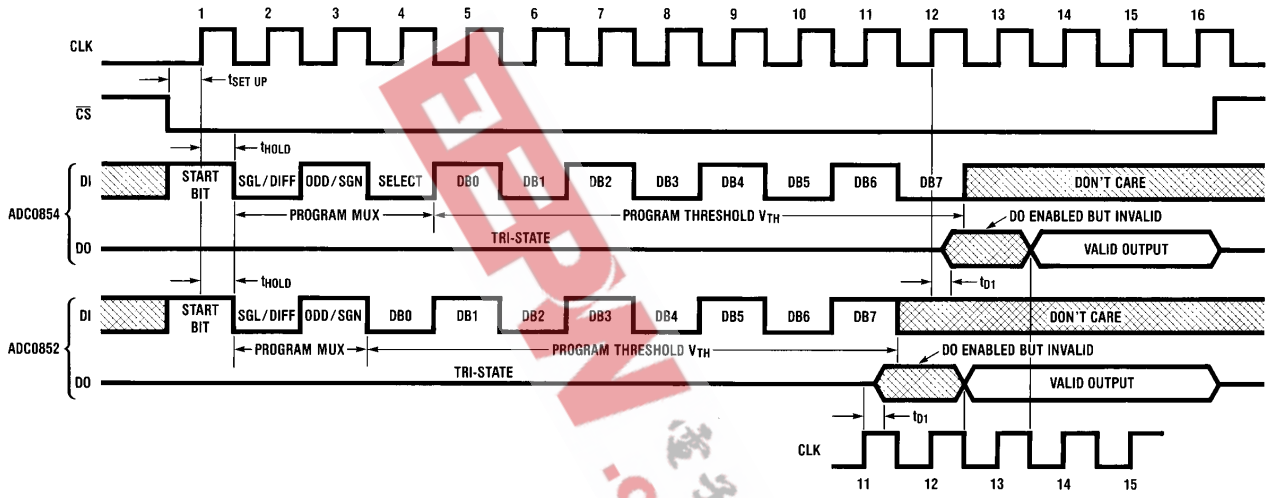
FIGURE 2. Detailed Block Diagram



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Note: Valid Output can change only on Falling Edge of CLK.

FIGURE 3. Timing Diagram

Functional Description

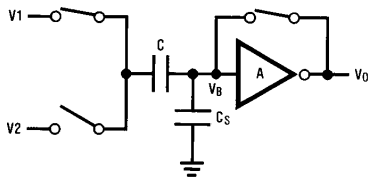
1. 1 The Sampled-data Comparator

The ADC0852 and ADC0854 utilize a sampled-data comparator structure to compare the analog difference between a selected "+" and "−" input to an 8-bit programmable threshold.

This comparator consists of a CMOS inverter with a capacitively coupled input (*Figure 4*). Analog switches connect the two comparator inputs to the input capacitor and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator and another for making the comparison.

In the first cycle (*Figure 4a*), one input switch and the inverter's feedback switch are closed. In this interval, the input capacitor (C) is charged to the connected input (V1) less the inverter's bias voltage (V_B, approx. 1.2 volts). In the second cycle (*Figure 4b*) these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter input (V_B') becomes $V_B - (V1 - V2)\frac{C}{C + C_S}$ and the output will go high or low depending on the sign of V_B'-V_B.

FIGURE 4. Sampled-Data Comparator



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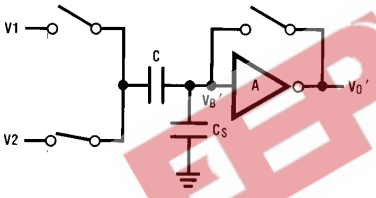
- $V_0 = V_B$
- V on C = $V_1 - V_B$
- C_S = Stray Input Node Cap.
- V_B = Inverter Input Bias Voltage

FIGURE 4a. Zeroing Phase



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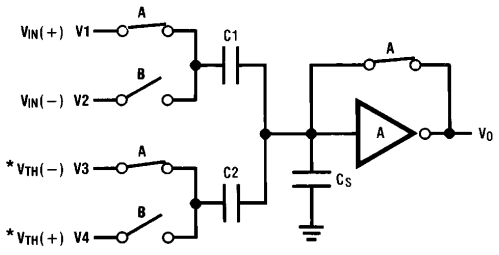
- $V_{B'} - V_B = (V_2 - V_1)\frac{C}{C + C_S}$
- $V_0 = \frac{-A}{C + C_S}[CV_2 - CV_1]$
- V_0 is dependent on $V_2 - V_1$

FIGURE 4b. Compare Phase



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$$V_0 = \frac{-A}{C_1 + C_2 + C_S}[C_1 (V_2 - V_1) + C_2 (V_4 - V_3)]$$

$$= \frac{-A}{C_1 + C_2 + C_S}[\Delta Q C_1 + \Delta Q C_2]$$

* Comparator Reads V_{TH} from Internal DAC Differentially

FIGURE 4c. Multiple Differential Inputs

Functional Description (Continued)

In actual practice, the devices used in the ADC0852/4 are a simple but important expansion of the basic comparator described above. As shown in *Figure 4c*, multiple differential comparisons can be made. In this circuit, the feedback switch and one input switch on each capacitor (A switches) are closed in the first cycle. Then the other input on each capacitor is connected while all of the first switches are opened. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor (C1, C2), will now depend on both input signal differences.

1.2 Input Sampling and Response Time

The input phases of the comparator relate to the device clock (CLK) as shown in *Figure 5*. Because the comparator is a sampling device, its response characteristics are somewhat different from those of linear comparators. The $V_{IN}(+)$ input is sampled first (CLK high) followed by $V_{IN}(-)$ (CLK low). The output responds to those inputs, one half cycle later, on CLK's falling edge.

The comparator's response time to an input step is dependent on the step's phase relation to the CLK signal. If an input step occurs too late to influence the most imminent comparator decision, one more CLK cycle will pass before the output is correct. In effect, the response time for the $V_{IN}(+)$ input has a minimum of 1 CLK cycle + 1 μS and a maximum of 2 CLK cycles + 1 μS. The $V_{IN}(-)$ input's delay will range from 1/2 CLK cycle + 1 μS to 1.5 CLK cycles + 1 μS since it is sampled after $V_{IN}(+)$.

The sampled inputs also affect the device's response to pulsed signals. As shown in the shaded areas in *Figure 5*, pulses that rise and/or fall near the latter part of a CLK half-cycle may be ignored.

1.3 Input Multiplexer

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential operation. The analog signal conditioning required in transducer-input and other types of data acquisition systems is significantly simplified with this type of input flexibility. One device package can now handle ground referenced inputs as well as signals with some arbitrary reference voltage.

On the ADC0854, the "common" pin (pin 6) is used as the "−" input for all channels in single-ended mode. Since this input need not be at analog ground, it can be used as the common line for pseudo-differential operation. It may be tied to a reference potential that is common to all inputs and within the input range of the comparator. This feature is especially useful in single-supply applications where the analog circuitry is biased to a potential other than ground.

A particular input configuration is assigned during the MUX addressing sequence which occurs prior to the start of a comparison. The MUX address selects which of the analog channels is to be enabled, what the input mode will be, and the input channel polarity. One limitation is that differential inputs are restricted to adjacent channel pairs. For example, channel 0 and 1 may be selected as a differential pair but they cannot act differentially with any other channel.

The channel and polarity selection is done serially via the DI input. A complete listing of the input configurations and corresponding MUX addresses for the ADC0852 and ADC0854 is shown in tables I and II. *Figure 6* illustrates the analog connections for the various input options.

The analog input voltage for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading accuracy.

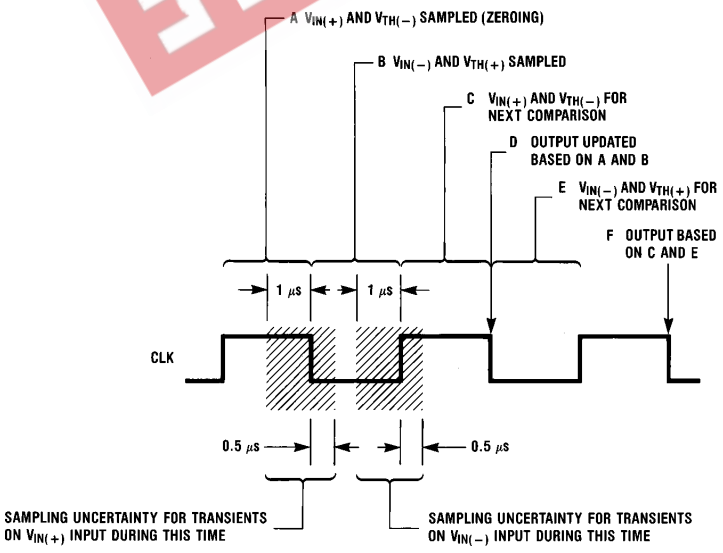

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FIGURE 5. Analog Input Timing

Functional Description (Continued)

TABLE I. MUX Addressing: ADC0854
Single-Ended MUX Mode

MUX Address			Channel				
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT	0	1	2	3	COM
1	0	0	+				−
1	0	1			+		−
1	1	0		+			−
1	1	1				+	−

Differential MUX Mode

MUX Address			Channel			
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE II. MUX Addressing: ADC0852
Single Ended MUX Mode

MUX Address		Channel	
SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel	
SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
0	0	+	−
0	1	−	+

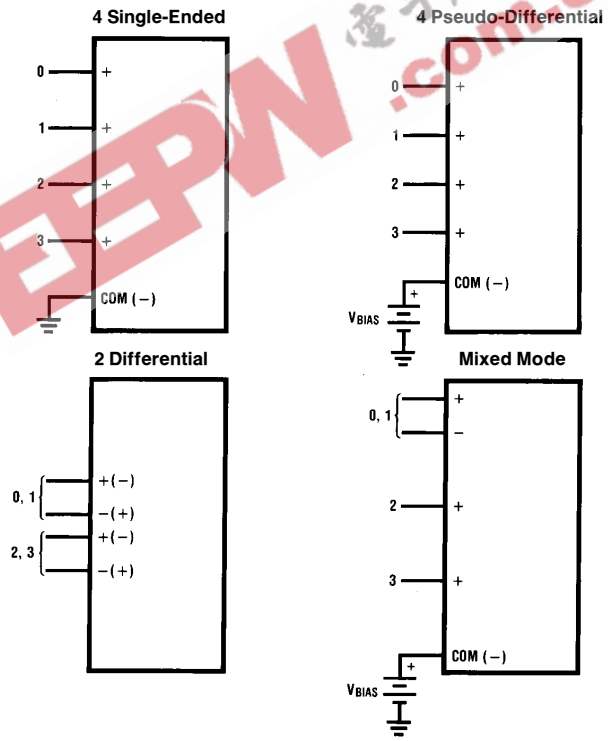

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FIGURE 6. Analog Input Multiplexer Options for the ADC0854

Functional Description (Continued)

2.0 THE DIGITAL INTERFACE

An important characteristic of the ADC0852 and ADC0854 is their serial data link with the controlling processor. A serial communication format eliminates the transmission of low level analog signals by locating the comparator close to the signal source. Thus only highly noise immune digital signals need to be transmitted back to the host processor.

To understand the operation of these devices it is best to refer to the timing diagrams (*Figure 3*) and functional block diagram (*Figure 2*) while following a complete comparison sequence.

1. A comparison is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire addressing sequence and comparison. The comparator then waits for a start bit, its MUX assignment word, and an 8-bit code to set the internal DAC which supplies the comparator's threshold voltage (V_{TH}).

2. An external clock is applied to the CLK input. This clock can be applied continuously and need not be gated on and off.

3. On each rising edge of the clock, the level present on the DI line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line. All leading zeroes are ignored. After the start bit, the ADC0852 expects the next 2 bits to be the MUX assignment word while the ADC0854, with more MUX configurations, looks for 3 bits.

4. Immediately after the MUX assignment word has been clocked in, the shift register then reads the next eight bits as the input code to the internal DAC. This eight bit word is read LSB first and is used to set the voltage applied to the comparator's threshold input (internal).

5. After the rising edge of the 11th or 12th clock (ADC0852 or ADC0854 respectively) following the start bit, the comparator and DAC programming is complete. At this point the DI line is disabled and ignores further inputs. Also at this time the data out (DO) line comes out of TRI-STATE and enters a don't care state (undefined output) for 1.5 clock cycles.

6. The result of the comparison between the programmed threshold voltage and the difference between the two selected inputs ($V_{IN}(+) - V_{IN}(-)$) is output to the DO line on each subsequent high to low clock transition.

7. After programming, continuous comparison on the same selected channel with the same programmed threshold can be done indefinitely, without reprogramming the device, as long as $\overline{CS}$ remains low. Each new comparator decision will be shifted to the output on the falling edge of the clock. However, the output will, in effect, "lag" the analog input by 0.5 to 1.5 clock cycles because of the time required to make the comparison and latch the output (see *Figure 5*).

8. All internal registers are cleared when the $\overline{CS}$ line is brought high. If another comparison is desired $\overline{CS}$ must make a high to low transition followed by new address and threshold programming.

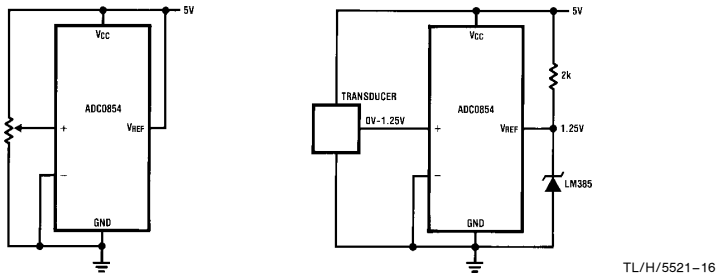
3.0 REFERENCE CONSIDERATIONS / RATIOMETRIC OPERATION

The voltage applied to the "V_{REF}" input of the DAC defines the voltage span that can be programmed to appear at the threshold input of the comparator. The ADC0854 can be used in either ratiometric applications or in systems with absolute references. The V_{REF} pin must be connected to a source capable of driving the DAC ladder resistance (typ. 2.4 kΩ) with a stable voltage.

In ratiometric systems, the analog input voltage is normally a proportion of the DAC's or A/D's reference voltage. For example, a mechanical position servo using a potentiometer to indicate rotation, could use the same voltage to drive the reference as well as the potentiometer. Changes in the value of V_{REF} would not affect system accuracy since only the relative value of these signals to each other is important. This technique relaxes the stability requirements of the system reference since the analog input and DAC reference move together, thus maintaining the same comparator output for a given input condition.

In the absolute case, the V_{REF} input can be driven with a stable voltage source whose output is insensitive to time and temperature changes. The LM385 and LM336 are good low current devices for this purpose.

The maximum value of V_{REF} is limited to the V_{CC} supply voltage. The minimum value can be quite small (see typical performance curves) allowing the effective resolution of the comparator threshold DAC to also be small ($V_{REF} = 0.5V$, DAC resolution = 2.0 mV). This in turn lets the designer have finer control over the comparator trip point. In such instances however, more care must be taken with regard to noise pickup, grounding, and system error sources.



a) Ratiometric **b) Absolute with a Reduced Span**

FIGURE 7. Referencing Examples

Functional Description (Continued)

4.0 ANALOG INPUTS

4. 1 Differential Inputs

The serial interface of the ADC0852 and ADC0854 allows them to be located right at the analog signal source and to communicate with a controlling processor via a few fairly noise immune digital lines. This feature in itself greatly reduces the analog front end circuitry often needed to maintain signal integrity. Nevertheless, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common mode voltage.

The differential input of the comparator actually reduces the effect of common-mode input noise, i.e. signals common to both selected "+" and "−" inputs such as 60 Hz line noise. The time interval between sampling the "+" input and then the "−" input is ½ of a clock period (see *Figure 5).*

The change in the common-mode voltage during this short time interval can cause comparator errors. For a sinusoidal common-mode signal this error is:

V_{ERROR} (MAX) = V_{PEAK} (2π f_{CM}/2 f_{CLK})

where f_{CM} is the frequency of the common-mode signal, V_{peak} is its peak voltage value, and f_{CLK} is the DAC clock frequency.

For example, 1 V_{PP} 60 Hz noise superimposed on both sides of a differential input signal would cause an error (referred to the input) of 0.75 mV. This amounts to less than 1/25 of an LSB referred to the threshold DAC, (assuming V_{REF} = 5V and f_{CLK} = 250 kHz).

4. 2 Input Currents and Filtering

Due to the sampling nature of the analog inputs, short spikes of current enter the "+" input and leave the "−" at the clock edges during a comparison. These currents decay rapidly and do not cause errors as the comparator is strobed at the end of the clock period (see *Figure 5*).

The source resistance of the analog input is important with regard to the DC leakage currents of the input multiplexer. The worst-case leakage currents of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op-amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance source be required.

4. 3 Arbitrary Analog Input/Reference Range

The total span of the DAC output and hence the comparator's threshold voltage is determined by the DAC reference. For example, if V_{REF} is set to 1 volt then the comparator's threshold can be programmed over a 0 to 1 volt range with 8 bits of resolution. From the analog input's point of view, this span can also be shifted by applying an offset potential to one of the comparator's selected analog input lines (usually "−"). This gives the designer greater control of the ADC0852/4's input range and resolution and can help simplify or eliminate expensive signal conditioning electronics.

An example of this capability is shown in the "Load Cell Limit Comparator" of *Figure 15*. In this circuit, the ADC0852 allows the load-cell signal conditioning to be done with only one dual op-amp and without complex, multiple resistor matching.

5.0 POWER SUPPLY

A unique feature of the ADC0854 is the inclusion of a 7 volt zener diode connected from the "V+" terminal to ground (*Figures 2* and *8*) "V+" also connects to "V_{CC}" via a silicon diode. The zener is intended for use as a shunt voltage regulator to eliminate the need for additional regulating components. This is especially useful if the ADC0854 is to be remotely located from the system power source.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 10* and *11*. Here this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the comparator clock. The low device current requirements and the relatively high clock frequencies used (10 kHz–400 kHz) allows use of the small value filter capacitor shown. The shunt zener regulator can also be used in this mode however this requires a clock voltage swing in excess of 7 volts. Current limiting for the zener is also needed, either built into the clock generator or through a resistor connected from the clock to V+.

Typical Applications

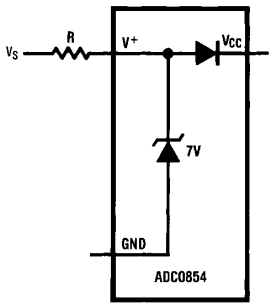


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FIGURE 8. An On-Chip Shunt Regulator Diode

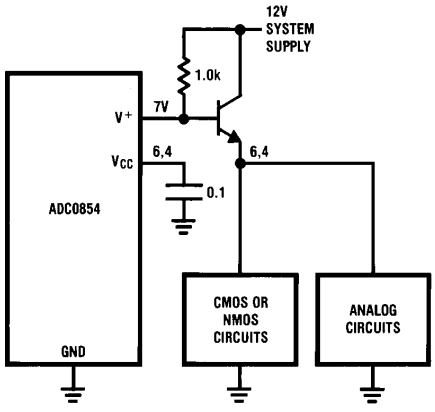

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FIGURE 9. Using the ADC0854 as the System Supply Regulator

Typical Applications (Continued)

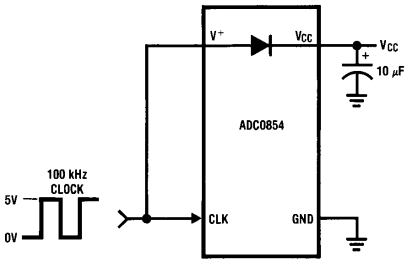

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FIGURE 10. Generating V_{CC} from the Comparator Clock

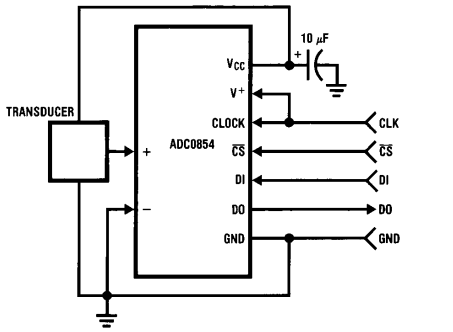

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FIGURE 11. Remote Sensing—Clock and Power on One Wire

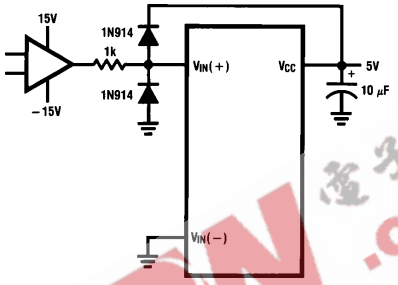

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FIGURE 12. Protecting the Analog Input

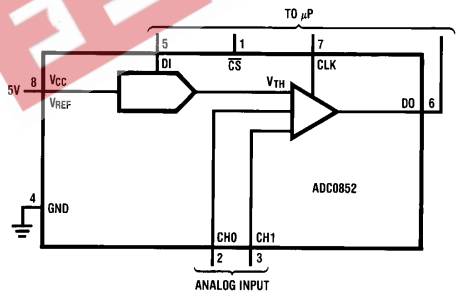

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FIGURE 13. One Component Window Comparator

Requires no additional parts. Window comparisons can be accomplished by inputting the upper and lower window limits into DI on successive comparisons and observing the two outputs:

Two high outputs ⟶ input > window

Two low outputs ⟶ input < window

One low and one high ⟶ input is within window

Typical Applications (Continued)

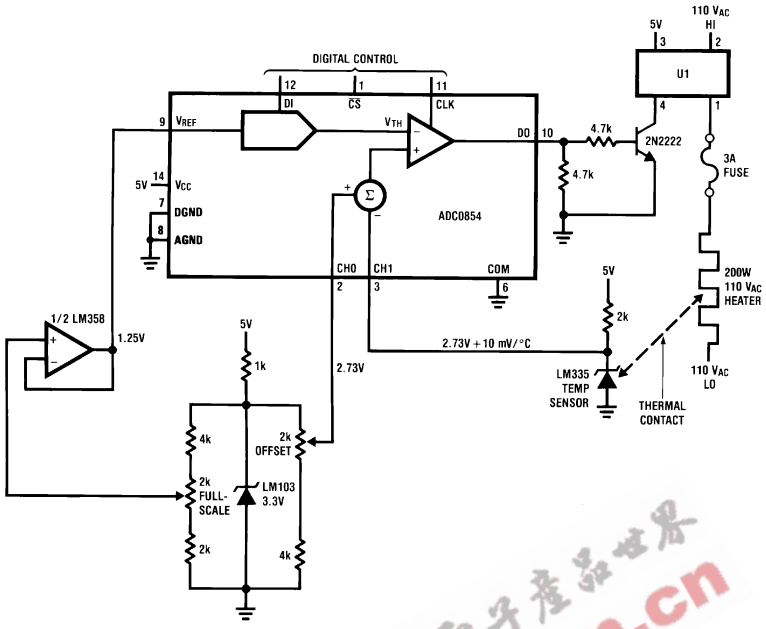

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FIGURE 14. Serial Input Temperature Controller

Note 1: ADC0854 does not require constant service from computer. Self controlled after one write to DI if CS remains low.

Note 2: U_1: Solid State Relay, Potter Brumfield #EOM1DB22

Note 3: Set Temp via. DI. Range: 0 to 125°C

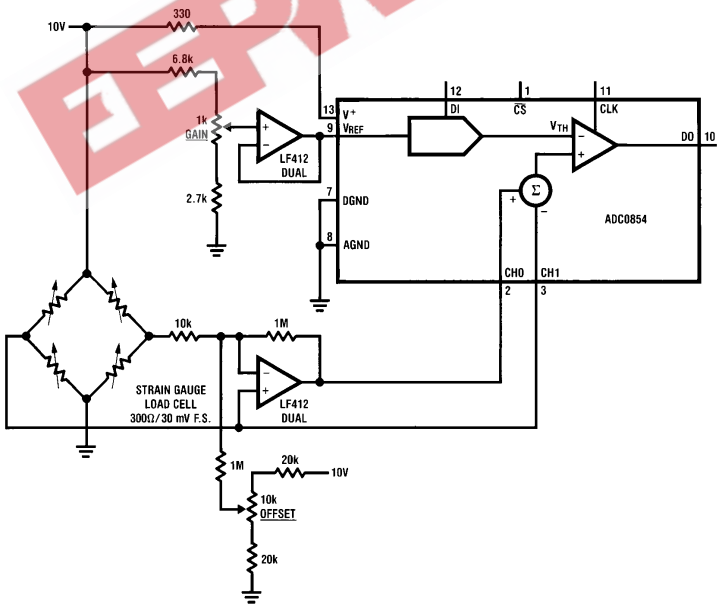

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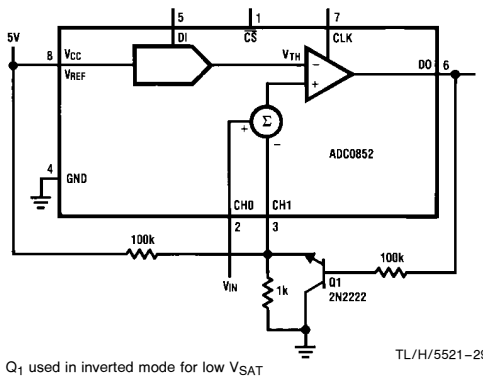
FIGURE 15. Load Cell Limit Comparator

- Differential Input elliminates need for instrumentation amplifier
- A total of 4 load cells can be monitored by ADC0854

Typical Applications (Continued)



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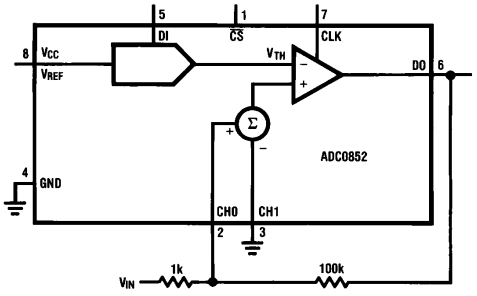
* Q_1 used in inverted mode for low V_{SAT}



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Hysteresis band = 50 mV

FIGURE 16. Adding Comparator Hysteresis

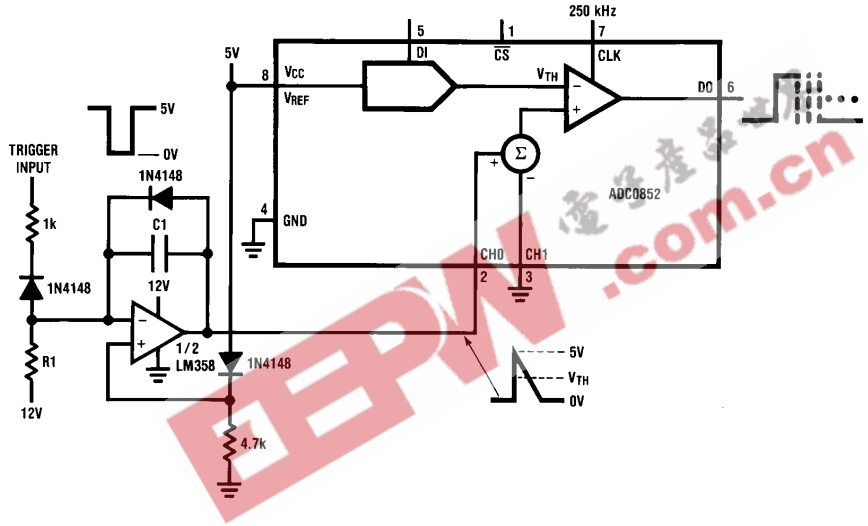

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FIGURE 17. Pulse-Width Modulator

- Range of pulse-widths controlled via R_1, C_1

Typical Applications (Continued)

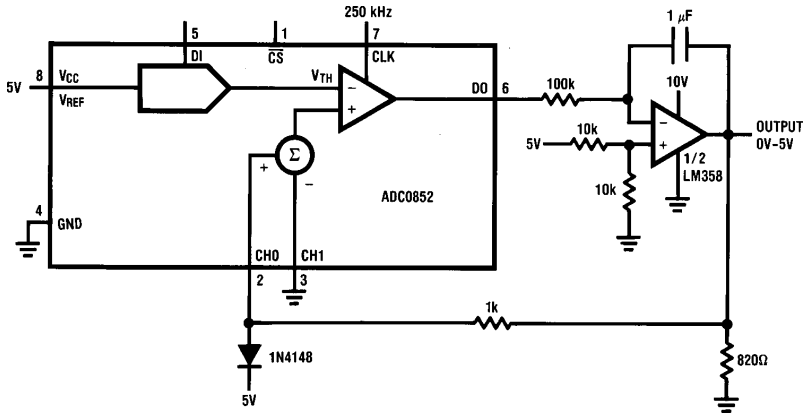

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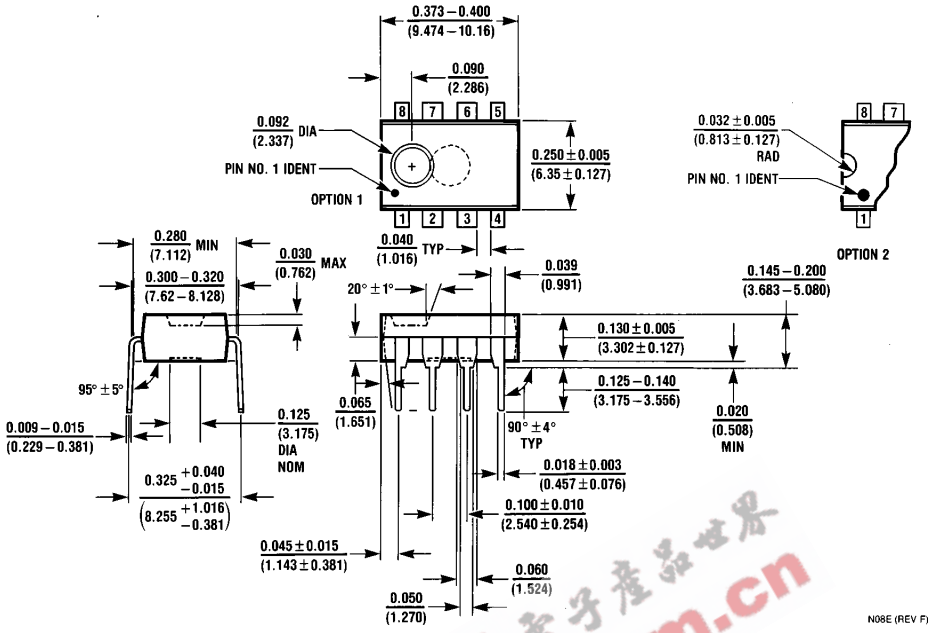
FIGURE 18. Serial Input 8-Bit DAC

Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0852CCN	2	±1	N08E	0°C to 70°C
ADC0854CCN	4	±1	N14A	0°C to 70°C

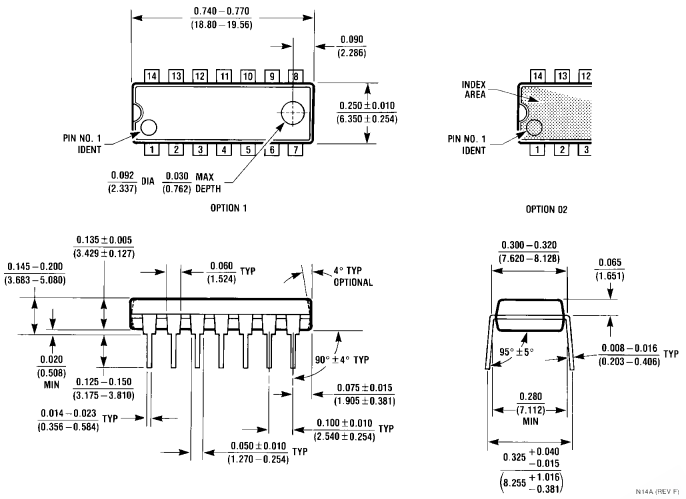

EEPW
.com.cn

Physical Dimensions inches (millimeters)



Dual-In-Line Package
Order Number ADC0852CCN
NS Package Number N08E

Physical Dimensions inches (millimeters) (Continued)



Dual-In-Line Package
Order Number ADC0854CCN
NS Package Number N14A

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