FINAL

Am4701 BiFIFO

Dual 512 x 8 Bidirectional Parity Generator/Checker, Bypass Mode, Programmable AE/AF Flags

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Two 512 x 8 FIFO buffers
- Full and Empty Flags
- Built in parity checker/generator
- Programmable Interrupt request
- Generates and detects framing bit
- Low power consumption
- Bidirectional full duplex communication
- Programmable Almost-Full and Almost-Empty flags
- Bypass mode—Changes the Am4701 to a transceiver
- Bidirectional mailbox communication
- Byte detect on read

GENERAL DESCRIPTION

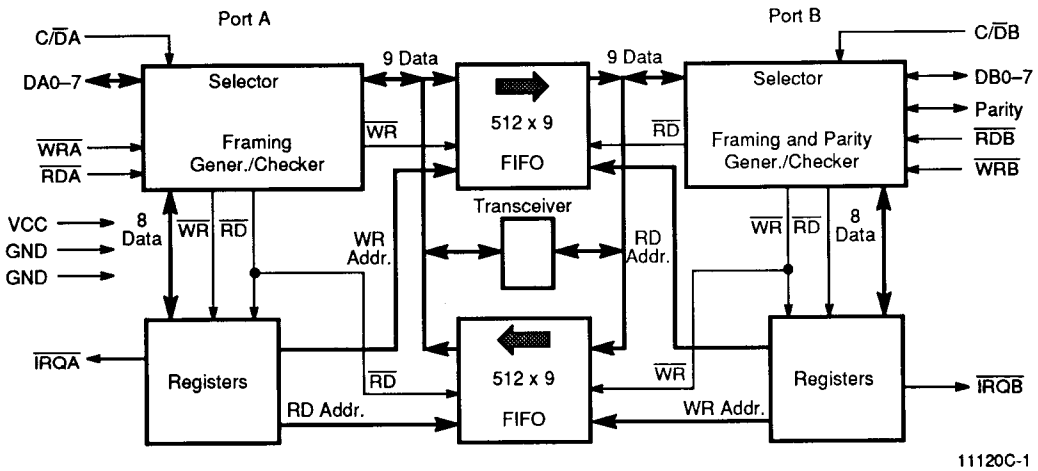
The Am4701 is a CMOS RAM-based, fully asynchronous, byte-wide bidirectional First In First Out (FIFO) device that is 512 words deep with 8-bit wide words in each direction. It contains two 512x9 FIFOs with the ninth bit in each array used for framing and parity functions.

The Am4701 can accept and output data asynchronously and simultaneously at data rates from 0 to 22.2 MHz for standard commercial temperature range products. Interrupt driven status flags are provided to signify Full, Empty and user programmable Almost Full and Almost Empty condition. Parity generation/checking, programmable interrupt requests, byte-detection, framing and port-to port communication through mail boxes are provided on chip. The Am4701 can also operate in Bypass Mode where it behaves like a transceiver.

The Am4701 is ideally suited for bidirectional interprocessor communication and data-buffering between a CPU and a peripheral device. The ability to buffer large transfers of data and its rate adaption capabilities make the Am4701 useful in communication, image processing, DSP and printing systems.

BLOCK DIAGRAM

2-512 x 9 BIFIFO



11120C-1

Publication# 11120 Rev. C Amendment/0
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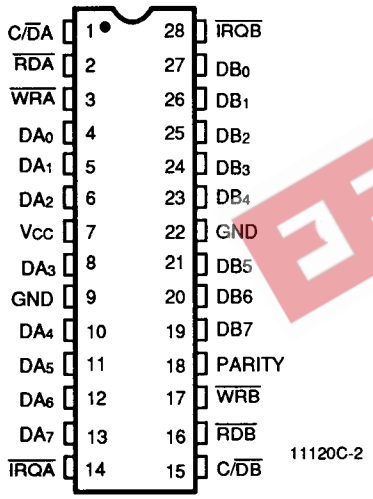
PRODUCT SELECTOR GUIDE

Part Number	Am4701-35	Am4701-45
Access Time	35 ns	45 ns
Maximum Power Supply	120 mA	100 mA
Operating Frequency	22.2 MHz	16.7 MHz
Operating Range	Com'l	Com'l

CONNECTION DIAGRAMS

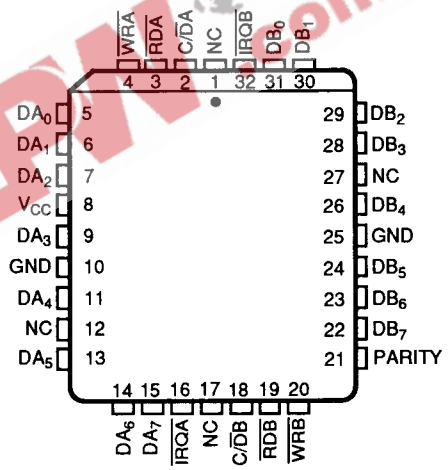
Top View

DIP



11120C-2

PLCC

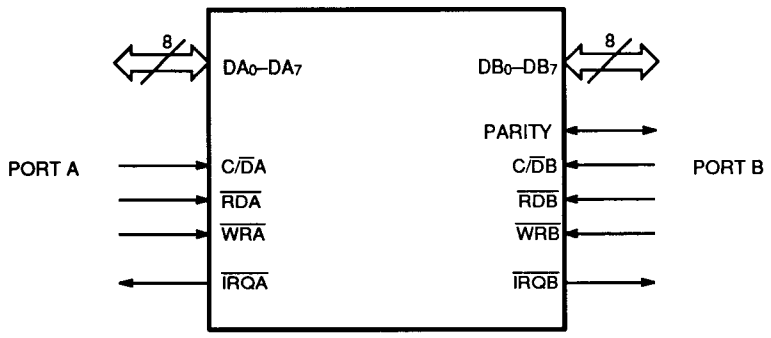


11120C-3

Notes:

Pin 1 is marked for orientation for plastic packages.
NC = No Connection.

LOGIC SYMBOL



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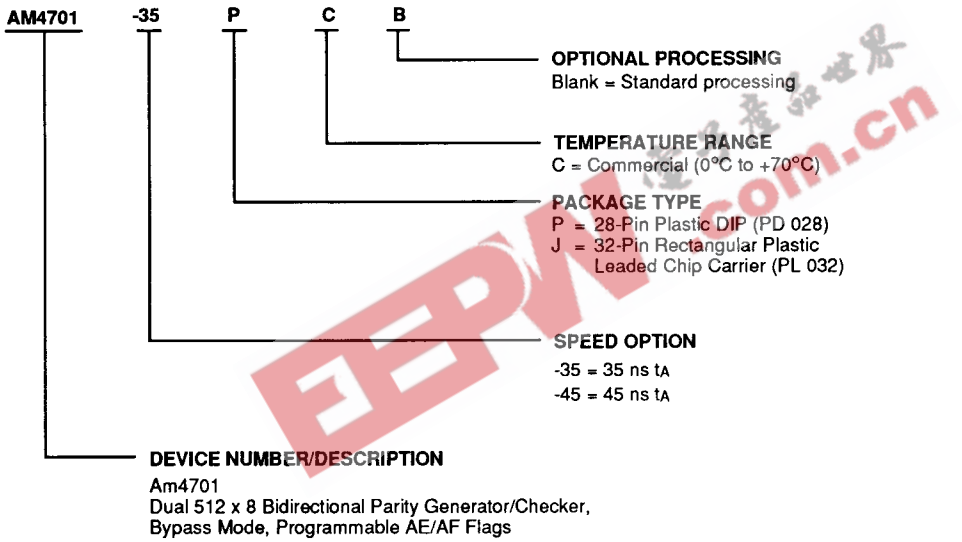
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM4701-35	PC, JC
AM4701-45	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

DA_7–DA_0, DB_7–DB_0

8-bit bidirectional data bus for port A,B.

PARITY

Bidirectional parity/framing bit (Port B only)

$\overline{RDA}$, $\overline{RDB}$

Read input for port A or B. The falling edge of Read initiates a read from the FIFO or the internal registers. Both ports can be read simultaneously by $\overline{RDA}$ and $\overline{RDB}$.

$\overline{WRA}$, $\overline{WRB}$

Write input to port A or B. The falling edge of Write initiates a write cycle. Data must be valid t_{DW} prior to $\overline{WR}$ rising, and held valid throughout the write cycle. Both ports can write simultaneously by $\overline{WRA}$ and $\overline{WRB}$.

C/$\overline{D}$

Command/Data selection for port A or B.
C/$\overline{D}$ = High: Read or Write to the internal registers.
C/$\overline{D}$ = Low: Read or Write to the FIFO.

$\overline{IRQA}$, $\overline{IRQB}$

Interrupt request output of port A, B. The $\overline{IRQ}$ flag will be active low by any changes of status in the appropriate port and is reset by reading the status register of the same port. Each port's $\overline{IRQ}$ flag can be masked by its mask register.

V_{CC}

Power Supply Pin, Input, +5 Volts

GND

Ground Supply Pin, Input, 0 Volts

FUNCTIONAL DESCRIPTION

The Am4701 BiFIFO consists of two 512 x 8 FIFOs connected to provide bidirectional FIFO action between two data ports, A and B. One FIFO provides buffering in the direction from A to B; the other FIFO provides buffering from B to A. The Am4701 also provides a set of application specific support logic to support communication between microprocessors and peripheral devices. This logic includes the following functions:

- Optional FIFO bypass for direct data transfer
- 9th bit for framing bit generation and detect
- Optional parity generate and detect on Port B
- Optional parity error insertion as framing bit
- Byte detect
- Mailbox registers
- Programmable Almost Empty and Almost Full flags
- Read and write pointer reset
- Interrupt on flag assertion

Operation of the Am4701 BiFIFO is controlled by two sets of registers, one for each port. Command registers in each set determine the operating mode for each port, and Status registers in each set indicate the status of chip operations. The remaining registers in each set provide data to support status bit generation. Though the registers will be reset to the default state during power up, it is recommended to always use the master reset to ensure proper operation. An interrupt pin is provided for each port. This pin can be activated by bits in its associated Status register and allow external hardware detection of a change in the status of the BiFIFO.

There are a variety of applications of the Am4701 BiFIFO. The bidirectional FIFO buffering feature simplifies CPU to CPU communication. The parity logic on Port B allows convenient communication between a CPU and a bus which requires parity generation and detection. The direct connect transceiver function provides efficient communication of command and status data between a CPU and a peripheral chip such as a disk controller while the FIFO function provides efficient buffering of its high speed data.

Read/Write Operations

Am4701 read and write operations are controlled by $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ control lines for each port. $\overline{RD}$ gates BiFIFO data to the bus, and the rising edge of the WR signal latches data from the bus into registers or a FIFO in the Am4701.

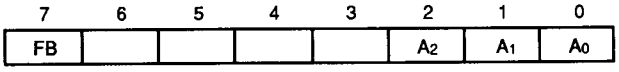
The C/$\overline{D}$ input selects the source or destination of the data. When C/$\overline{D}$ is low, data is written into or read from the appropriate FIFO for that port, with one exception: when Port A is in the Bypass mode, data will be transferred directly between Port A and Port B, bypassing the FIFOs. When C/$\overline{D}$ is high, data is written to or read from one of the registers in the port register set.

The register set for the Am4701 is shown in Table 1. All registers are read or written in a two cycle operation. The first cycle loads a Pointer register to select the register to be read, and the second cycle performs the read or write data transfer to the selected register. The Pointer register is cleared to zero by the data transfer cycle. Because the Pointer register is cleared to zero, the Status register may also be read directly in a single cycle. This is because the zero select code corresponds to the Status register. The Status register is therefore always selected and available to be read unless the Pointer register has been set to another value.

Table 1. Register Address Assignments

Reg Addrs	Write	Read
0	Pointer	Status
1	Command	Command
2	Mask	Mask
3	Byte Detect	Byte Detect
4	Outbound Mailbox	Outbound Mailbox
5	AE/AF	AE/AF
6	Reset Read Pointer	Inbound Mailbox
7	Reset Write Pointer	

Pointer Register

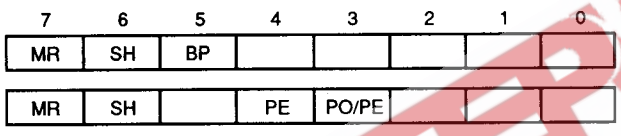


11120C-5

The Pointer register contents select which register in the register set is to be read or written, as shown in Table 1. The Pointer register is a write-only register. All register accesses are performed in two consecutive cycles: register select cycle and register data transfer cycle. The Pointer register is set by the register select cycle, and it is reset to zero by the completion of the data transfer cycle. The format of the Pointer register is as follows.

Bit	Name	Function
FB	Framing Bit	Writes a framing bit into the FIFO. This bit is set by writing it twice to the Pointer register. An 80 (hex) code is written to select the Pointer register and an 80 code is written to the Pointer register during the transfer cycle.
A2–A0	Reg Select	Selects a register for read or write transfer per Table 1.

Command Register

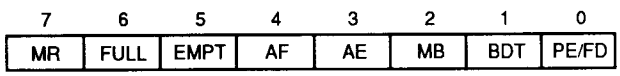


11120C-6

The Command register sets the operating mode for each port. The Command register format for Port A and Port B are different. Port A can be put into Bypass mode, and Port B can enable its parity generate/detect logic as well as determine its polarity. The format of the command registers is as follows.

Bit	Name	Function
MR	Master Reset	Software master reset. Resets both FIFOs and the register sets on both ports. Either port can set the master reset bit. The MR bit in the command register must be written twice consecutively and the status register of the same port must be read to complete a master reset operation. This prevents accidental resets. Setting the MR in the command register sets the MR bit in both status registers.
SH	Shift	Selects the FULL, EMPTY, AE and AF flags from the other port for display in the Status register. This allows displaying current status of the other port.
BP	Bypass	Bypass mode select (Port A only). See Bypass mode section.
PE	Parity Enable	Parity generate and check enable. (Port B only.) When this bit is set, the parity logic on Port B generates and checks bus parity at the Port B I/O inputs. See Parity Generate and Check section.
PO/PE	Odd/Even	Parity Odd or Even select. PO/PE = 1 for odd parity, PO/PE = 0 for even.

Status Register



11120C-7

The Status register indicates the status of various conditions on its associated port. The bits in the status register will be set automatically when those conditions occur and will activate the $\overline{IRQ}$ pin for the appropriate port. Reading the Status register will clear the PE/FD, MR, and the BDT bits. The mailbox bit is cleared by reading the Inbound Mailbox register. FULL, EMPTY, AF, and AE are cleared by reading the status register provided the condition making the bit go true ceased to exist. If the condition causing the bit to be set is still prevalent, then reading the status counter makes these bit "dynamic" and reflect the real condition of the FIFO until the FIFO exits and re-enters that condition. Then, the $\overline{IRQ}$ signal and the appropriate bit will be asserted again. Note that when the Shift bit in the Command register is a one, the Status register will display the FULL, EMPTY, AF, and AE flags for the other port. The format of the Status register is as follows.

Bit	Name	Function
MR	Master Reset	Set when either port has issued a master reset. The MR bit will be cleared by reading the status register.
FULL	Full	Outbound FIFO is full. Write command will be ignored as long as the FIFO is full. The flag is cleared by reading the status register and reading the FIFO in either order (see explanation above). The flag is also cleared by MR.
EMPT	Empty	Inbound FIFO is empty. Read command will be ignored as long as the FIFO is empty. The flag is cleared by reading the status register and writing to the FIFO in either order (see explanation above). The flag is also cleared by MR.
AF	Almost Full	Outbound FIFO is almost full. Set when the FIFO reaches or exceeds the depth limit programmed into the AE/AF register. Cleared by reading the status register and making the FIFO go below the depth limit (see explanation above). The flag is also cleared by MR.
AE	Almost Empty	Inbound FIFO is almost empty. Set when the FIFO reaches or is under the depth limit programmed into the AE/AF register. Cleared by reading the status register and making the FIFO go above the depth limit (see explanation above). The flag is also cleared by MR.
MB	Mailbox	The Inboard Mailbox register has been written into by the other port. Cleared by reading the Inbound Mailbox register or by MR.
BDT	Byte Detect	Set when the data at the output of the inbound FIFO matches the data in the Byte Detect register. Cleared by reading Status register or MR.
PE/FD	Parity Error/ Frame Detect	Set by the 9th bit of the inbound FIFO. Indicates a framing bit or Frame Detect parity error was inserted into the FIFO by the other port. Cleared by reading Status register or MR.

Mask Register

7	6	5	4	3	2	1	0
	FULL	EMPT	AF	AE	MB	BDT	PE/FD

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The Mask register masks the bits of the Status register which will generate the interrupt request, $\overline{IRQ}$. The bits are set in the Status register by the appropriate conditions but do not trigger the $\overline{IRQ}$ signal if masked out. A one in the Mask register enables interrupt by the corresponding bit in the Status register; a zero in the Mask register disables it. The MR bit of the Status register is unmaskable and will always cause an interrupt when set. The bit definitions for the Mask register are the same as for the Status register.

Byte Detect Register

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

11120C-9

The Byte Detect register contains a programmable byte to be detected while reading the FIFO. When the data being read from the FIFO matches the contents of the Byte Detect register, the BDT flag in the Status register is set.

AE/AF Register

7	6	5	4	3	2	1	0
AF_3	AF_2	AF_1	AF_0	AE_3	AE_2	AE_1	AE_0

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The contents of the AE/AF register defines the limits for the Almost Empty and Almost Full flags. Limit programming is done in increments of 16. A code of 0 (hex) for either limit corresponds to 16 for the Almost Empty flag and (512–16) for the Almost full flag. A code of F for either limit corresponds to 256 for the Almost empty flag and (512–256) for the Almost Full flag. Master reset sets this register to 00 (hex code).

Bit	Name	Function
AF_{3-0}	Almost Full	Almost Full limit code: 0000 = 16, 0001 = 32, etc. 1111 = 256.
AE_{3-0}	Almost Empty	Almost Empty limit code: 0000 = (512–16), 0001 = (512–32), etc.

Outbound Mailbox Register

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

11120C-11

Each port has an 8-bit mailbox where it can receive messages from the other port. The mailbox for a given port is called the Inbound Mailbox. The mailbox for the other port is called the outbound Mailbox. The Outbound Mailbox register is the mailbox register for the other port. This register is written into when a message is to be sent to the other port. Writing to this register will cause the MB bit to be set in the Status register of the other port and will cause a mailbox interrupt on that port if enabled by its Mask register.

The Outbound Mailbox register can be read as well as written. The contents of the Outbound Mailbox register will be cleared to zero and zeros will be read back when the other port reads its Inbound Mailbox register. This can be used to determine whether the other port has received the message.

Inbound Mailbox Register

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

11120C-12

The Inbound Mailbox register receives 8-bit messages from the other port. The other port sends a message by writing into its Outbound Mailbox register. The message thus written appears in the Inbound Mailbox for this port.

When the mailbox register has been written into, the MB bit is set in the Status register. The MB bit is reset and the mailbox register is cleared to zeros when the Inbound Mailbox register is read.

FIFO Read and Write Pointer Reset

The read pointer for the inbound FIFO and the write pointer for the outbound FIFO can be reset by writing with the appropriate register select code. The operation requires two cycle as for any other register write operation: address latching and a (dummy) write. No data is actually transferred, but the appropriate pointer is reset. Resetting the write pointer allows overwriting a block that may have contained bad data. Resetting the read pointer allows rereading a block.

Resetting the read or write pointers may cause erroneous AF and AE flags. **Only a master reset will cause correct AF and AE flags**. It is recommended that the AF and AE flags be masked by the Mask register when using these pointer reset commands.

Master Reset

The master reset operation resets both FIFOs and the register sets on both ports. Either port can initiate a master reset operation. The MR bit in the command register must be written twice consecutively and the status register of the same port must be read to complete a master reset operation. This prevents accidental resets. Setting the MR in the command register sets the MR bit in both status registers. A master reset sequence is outlined below:

Port 1	Port 2
Port 1 writes a 1 into the MR bit of the command register (a 2-cycle register operation).	
Port 1 writes a 1 into the MR bit of the command register (a 2-cycle register operation) again.	
	Both $\overline{IRQ}$ signals are asserted The MR bits in both status registers are set
	If port 2 reads its status register, its $\overline{IRQ}$ signal will be deasserted. The MR bit in the status register will not be cleared.
Port 1 reads its status register	
	The master reset operation is complete
Port 1 $\overline{IRQ}$ signal is deasserted The MR bit of port 1's status register is cleared.	
	If port 2 has already read its status register, the MR bit will now be cleared.
	If port 2 has not read its status register yet, both $\overline{IRQ}$ and the MR bit will be cleared once port 2 reads it.

After a master reset, the Am4701 will come up in the default state described below.

- Both FIFOs cleared to empty
- Command registers cleared
  - Port A Bypass mode disabled
  - Port B Parity generate and detect disabled
- AE/AF register cleared to zero: i.e., AF and AE flags set to 16
- Mask registers set to Full and Empty flags only enabled
- $\overline{IRQ}$ is deasserted on both ports due to Master Reset (despite Empty condition on both ports)

The registers will typically be reset to the default state by power up; however, this power up reset cannot be guaranteed. Therefore, a Master Reset should always be performed after power up to insure proper operation.

Status Interrupts

If a condition for an interrupt occurs, the corresponding bit in the status register will be automatically set. If that bit is enabled by its corresponding bit in the Mask register, the $\overline{IRQ}$ signal for that port will be asserted. Reading the status register clears the $\overline{IRQ}$ signal and may clear the bit in the Status register as well. One exception is the MB, Mailbox bit which can only be cleared by reading the Inbound Mailbox register.

Status register interrupts are used to signal the CPU on a port that something interesting has happened rather than having to continually poll for activity.

Framing Bit

The FIFOs in the Am4701 are 512 x 9 in organization. Eight data bits communicate with the external port data buses; the ninth bit is used as a framing bit to identify

natural divisions in the data. The Framing bit can be set by writing to the Pointer register with the FB bit set to one.Two write operations are required, one to set the address and one to set the framing bit (like any other register access). Both operations are performed with 1 in the FB location and address 0. This will cause a one to be written to the ninth FIFO bit during the next write into the FIFO. The Framing bit is reset to zero when the word is written into the FIFO.

When the eight bits of data are read from the FIFO, the Framing bit is written into the FB bit of the Status register. If the Framing bit is a one and the corresponding Mask register bit is set, an interrupt will be generated. The Framing bit can thus be used to signal the receiving port that a block of data has been received.

Port B has additional capability for setting the Framing bit. If Port B parity generation and detect is not enabled and if the Parity input pin is high during a Port B FIFO write, the Framing bit will be set. This allows hardware generation of the Framing bit.

Parity

The Am4701 has built-in parity generate and check logic for port B. The parity generate and check logic simplifies interfacing the Am4701 to a bus with byte parity. Parity generation for data being read from the FIFO and written to the bus provides the required bus parity bit along with the eight bits of bus data. Parity check logic for data being read from the bus and written into the FIFO provides the required parity checking on the data received from the bus.

Parity Generate

Port B parity generate and check logic is enabled by a bit in the Port B Command register. A corresponding bit in the Command register defines the parity sense: odd or even. When this logic is enabled, parity is generated for data being read from the FIFO on port B.

Parity Check

When Port B's parity generate and check bit in the command register is set, data coming into the FIFO on port B will be checked for parity. If parity error is detected, port B's $\overline{IRQ}$ and parity error bit will be set. The FIFO will automatically attach an error bit to the word in error and when this word comes out of port A, port A's $\overline{IRQ}$ and parity error bit will be set. This will allow the recipient of the data to recognize the word in error and to act accordingly.

Port A Bypass Mode Data Transfer

The Bypass mode allows Port A to bypass the FIFOs and directly control the Port B data bus. In this mode, the Am4701 functions as a transceiver-similar to a 74LS245. In this mode, data written to Port A will be gated directly onto the Port B data bus. Reading Port A data will read the state of the Port B data bus lines. The truth table for this operation is shown in Table 2.

Bypass mode allows a CPU on Port A to control a peripheral chip such as a disk controller on Port B. The CPU typically requires direct access to the command and status registers of the disk controller chip to set up a disk I/O operation. Once the operation is begun, the FIFOs are used to buffer the high speed disk data. By providing the Bypass mode, the Am4701 allows this communication without requiring external logic.

Also, the Bypass mode allows port A to read from and write into port B's register set. This feature is useful in applications where one port has "intelligent" control and the other port is a "slave" only.

The Bypass mode supports the following operations (see table):

Data transfer from port B to port A (Port A read)

Data transfer from port A to port B (port A write)

Port A access of port A registers

Port A access of port B's registers

Port A access of port B's registers is performed in two cycles just like an ordinary register access with the exception that port A's C/$\overline{D}$ signal is held Low and port B's C/$\overline{D}$ is held High during both register address latching and register data transfer.

Table 2. Bypass Mode Truth Table

Function	$\overline{RDA}$	$\overline{WRA}$	C/$\overline{D}$A	$\overline{RDB}$	$\overline{WRB}$	C/$\overline{D}$B
Writing data from Port A to Port B Bus.	H	L	L	X	X	L
Reading data from Port B to Port A Bus.	L	H	L	X	X	L
Writing data to Port A registers.	H	L	H	X	X	X
Reading data from Port A's reg'rs to Port A.	L	H	H	X	X	X
Writing data from Port A to B registers.	H	L	L	H	L	H
Reading data from B registers to Port A.	L	H	L	L	H	H

Mailbox Operations

Each port has an 8-bit mailbox where it can receive messages from the other port. The mailbox for a given port is called the Inbound Mailbox. The mailbox for the other port is called the outbound Mailbox. The Outbound Mailbox register is the mailbox register for the other port. This register is written into when a message is to be sent to the other port. Writing to this register will cause the MB bit to be set in the Status register of the other port and will cause a mailbox interrupt on that port if enabled by its Mask register.

The Outbound Mailbox register can be read as well as written. The contents of the Outbound Mailbox register will be cleared to zero and zeros will be read back when the other port reads its Inbound Mailbox register. This can be used to determine whether the other port has received the message.

An example of the mailbox passing protocol is given below.

Port 1	Port 2
Port 1 writes a message byte to Port 2 by writing to its Outbound Mailbox register	
	Port 2 $\overline{IRQ}$ signal is asserted and MB bit set
	Port 2 reads its Status register and recognizes the MB bit. The IRQ signal is reset.
	Port 2 reads its Incoming Mailbox. The mailbox register, and the MB bit are reset.
Port 1 reads the message it wrote in its Outbound Mailbox register. If all bits are zero, Port 2 must have read its mail.	
.... Ready for next message	

APPLICATIONS

The Am4701 provides bidirectional buffering of high speed digital data. Its application support logic makes it well suited to providing communication between two CPUs, between a CPU and a bus and between a CPU and a peripheral device.

An example of a simple 8-bit CPU-to-CPU connection is shown in Figure 1. In this case, parity is not used, and a simple, high speed communication path is set up using a single chip.

Figure 2 shows an example of the Am4701 used to provide communication between a CPU and a bus with byte parity. In this case, the parity generation and check logic available on Port B is used to provide the parity generation and checking required by the bus. The Am4701 provides this function without requiring any external logic, representing a savings in chip count, board space and complexity.

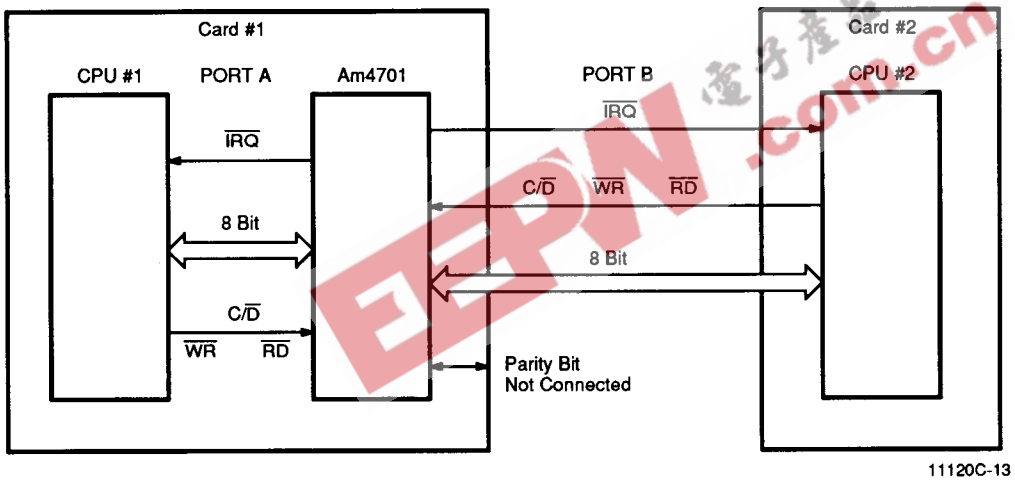


Figure 1. CPU-CPU Communication

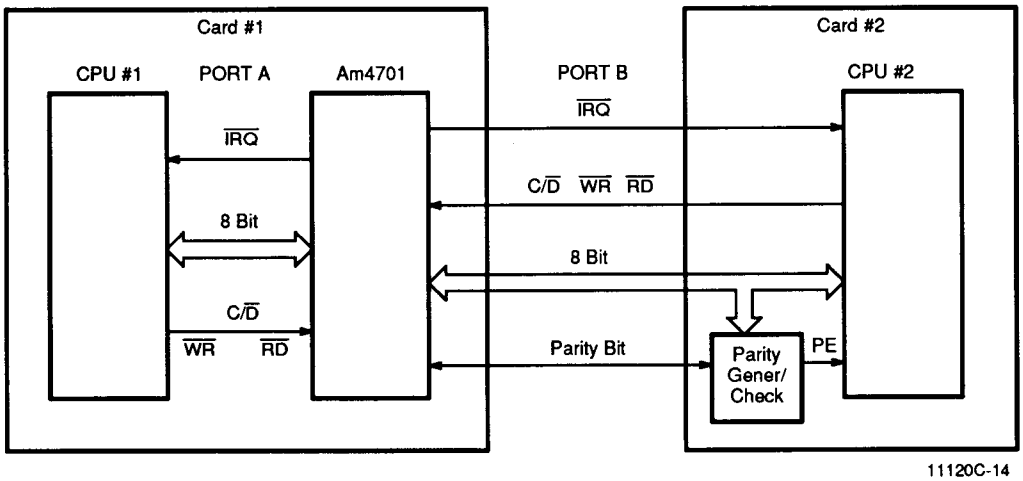


Figure 2. CPU-CPU Communication with Parity

In Figure 3, the Am4701 is used as a single chip interface between a CPU and a peripheral device such as a disk controller chip. The Am4701 provides a number of benefits in this single chip communication design. The Bypass mode allows the CPU to set up both the registers in the peripheral device as well as the Port B register set of the Am4701. The bidirectional FIFO function provides buffering of data at rates up to 16 megabytes/second. Finally, the interrupt function provides direct indication to the CPU of data transfer status of the peripheral device, allows the CPU to set up the most efficient mode of processing by exception, and provides control information to the peripheral interface logic (the PAL) to allow it to sequence the peripheral device in a direct manner.

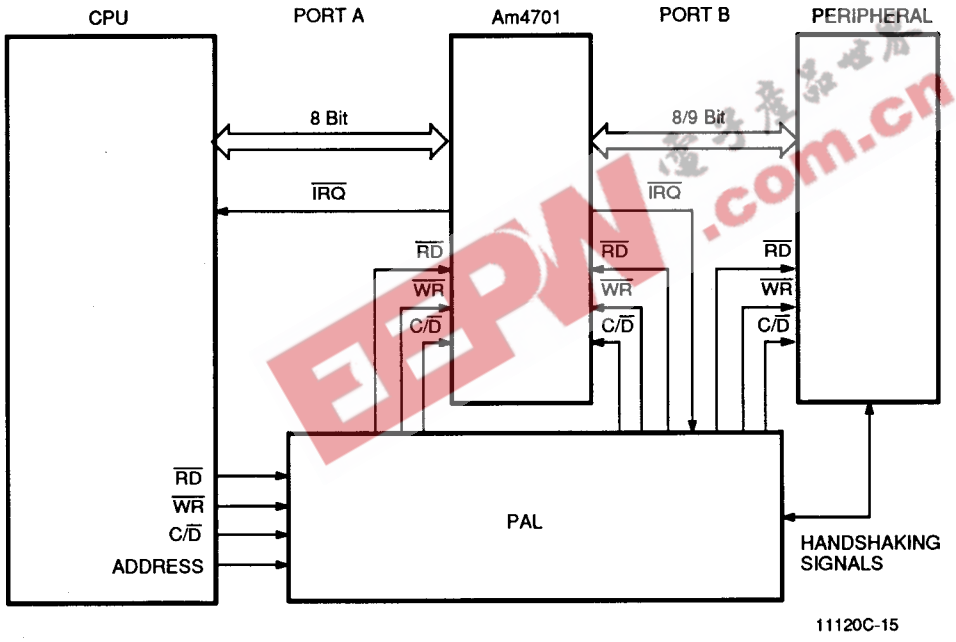


Figure 3. CPU-Peripheral Communication with Bypass

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . –0.5 V to +7.0 V
All Signal Voltages . . . . . –0.5 V to +7.0 V
DC Output Current . . . . . 20 mA
Power Dissipation . . . . . 1.0 W
Operating Temperature . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +155°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Commercial (C) Devices

Supply Voltage . . . . . +4.5 V to +5.5 V
Operating Temperature . . . . . 0°C to +70°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	COM'L Min.	COM'L Max.	Unit
I_{OH}	Output High Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	–2.0		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V, V_{CC} = 4.5 V	+6.0		mA
V_{IH}	Input High Voltage	(Note 1)	2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage	(Note 1)		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = 5.5 V	–10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V	–10	10	µA
I_{CC1}	Static Operating Supply Current	GND ≤ V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V (Note 2)		15	mA
I_{CC2}	Dynamic Operating Current, (16.7 MHz Max.)	GND ≤ V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V (Note 2)		100	mA
I_{CC3}	Dynamic Operating Current, (22.5 MHz Max.)	GND ≤ V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V (Note 2)		120	mA

Notes:

1. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I_{CC} measurements are made with outputs open.

CAPACITANCE (Note 3) (V_{CC} = 5.0 V, T_A = 25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Descriptions	Test Conditions	Typ.	Unit
C_I	Input Capacitance	V_{IN} = 0 V	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0 V	7	

Note:

3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

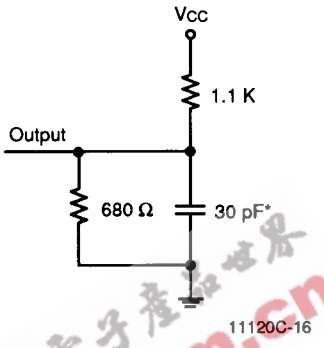
No. (Note 5)	Symbol	Description	COM'L 35 ns		COM'L 45 ns		Unit
			Min.	Max.	Min.	Max.	
Read Cycle Parameters							
1	t_{RC}	Read cycle time	45		60		ns
2	t_{RA}	Read Access time		35		45	ns
3	t_{RAP}	Read Access time with Parity		45		55	ns
4	t_{RPW}	Read Pulse width	35		45		ns
5	t_{RR}	Read Recovery time	10		15		ns
6	t_{OH}	Output Hold after RD	5		5		ns
7	t_{LZ}	RD Low to Output Active	5		5		ns
8	t_{HZ}	RD High to Output Disable		25		30	ns
9	t_{AH}	C/D Hold time after RD or WR	5		5		ns
10	t_{AS}	C/D Setup Time to RD or WR	5		5		ns
11	t_{RCS}	Write End to Begin Read (Note 4)	20		30		ns
Write Cycle Parameters							
12	t_{RCH}	Read End to Begin Write (Note 4)	20		30		ns
13	t_{WC}	Write Cycle Time	45		60		ns
14	t_{WP}	Write Pulse Width	20		45		ns
15	t_{DW}	Data Setup time to WR	20		30		ns
16	t_{DH}	Data Hold Time after WR	0		5		ns
17	t_{WR}	Write Recovery Time	10		15		ns
18	t_{FL}	Fall Through Time	45		60		ns
IRQ and Flag Timing							
21	t_{WLIL1}	Write low to IRQ low (FULL flag)		45		55	ns
21	t_{WLIL2}	Write low to IRQ low (AF flag)		55		75	ns
22	t_{WHIL1}	Write high to IRQ low		35		45	ns
23	t_{RHIH}	Read status high to IRQ high		35		45	ns
24	t_{RLIL1}	Read low to IRQ low (EMPTY flag)		45		55	ns
24	t_{RLIL2}	Read low to IRQ low (AE flag)		55		75	ns
25	t_{RHIL}	Read high to IRQ low		35		45	ns
26	t_{RLIH}	Read low to MB flag reset		35		45	ns
Bypass Timing							
27	t_{FLB}	Flow Through Delay (Bypass)	45		60		ns

Notes:

4. This parameter refers to read/write on the same port.
5. Switching Waveforms Reference numbers.
* Subgroups 7 and 8 apply to functional tests.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output timing reference levels	1.5 V
Output loads	See AC Test Load



* Includes jig and scope capacitances

AC Test Load

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

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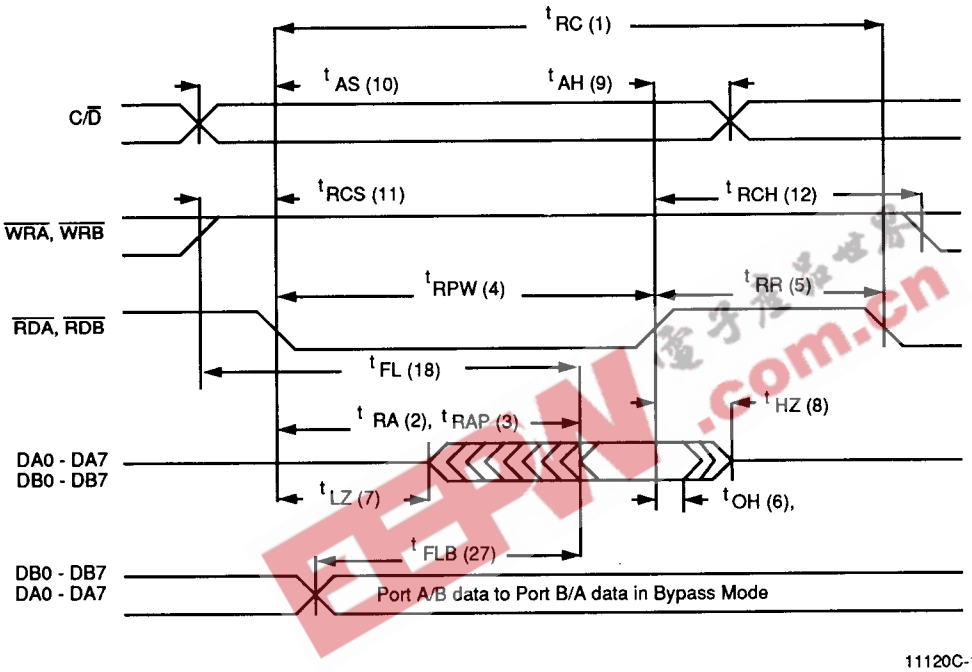
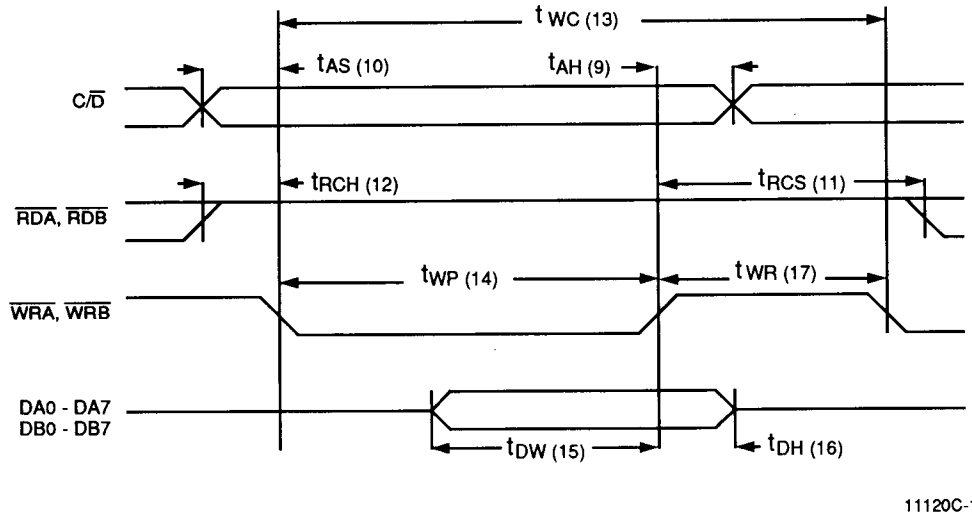
SWITCHING WAVEFORMS



11120C-17

Read Timing



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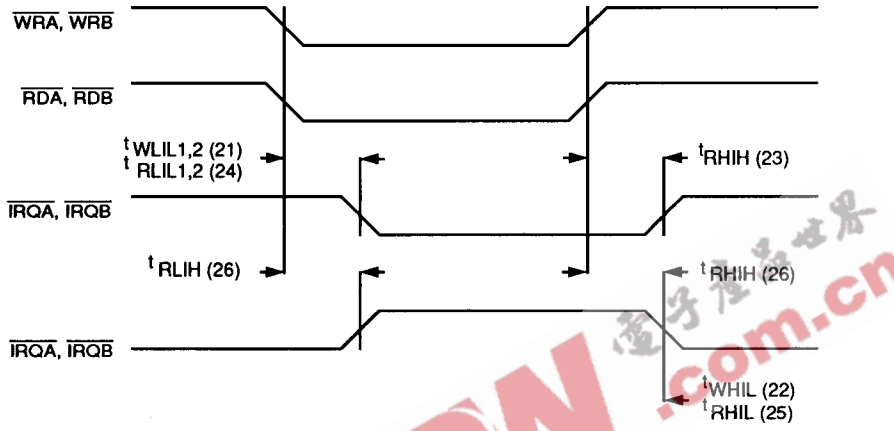
Write Timing

SWITCHING WAVEFORMS



IRQ Timing