

CD54HC299, CD74HC299, CD54HCT299

Data sheet acquired from Harris Semiconductor SCHS178C

January 1998 - Revised May 2003

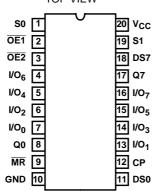
High-Speed CMOS Logic 8-Bit Universal Shift Register; Three-State

Features

- Buffered Inputs
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- · Can be Cascaded for N-Bit Word Lengths
- I/O₀ I/O₇ Bus Drive Capability and Three-State for Bus Oriented Applications
- Typical $f_{MAX} = 50MHz$ at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^{\circ}C$
- Fanout (Over Temperature Range)
 - Standard Outputs......10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
 - CMOS Input Compatibility, $\text{I}_{\text{I}} \leq 1 \mu \text{A}$ at $\text{V}_{\text{OL}}, \, \text{V}_{\text{OH}}$

Pinout

CD54HC299, CD54HCT299 (CERDIP) CD74HC299, CD74HCT299 (PDIP, SOIC) TOP VIEW



Description

The 'HC259 and 'HCT299 are 8-bit shift/storage registers with three-state bus interface capability. The register has four synchronous-operating modes controlled by the two select inputs as shown in the mode select (S0, S1) table. The mode select, the serial data (DS0, DS7) and the parallel data (I/O $_0$ - I/O $_7$) respond only to the low-to-high transition of the clock (CP) pulse. S0, S1 and data inputs must be stable one setup time prior to the clock positive transition.

The Master Reset (\overline{MR}) is an asynchronous active low input. When \overline{MR} output is low, the register is cleared regardless of the status of all other inputs. The register can be expanded by cascading same units by tying the serial output (Q0) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DS0) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DS0 of the first stage.

The three-state input/output I(/O) port has three modes of operation:

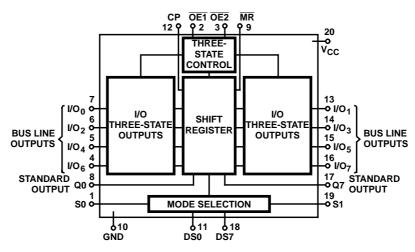
- Both output enable (OE1 and OE2) inputs are low and S0 or S1 or both are low, the data in the register is presented at the eight outputs.
- 2. When both S0 and S1 are high, I/O terminals are in the high impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of OE1 and OE2.
- 3. Either one of the two output enable inputs being high will force I/O terminals to be in the off-state. It is noted that each I/O terminal is a three-state output and a CMOS buffer input.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC299F3A	-55 to 125	20 Ld CERDIP
CD54HCT299F3A	-55 to 125	20 Ld CERDIP
CD74HC299E	-55 to 125	20 Ld PDIP
CD74HC299M	-55 to 125	20 Ld SOIC
CD74HC299M96	-55 to 125	20 Ld SOIC
CD74HCT299E	-55 to 125	20 Ld PDIP
CD74HCT299M	-55 to 125	20 Ld SOIC
CD74HCT299M96	-55 to 125	20 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

Functional Diagram



MODE SELECT FUNCTION TABLE THREE-STATE I/O PORT OPERATING MODE

		INPUTS/OUTPUTS				
FUNCTION	OE1	OE2	S0	S1	Qn (REGISTER)	I/O0 I/O7
Read Register	L	L	L	X	L	L
	L	4	_ ₁	X	Н	Н
	٦	L)\	X	L	L	L
	L	L	Х	L	Н	Н
Load Register	X	X	Н	Н	Qn = I/On	I/On = Inputs
Disable I/O	Н	X	Х	Х	Х	(Z)
	X	Н	Х	Х	Х	(Z)

TRUTH TABLE

				INPUTS					REGIS	TER OU	TPUTS	
FUNCTION	MR	СР	S0	S1	DS0	DS7	I/On	Q0	Q1		Q6	Q7
RESET (CLEAR)	L	х	Х	Х	х	Х	Х	L	L		L	L
Shift Right	Н	1	h	I	I	Х	Х	L	q ₀		q_5	q ₆
	Н	1	h	I	h	Х	Х	Н	q ₀		q ₅	Q6
Shift Left	Н	1	I	h	Х	I	Х	q ₁	q2		97	L
	Н	1	I	h	Х	h	Х	91	q ₂		q ₇	Н
Hold (Do Nothing)	Н	1	I	I	Х	Х	Х	q ₀	9 1		q ₆	97
Parallel Load	Н	1	h	h	Х	Х	I	L	L		L	L
	Н	1	h	h	Х	Х	h	Н	Н		Н	Н

H = Input Voltage High Level, h = Input voltage high one set-up timer prior clock transition; L = Input Voltage Low Level; I = Input voltage low one set-up time prior to clock transition; qn = Lower case letter indicates the state of the reference output one set-up time prior to clock transition; X - Voltage level on logic status don't care; Z = Output in high impedance state, ↑ = Low to High Clock Transition.

Thermal Information Absolute Maximum Ratings DC Supply Voltage, VCC $\,$ -0.5V to 7V $\,$ θ_{JA} (°C/W) Thermal Resistance (Typical, Note 1) DC Input Diode Current, I_{IK} M (SOIC) Package.....58 DC Output Diode Current, I_{OK} For $V_O < -0.5V$ or $V_O > V_{CC}^{-1} + 0.5V$ ± 20 mA Maximum Storage Temperature Range $\dots -65^{o}C$ to $150^{o}C$ DC Drain Current, per Output, I_{O.} For -0.5V < V_O < V_{CC} + 0.5V Maximum Lead Temperature (Soldering 10s).....300°C (SOIC - Lead Tips Only) For I/O Outputs.....±35mA DC Output Source or Sink Current per Output Pin, IO For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$±25mA **Operating Conditions** Temperature Range, T_A -55°C to 125°C Supply Voltage Range, V_{CC} HC Types2V to 6V DC Input or Output Voltage, $V_{\mbox{\scriptsize I}},\,V_{\mbox{\scriptsize O}}$ 0V to $V_{\mbox{\scriptsize CC}}$ Input Rise and Fall Time 4.5V...... 500ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

			EST DITION	s	V _{CC}		25°C		-40°C T	O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	V ₁ (V)	l _o (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES													
High Level Input	V _{IH}	-		-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage					4.5	3.15	-	-	3.15	-	3.15	-	V
					6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V _{IL}	-		-		-	-	0.5	-	0.5	-	0.5	V
Voltage					4.5	-	-	1.35	-	1.35	-	1.35	V
					6	-	-	1.8	-	1.8	-	1.8	V
High Level Output	V _{OH}	V _{IH} or V _{IL}	-0.	.02	2	1.9	-	-	1.9	-	1.9	-	V
Voltage CMOS Loads					4.5	4.4	-	-	4.4	-	4.4	-	V
OWIGO Educa					6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			Qn	I/On	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	-6	4.5	3.98	-	-	3.84	-	3.7	-	V
TTE Education			-5.2	-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V _{OL}	V _{IH} or V _{IL}	0.	02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads					4.5	-	-	0.1	-	0.1	-	0.1	V
OWIGO Educa					6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output			Qn	I/On	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	6	4.5	-	-	0.26	-	0.33	-	0.4	V
TTE EUGGS			5.2	7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lį	V _{CC} or GND		-	6	-	-	±0.1	-	±1	-	±1	μА

DC Electrical Specifications (Continued)

			EST DITIONS	v _{cc}		25°C		-40°C T	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V _I (V)	I _O (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μА
Three- State Leak- age Current	V _{IL} or V _{IH}	V _O =V _{CC} or GND	-	6	-	-	±0.5	-	±5	-	±10	μА
HCT TYPES	•									•	•	
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	35	0.1	1.75	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	3	为 (0.26	.0.	0.33	-	0.4	V
Input Leakage Current	lį	V _{CC} and GND	0	5.5		.0	±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V _{CC} or GND	0	5.5		-	8	-	80	-	160	μА
Three- State Leak- age Current	V _{IL} or V _{IH}	V _O =V _{CC} or GND		6	-	-	±0.5	-	±5	-	±10	μА
Additional Quies- cent Device Cur- rent Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1		4.5 to 5.5	-	100	360	-	450	-	490	μА

NOTE:

HCT Input Loading Table

INPUT	UNIT LOADS
S1, MR	0.25
I/O ₀ - I/O ₇	0.25
DS0, DS7	0.25
S0, CP	0.6
OE1, OE2	0.3

NOTE: Unit Load is ΔI_{CC} limit specific in Static Specifications Table, e.g., $360\mu A$ max. at $25^{o}C.$

^{2.} For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Prerequisite for Switching Specifications

				25°C		-40	°C TO 85	o°C	-55 ⁰	C TO 12	5°C	
PARAMETER	SYMBOL	V _{CC} (V)	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	МАХ	UNITS
HC TYPES	•											•
Maximum Clock	f _{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
Frequency		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
MR Pulse Width	t _W	2	50	-	-	65	-	-	75	-	-	ns
		4.5	10	-	-	13	-	-	15	-	-	ns
		6	9	-	-	11	-	-	13	-	-	ns
Clock Pulse Width	t _W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Setup Time	tsu	2	100	-	-	125	31	4	150	-	-	ns
DS0, DS7, I/On to Clock		4.5	20	-	-	25	40	-10	30	-	-	ns
		6	17	-	90	21	-	O.	26	-	-	ns
Hold Time DS0, DS7,	t _H	2	0	1	13	0	10.	-	0	-	-	ns
I/On, S0, S1 to Clock		4.5	0	-	-	0	-	-	0	-	-	ns
		6	0), - [0	-	=	0	-	-	ns
Recovery Time	t _{REC}	2	5		-	5	-	-	5	-	-	ns
MR to Clock		4.5	5	-	=	5	-	=	5	-	-	ns
		6	5	-	=	5	-	=	5	-	-	ns
Setup Time	t _{SU}	2	120	-	=	150	-	=	180	-	-	ns
S1, S0 to Clock		4.5	24	-	-	30	-	-	36	-	-	ns
		6	20	-	-	26	-	-	31	-	-	ns
HCT TYPES												
Maximum Clock Frequency	f _{MAX}	4.5	25	-	-	20	-	-	16	-	-	MHz
MR Pulse Width	t _W	4.5	15	-	-	19	-	-	22	-	-	ns
Clock Pulse Width	t _W	4.5	20	-	-	25	-	-	30	-	-	ns
Setup Time DS0, DS7, I/On, S0, S1 to Clock	t _{SU}	4.5	20	-	-	25	-	-	30	-	-	ns
Hold Time DS0, DS7, I/On, S0, S1 to Clock	tH	4.5	0	-	-	0	-	-	0	-	-	ns
Recovery Time MR to Clock	t _{REC}	4.5	5	-	-	5	-	-	5	-	-	ns
Setup Time S1, S0 to Clock	t _{SU}	4.5	27	-	-	34	-	-	41	-	-	ns

Switching Specifications $C_L = 50pF$, Input t_r , $t_f = 6ns$

		TEST			25°C		-40 ⁰ 85	с то °С		С ТО 5°С	
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES											
Propagation Delay	t _{PLH} , t _{PHL}	$C_L = 50pF$									
Clock to I/O Output, Clock to Q0 and Q7,			2	-	-	200	-	250	-	300	ns
MR to Output			4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	34	-	43	-	51	ns
Output Enable and Disable	t _{PZL}	C _L = 15pF	5	-	10	-	-	-	-	-	ns
Times	t _{PZH} , t _{PLZ}			-	13	-	-	-	-	-	ns
	t _{PHZ}			-	15	-	-	-	-	-	ns
Output High-Z to High Level	t _{PZH}	C _L = 50pF	2	-	-	155	-	195	-	235	ns
			4.5	-	-	31	g-	39	-	47	ns
			6	-	35- 3	26	-0	33	-	40	ns
Output High Level to High-Z	t _{PHZ}	C _L = 50pF	2	20 9	13	185	3	230	_	280	ns
			4.5	10		37	-	46	-	56	ns
			6	-,5		31	_	39	-	48	ns
Output Low Level to High-Z	t _{PLZ}	C _L = 50pF	2	_	-	155	_	195	-	235	ns
			4.5	-	_	31	_	39	-	47	ns
			6	-	-	26	-	33	-	40	ns
Output High-Z to Low Level	t _{PZL}	C _L = 50pF	2	-	-	130	_	165	-	195	ns
	1.22		4.5	-	_	26	_	33	-	39	ns
			6	-	_	22	_	28	-	33	ns
Output Transition Time	t _{THL} , t _{TLH}	C _L = 50pF									
Q0, Q7	*1116, *1611	2 <u> 24</u>	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
I/O ₀ to I/O ₇	t _{THL} , t _{TLH}	C _L = 50pF	2	-	-	60	-	75	-	90	ns
		-	4.5	-	-	12	-	15	-	18	ns
			6	-	_	10	-	13	-	15	ns
Input Capacitance	Cl	C _L = 50pF	-	10	-	10	_	10	-	10	pF
Three-State Output Capacitance	CO		-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L = 15pF	5	-	150	-	-	-	-	-	pF

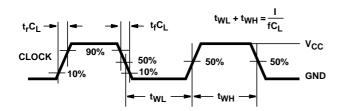
Switching Specifications $C_L = 50pF$, Input t_r , $t_f = 6ns$ (Continued)

		TEST			25°C			С ТО °С		C TO 5°C		
PARAMETER	SYMBOL	CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS	
HCT TYPES			=								-	
Propagation Delay	t _{PHL} , t _{PLH}											
Clock to I/O Output, Clock to Q0 and Q7		$C_L = 50pF$	4.5	-	-	45	-	56	-	68	ns	
Clock to Qu and Q7		C _L = 15pF	5	-	19	-	-	-	-	-	ns	
MR to Output	t _{PHL} , t _{PLH}	C _L = 50pF	4.5	-	-	46	-	58	-	69	ns	
Output Enable and Disable Times	t _{PZL} , t _{PZH} , t _{PLZ} , t _{PHZ}	C _L = 15pF	5	-	10, 13, 15	-	-	-	-	-	ns	
Output High-Z to High Level	t _{PZH}	C _L = 50pF	4.5	-	-	32	-	40	-	48	ns	
Output High Level to High-Z	t _{PHZ}	C _L = 50pF	4.5	-	-	37	-	46	-	56	ns	
Output Low Level to High-Z	t _{PLZ}	C _L = 50pF	4.5	-	-	32	-	40	-	48	ns	
Output High-Z to Low Level	t _{PZL}	C _L = 50pF	4.5	-	-	30	2	38	-	45	ns	
Output Transition Time	t _{TLH} , t _{THL}	0 50 5	4.5		20. 1	15	713	40		-00		
Q0, Q7		C _L = 50pF	4.5	- 3	1	15		19	-	22	ns	
I/O ₀ to I/O ₇		$C_L = 50pF$	4.5	16		12	-	15	-	18	ns	
Input Capacitance	C _{IN}	C _L = 50pF	-	10	O	10	-	10	-	10	pF	
Three-State Output Capacitance	CO			20		20	-	20	-	20	pF	
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L = 15pF	5	-	170	-	-	-	-	-	pF	

NOTES:

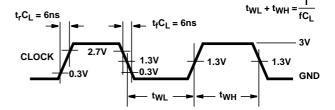
- 3. C_{PD} is used to determine the dynamic power consumption, per register.
- P_D = C_{PD} V_{CC}² f_i + Σ (C_L V_{CC}² f_O) where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% $\rm V_{CC}$ to 90% $\rm V_{CC}$ in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND **PULSE WIDTH**



NOTE: Outputs should be switching from 10% $\rm V_{CC}$ to 90% $\rm V_{CC}$ in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND **PULSE WIDTH**

Test Circuits and Waveforms (Continued)

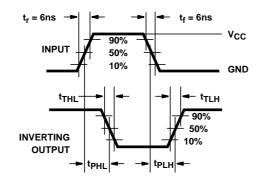


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

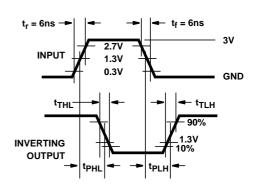


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

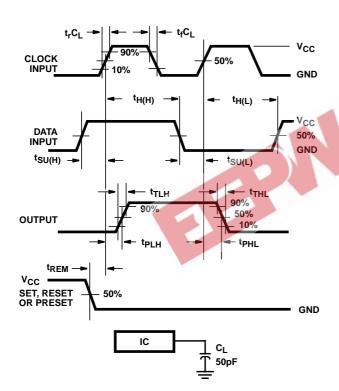


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

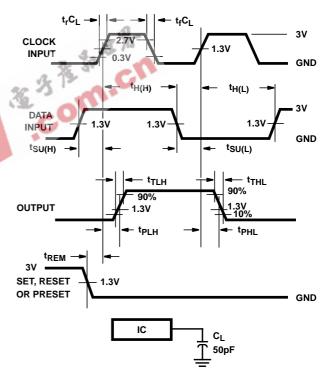


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued) t_f -3V OUTPUT v_{cc} OUTPUT DISABLE **DISABLE** 50% 0.3 10% GND GND t_{PZL} t_{PZL} t_{PLZ} → t_{PLZ} → **OUTPUT LOW OUTPUT LOW** 50% TO OFF TO OFF 1.3V 10% 10% ◆ t_{PHZ} ◆ ← t_{PZH} ← t_{PHZ} ← <- t_{PZH} → 90% 90% **OUTPUT HIGH OUTPUT HIGH** TO OFF TO OFF OUTPUTS -OUTPUTS OUTPUTS OUTPUTS **OUTPUTS OUTPUTS ENABLED** ENABLED DISABLED **ENABLED** DISABLED ENABLED FIGURE 7. HC THREE-STATE PROPAGATION DELAY FIGURE 8. HCT THREE-STATE PROPAGATION DELAY **WAVEFORM WAVEFORM** OTHER (OUTPUT

INPUTS

OR LOW 0

OUTPUT DISABLE

TIED HIGH

IC WITH

THREE-

STATE

OUTPUT

NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

 $R_L = 1k\Omega$

 $\textbf{C}_{\textbf{L}}$

50pF

V_{CC} FOR t_{PLZ} AND t_{PZL}

GND FOR tPHZ AND tPZH

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
5962-8780601RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8943601MRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC299F	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HC299F3A	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CD54HCT299F3A	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CD74HC299E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC299EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HC299M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC299M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC299M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC299M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC299ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC299MG4	ACTIVE	SOIC	DW	20	2 5	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT299E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT299EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74HCT299M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT299M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT299M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT299M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT299ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT299MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

Pb-Free (RoHS): Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.



PACKAGE OPTION ADDENDUM

9-Oct-2007

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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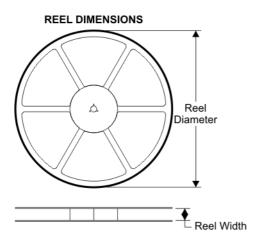


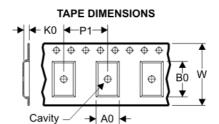


PACKAGE MATERIALS INFORMATION

4-Oct-2007

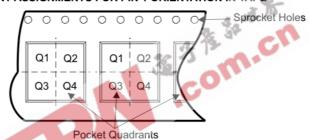
TAPE AND REEL BOX INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPES

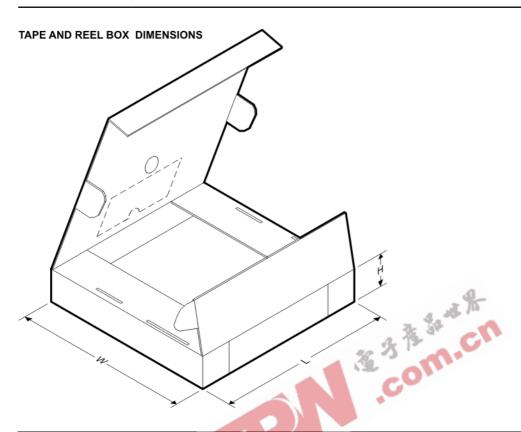


Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC299M96	DW	20	SITE 41	330	24	10.8	13.0	2.7	12	24	Q1
CD74HCT299M96	DW	20	SITE 41	330	24	10.8	13.0	2.7	12	24	Q1

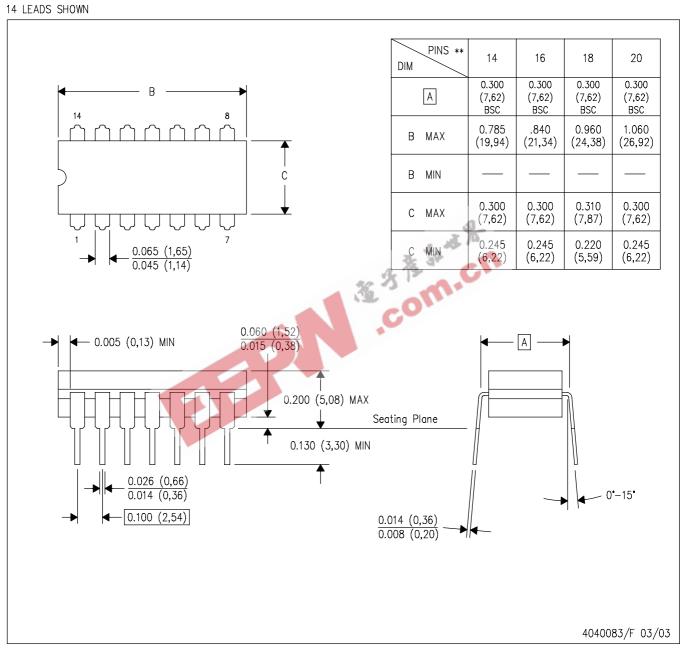




4-Oct-2007



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD74HC299M96	DW	20	SITE 41	346.0	346.0	41.0
CD74HCT299M96	DW	20	SITE 41	346.0	346.0	41.0



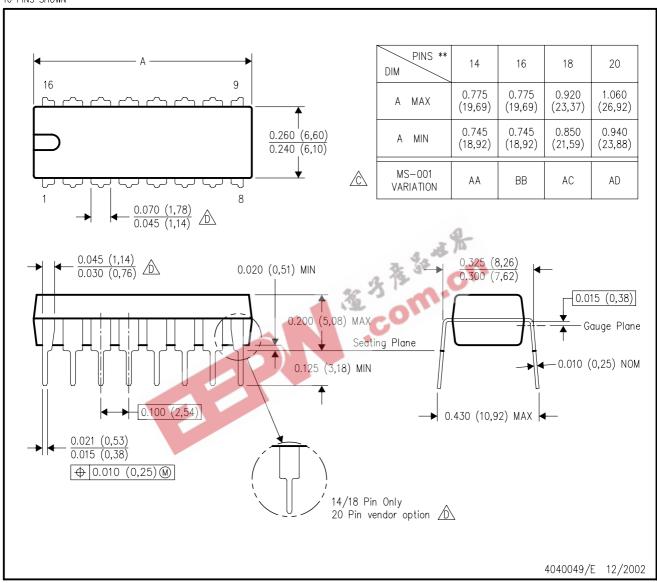
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



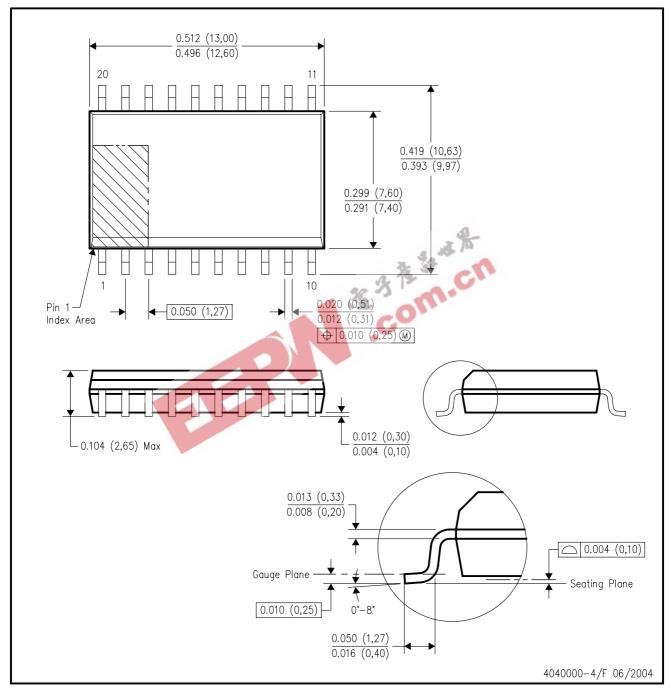
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



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