

54LS164/DM54LS164/DM74LS164 8-Bit Serial In/Parallel Out Shift Registers

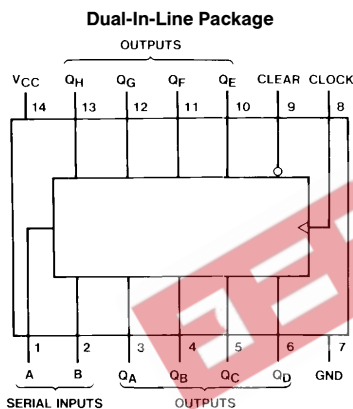
General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW
- Alternate Military/Aerospace device (54LS164) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



TL/F/6398-1

Order Number 54LS164DMQB, 54LS164FMQB,
54LS164LMQB, DM54LS164J, DM54LS164W,
DM74LS164M or DM74LS164N
See NS Package Number E20A,
J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs			
Clear	Clock	A	B	QA	QB	...	QH
L	X	X	X	L	L	...	L
H	L	X	X	QA0	QB0	...	QH0
H	↑	H	H	H	QA _n	...	QH _n
H	↑	L	X	L	QA _n	...	QH _n
H	↑	X	L	L	QA _n	...	QH _n

H = High Level (steady state), L = Low Level (steady state)

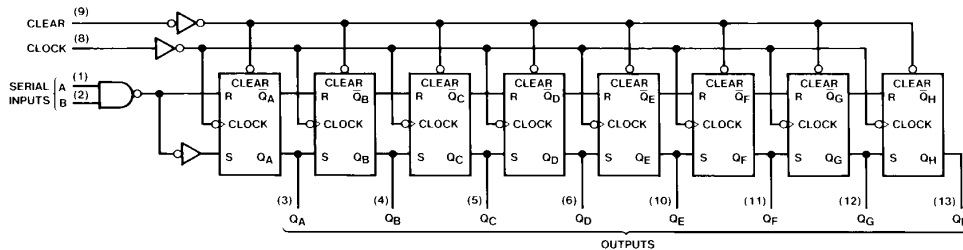
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

QA₀, QB₀, QH₀ = The level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

QA_n, QH_n = The level of QA or QH before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



TL/F/6398-2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	–55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS164			DM74LS164			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			–0.4			–0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
f _{CLK}	Clock Frequency (Note 4)	0		25	0		25	MHz
t _w	Pulse Width (Note 4)	Clock	20		20			ns
		Clear	20		20			
t _{SU}	Data Setup Time (Note 4)	17			17			ns
t _H	Data Hold Time (Note 4)	5			5			ns
t _{REL}	Clear Release Time (Note 4)	30			30			ns
T _A	Free Air Operating Temperature	–55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = –18 mA			–1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max	DM54	2.5	3.4	V
		V _{IL} = Max, V _{IH} = Min	DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max	DM54	0.25	0.4	V
		V _{IL} = Max, V _{IH} = Min	DM74	0.35	0.5	
		I _{OL} = 4 mA, V _{CC} = Min	DM74	0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			–0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	–20	–100	mA
			DM74	–20	–100	
I _{CC}	Supply Current	V _{CC} = Max (Note 3)		16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

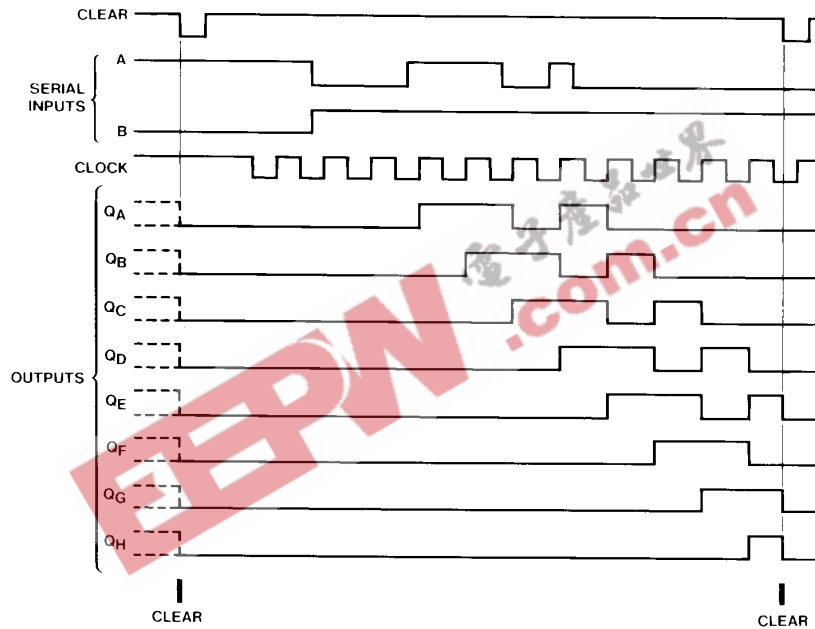
Note 3: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

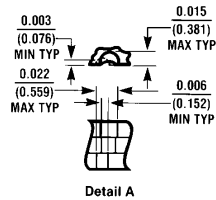
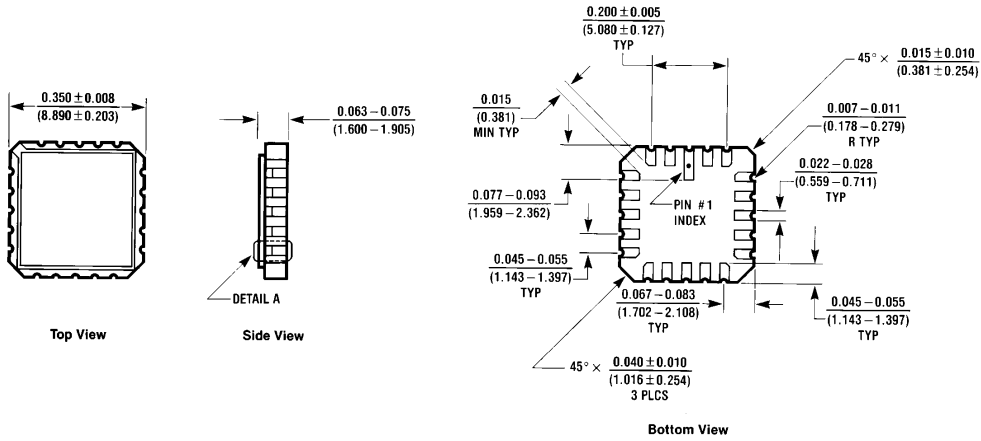
Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		45	ns

Timing Diagram



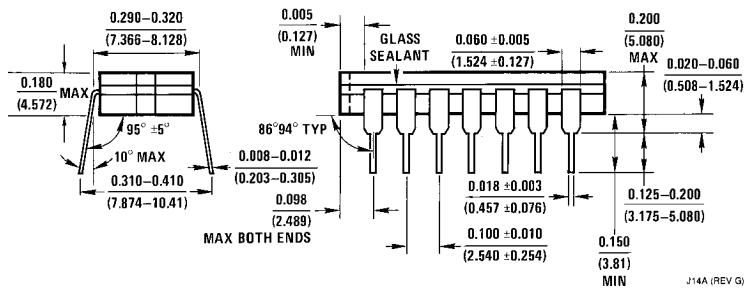
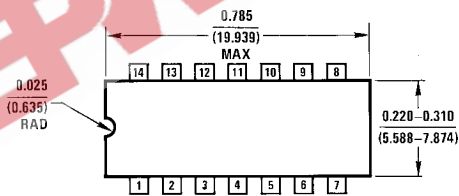
TL/F/6398-3

Physical Dimensions inches (millimeters)



Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS164LMQB
NS Package Number E20A

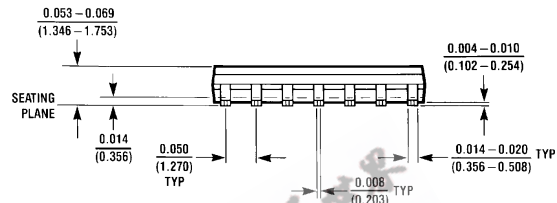
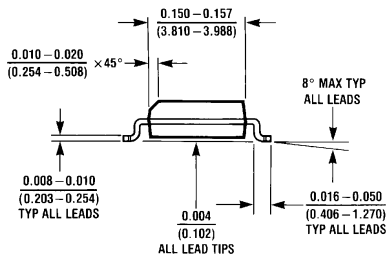
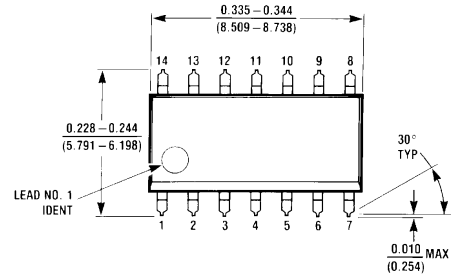
E20A (REV D)



14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS164DMQB or DM54LS164J
NS Package Number J14A

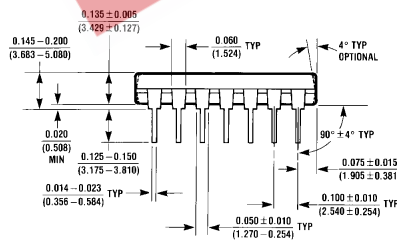
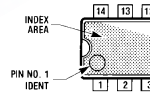
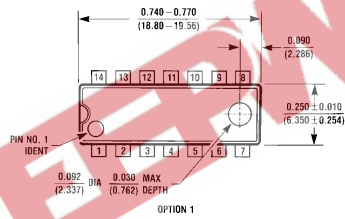
J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)

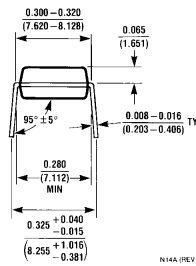


M14A (REV H)

14-Lead Small Outline Molded Package (M)
Order Number DM74LS164M
NS Package Number M14A



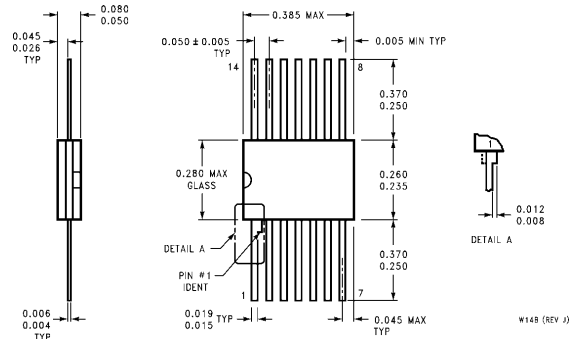
OPTION 02



N14A (REV F)

14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS164N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS164FMB or DM54LS164W
NS Package Number W14B



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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@levm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 13th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408

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