

DM74LS962 (DM86LS62) Dual Rank 8-Bit TRI-STATE® Shift Register

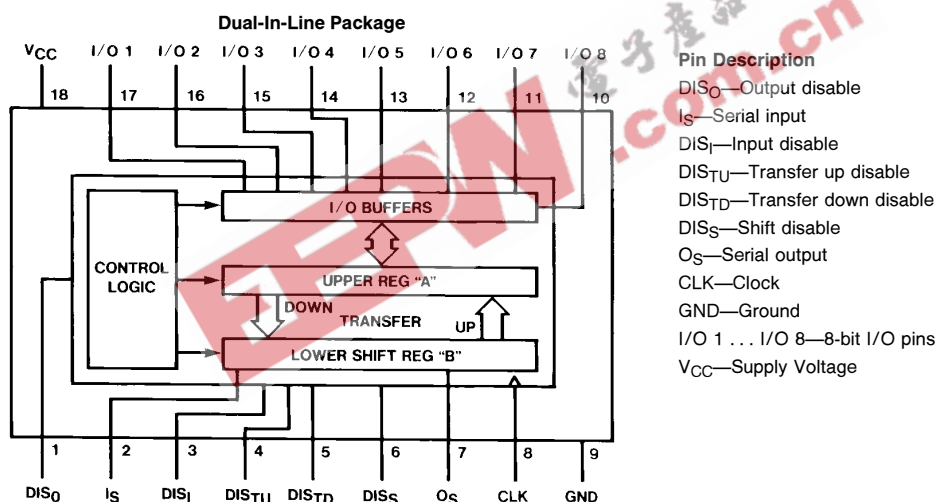
General Description

These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", or exchange data between register "A" and shift register "B". Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Connection Diagram



Top View

Order Number DM74LS962N or DM86LS62N
See NS Package Number N18A

TL/F/6438-1

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Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS/DM86LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High-Level Input Voltage	2			V
V _{IL}	Low-Level Input Voltage			0.8	V
I _{OH}	High-Level Output Current			−5.2	mA
I _{OL}	Low-Level Output Current			16	mA
f _{CLOCK}	Clock Frequency (Note 5)	0		25	MHz
Clock Pulse	High Pulse Width (Note 5)	25	17		ns
	Low Pulse Width (Note 5)	15	7		ns
t _{SET-UP}	Data Set-Up Time (Note 5)	10			ns
t _{HOLD}	Data Hold Time (Note 5)	0			ns
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)	Min	Typ (2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.5	V
V _{OH}	High-Level Output Voltage	V _{CC} = Min, V _{IH} = 2 V, V _{IL} = V _{IL} Max	I _{OH} = −2.6 mA I _{OH} = −5.2 mA			V
V _{OL}	Low-Level Output Voltage	V _{CC} = Min, V _{IH} = 2 V, V _{IL} = V _{IL} Max	I _{OL} = 8 mA I _{OL} = 16 mA	0.25 0.35	0.4 0.5	V
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max, V _I = 5.5V			0.1	mA
I _{IH}	High-Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low-Level Input Current	V _{CC} = Max, V _I = 0.4V			−50	μA
I _{OS}	Short-Circuit Output Current	V _{CC} = Max (3)	−20		−100	mA
I _{CC}	Supply Current	V _{CC} = Max (4)		61	99	mA
I _{OFF}	TRI-STATE I/O Current	V _{CC} = Max, V _{IH} = 2V	V _O = 2.4V V _O = 0.4V		20 −20	μA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

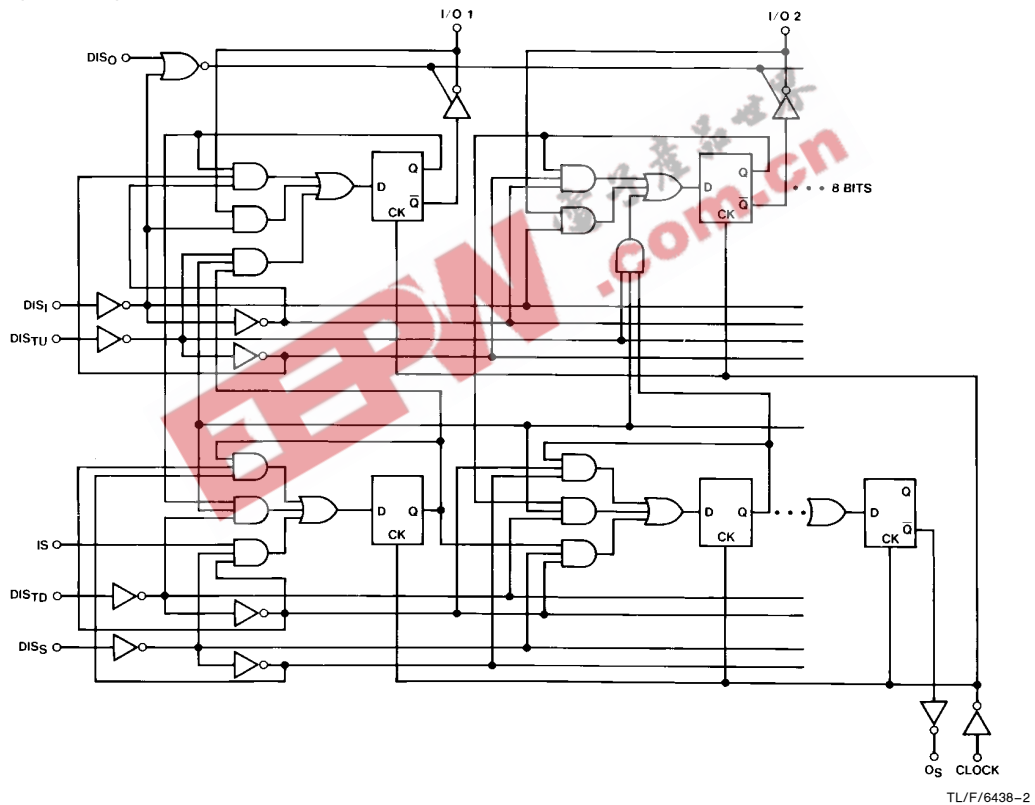
Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4V. All other control inputs and I/O pins grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics $V_{CC} = 5V$ and $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	$C_L = 15\text{ pF}, R_L = 1\text{ k}\Omega$	25		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		7	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Outputs		10	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	30	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	30	ns
t_{ZH}	Output Enable Time to High Level		5	23	ns
t_{ZL}	Output Enable to Low Level		4	18	ns
t_{HZ}	Output Disable Time from High Level	$C_L = 5\text{ pF}, R_L = 1\text{ k}\Omega$	5	23	ns
t_{LZ}	Output Disable Time from Low Level		6	27	ns

Logic Diagram



Function Table

Table 1

DISO	DISI	DIS _{TU}	DIS _{TD}	DIS _S	CLK	IS	8-Bit I/O Pins	Content of Upper Reg. "A"								Content of Lower Serial Shift Reg. "B"								Os	Comments
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state Entering data from I/O to reg. "A"
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	b1	b2	b3	b4	b5	b6	b7	b8	b8	
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A" Reg. "A" will OR data from I/O to reg. "B"
H	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	←	←	←	←	DOR	→	→	→	b1	b2	b3	b4	b5	b6	b7	b8	b8	
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B" Entering data and transfer down
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	a1	a2	a3	a4	a5	a6	a7	a8	a8	
H	H	L	L	X	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	(1) Exchange data between registers (2) Beside data exchanging, reg. "A" (3) will "OR" data from I/O and reg. "B"
L	H	L	L	X	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	L	L	X	↑	X	Input	←	←	←	←	DOR	→	→	→	a1	a2	a3	a4	a5	a6	a7	a8	a8	
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B" Entering data and serial shifting
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	d	b1	b2	b3	b4	b5	b6	b7	b7	
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting DOR function and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	L	L	↑	d	Input	←	←	←	←	DOR	→	→	→	d	b1	b2	b3	b4	b5	b6	b7	b7	

X ≡ Don't Care

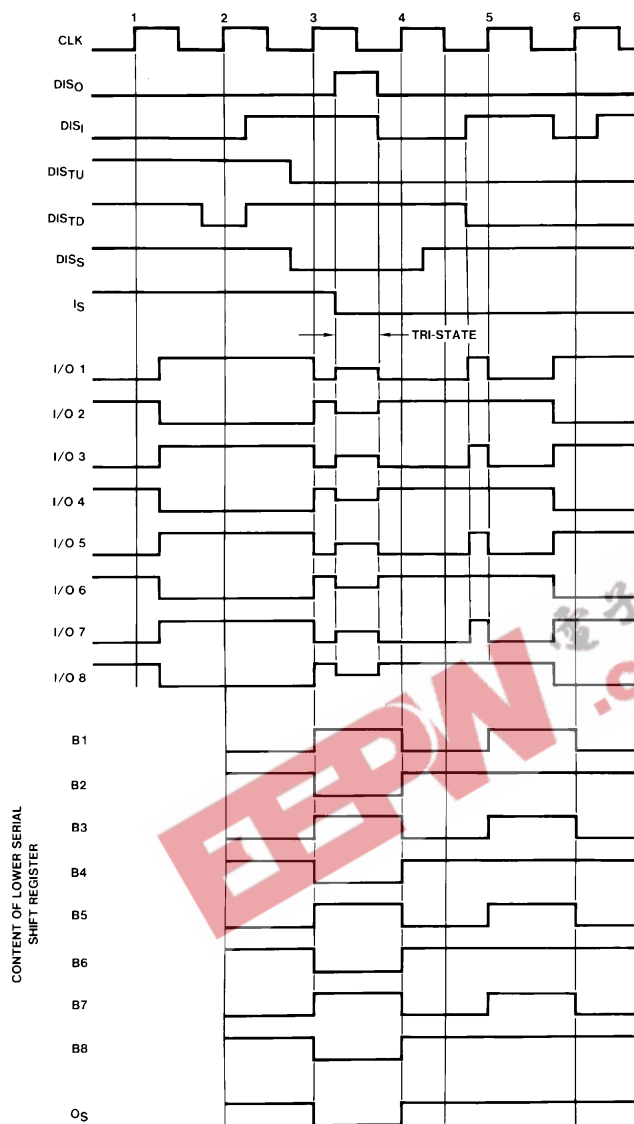
Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

a1 ... a8/b1 ... b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

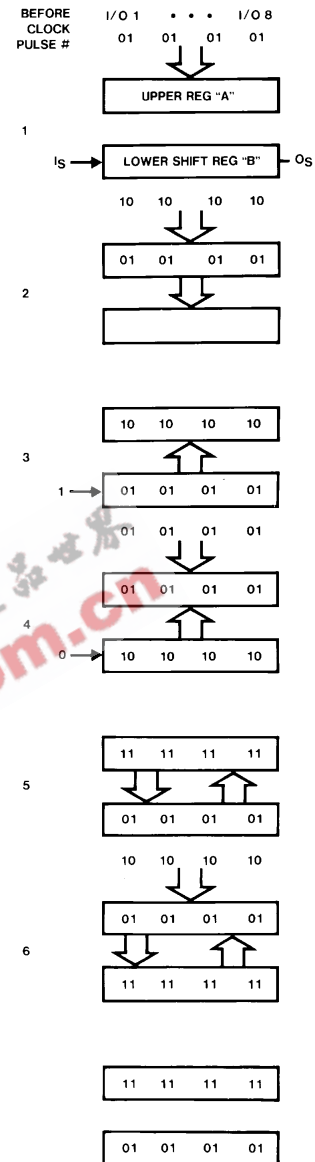
I₁ ... I₈ ≡ The level of steady state inputs of the I/O pinsDOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., I₁ + b1, I₂ + b2, I₃ + b3 ..., I₈ + b8

d ≡ Data of the serial input

Timing Diagram

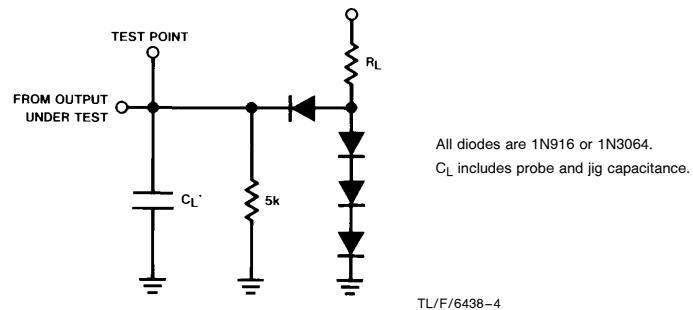


CONTENT OF LOWER SERIAL
SHIFT REGISTER

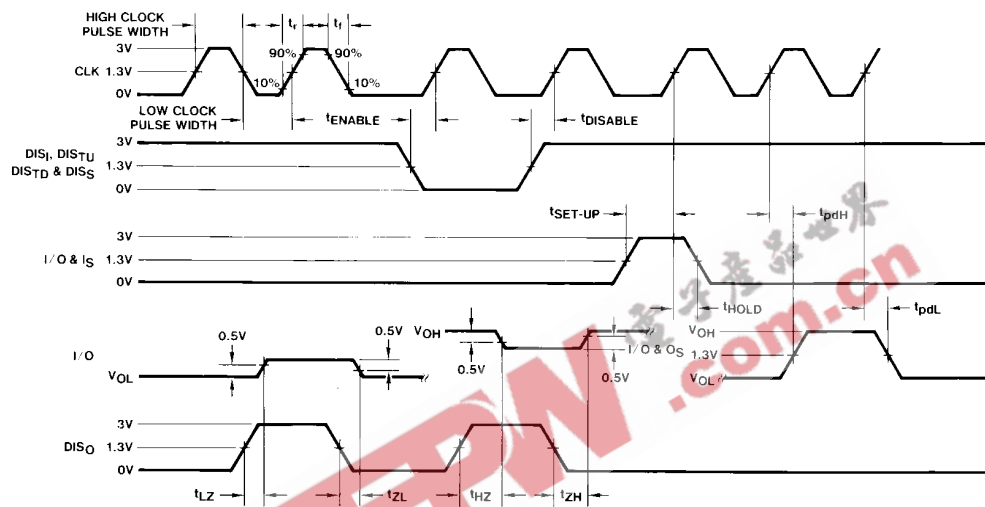


TL/F/6438-3

AC Test Circuit and Switching Time Waveforms



TL/F/6438-4

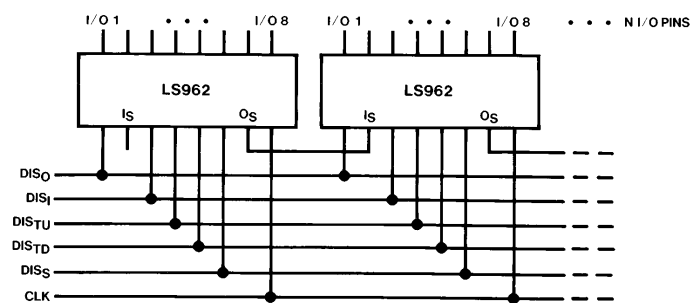


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All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, $Z_{OUT} \approx 50\Omega$.

Cascading Packages

Cascading Packages for N-Bit Word

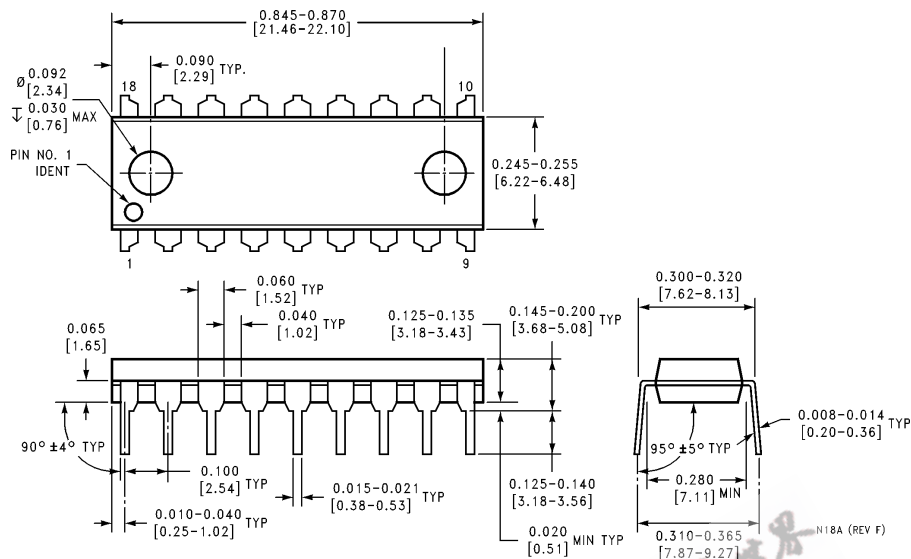


TL/F/6438-6

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DM74LS962 (DM86LS62) Dual Rank 8-Bit TRI-STATE Shift Register

Physical Dimensions inches (millimeters)



18-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS962N or DM86LS62N
NS Package Number N18A

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