

**IW4021B**

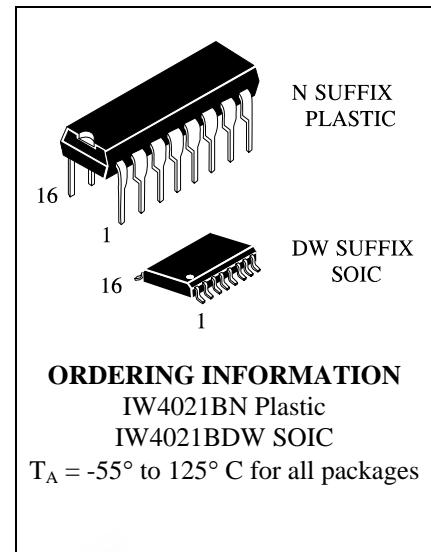
**8-Bit Shift Register  
High-Voltage Silicon-Gate CMOS**

The IW4021B is an Edge-Triggered 8-Bit Shift Register (Parallel-to-Serial Converter) with a synchronous Serial Data Input (D<sub>S</sub>), a Clock Input (CP), an asynchronous active HIGH Parallel Load Input (PL), eight asynchronous Parallel Data Inputs (P<sub>0</sub>-P<sub>7</sub>) and Buffered Parallel Outputs from the last three stages (Q<sub>5</sub>-Q<sub>7</sub>).

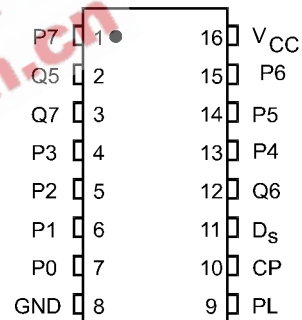
Information on the Parallel Data Inputs (P<sub>0</sub>-P<sub>7</sub>) is asynchronously loaded into the register while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Serial Data (D<sub>S</sub>) inputs. Data present in the register is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL).

When the Parallel Load Input is LOW, data on the Serial Data Input (D<sub>S</sub>) is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

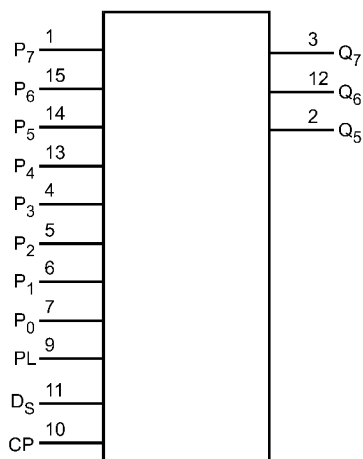
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply



**PIN ASSIGNMENT**



**LOGIC DIAGRAM**



PIN 16 = V<sub>CC</sub>  
PIN 8 = GND

**FUNCTION TABLE**

**SERIAL OPERATION:**

t	CP	D <sub>S</sub>	PL	Q <sub>5</sub> t=n+6	Q <sub>6</sub> t=n+7	Q <sub>7</sub> t=n+8
n	⌊	0	0	0		
n+1	⌋	1	0	1	0	
n+2	⌊	0	0	0	1	0
n+3	⌋	1	0	1	0	1
	⌋	X	0	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>

**PARALLEL OPERATION:**

CP	D <sub>S</sub>	PL	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>
X	X	1	D	D	D	D	D	D

X = don't care  
D = 1 or 0

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P <sub>D</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.5 V or V <sub>CC</sub> - 0.5 V	5.0	3.5	3.5	3.5	V
		V <sub>OUT</sub> =1.0 V or V <sub>CC</sub> - 1.0 V	10	7	7	7	
		V <sub>OUT</sub> =1.5 V or V <sub>CC</sub> - 1.5 V	15	11	11	11	
V <sub>IL</sub>	Maximum Low -Level Input Voltage	V <sub>OUT</sub> =0.5 V or V <sub>CC</sub> - 0.5 V	5.0	1.5	1.5	1.5	V
		V <sub>OUT</sub> =1.0 V or V <sub>CC</sub> - 1.0 V	10	3	3	3	
		V <sub>OUT</sub> =1.5 V or V <sub>CC</sub> - 1.5 V	15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0	5.0	5.0	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> V <sub>OL</sub> =0.4 V V <sub>OL</sub> =0.5 V V <sub>OL</sub> =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> V <sub>OH</sub> =2.5 V V <sub>OH</sub> =4.6 V V <sub>OH</sub> =9.5 V V <sub>OH</sub> =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

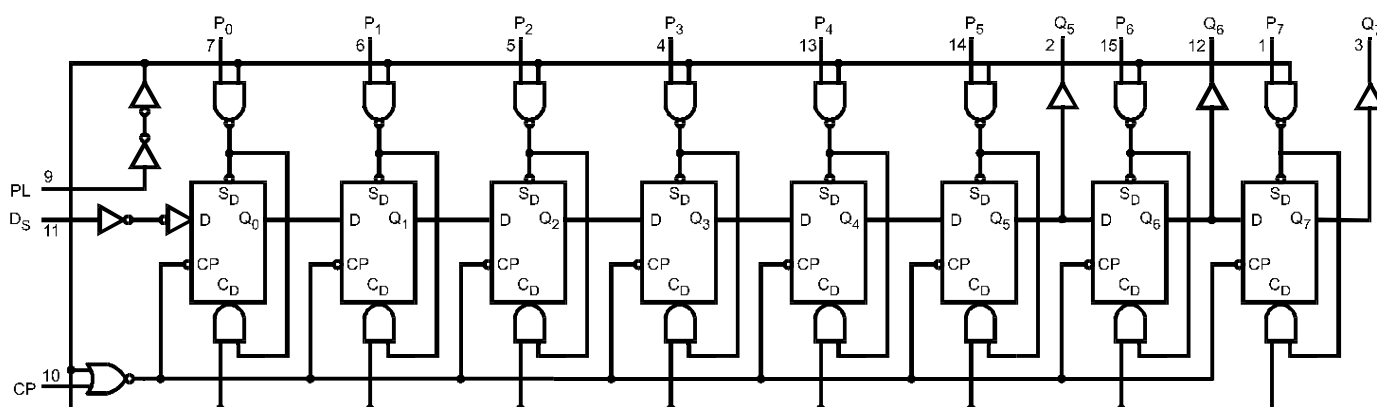
**AC ELECTRICAL CHARACTERISTICS** (C<sub>L</sub>=50pF, R<sub>L</sub>=200 kΩ, Input t<sub>r</sub>=t<sub>f</sub>=20 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
f <sub>max</sub>	Maximum Clock Frequency	5.0	3.0	3.0	1.5	MHz
		10	6.0	6.0	3.0	
		15	8.5	8.5	4.25	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CP to Qn	5.0	320	320	640	ns
		10	160	160	320	
		15	120	120	240	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, PL to Qn	5.0	320	320	640	ns
		10	160	160	320	
		15	120	120	240	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C <sub>IN</sub>	Maximum Input Capacitance	5.0		7.5		pF

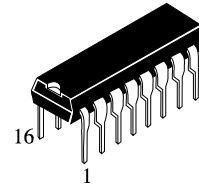
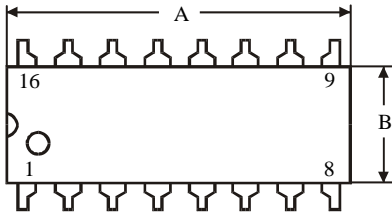
**TIMING REQUIREMENTS** ( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t <sub>w</sub>	Minimum Pulse Width CP	5.0	160	160	320	ns
		10	80	80	160	
		15	50	50	100	
t <sub>w</sub>	Minimum Pulse Width PL	5.0	180	180	360	ns
		10	80	80	160	
		15	50	50	100	
t <sub>su</sub>	Minimum Setup Time, D <sub>S</sub> to CP	5.0	120	120	240	ns
		10	80	80	160	
		15	60	60	120	
t <sub>su</sub>	Minimum Setup Time, P <sub>n</sub> to PL	5.0	50	50	100	ns
		10	30	30	60	
		15	20	20	40	
t <sub>h</sub>	Minimum Hold Time, D <sub>S</sub> to CP	5.0	0	0	0	ns
		10	0	0	0	
		15	0	0	0	
t <sub>h</sub>	Minimum Hold Time, P <sub>n</sub> to PL	5.0	0	0	0	ns
		10	0	0	0	
		15	0	0	0	
t <sub>rec</sub>	Minimum Recovery Time PL	5.0	280	280	560	ns
		10	140	140	240	
		15	100	100	200	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise or Fall Time	5.0	15	15	15	μs
		10	15	15	15	
		15	15	15	15	

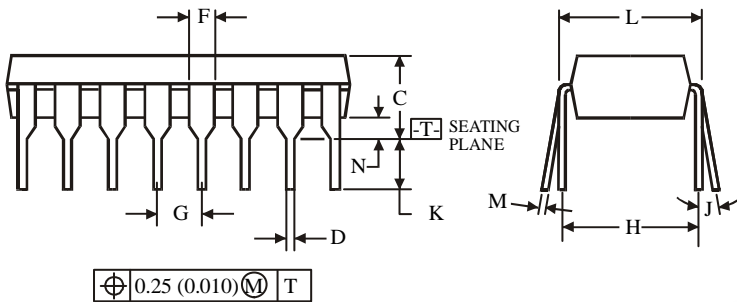
**EXPANDED LOGIC DIAGRAM**



**N SUFFIX PLASTIC  
(MS - 001BB)**



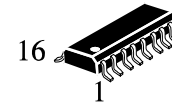
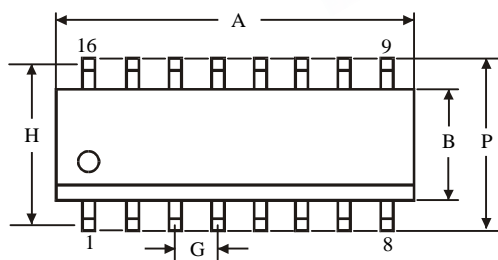
Symbol	Dimensions, mm	
	MIN	MAX
A	18.67	19.69
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	



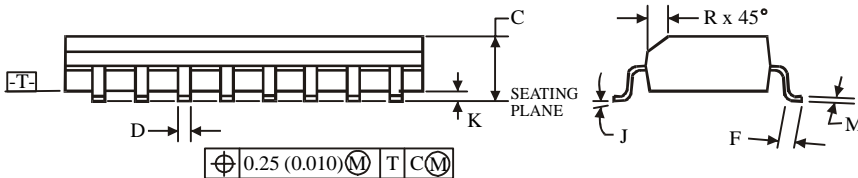
**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

**D SUFFIX SOIC  
(MS - 012AC)**



Symbol	Dimensions, mm	
	MIN	MAX
A	9.80	10.0
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50



**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A, for B - 0.25 mm (0.010) per side.