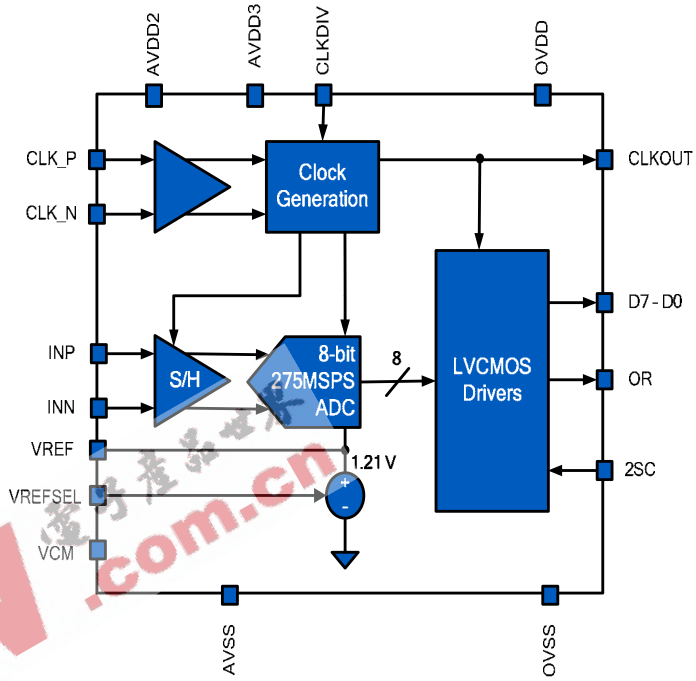
KAD2708C

8-Bit, 275MSPS Analog-to-Digital Converter

Description

The Kenet **KAD2708C** is the industry's lowest power, 8-bit, high performance Analog-to-Digital converter. The converter runs at sampling rates up to 275MSPS, and is fabricated with Kenet's proprietary ***FemtoCharge®*** CMOS technology. Users can now obtain industry-leading SNR and SFDR specifications while nearly halving power consumption. Sampling rates of 210, 170 and 105MSPS are also available in the same pin-compatible package and in versions with 10-bit resolution. Kenet's KAD2708L offers this performance with LVDS outputs. All are available in 68-pin RoHS-compliant QFN packages with exposed paddle. Performance is specified over the full industrial temperature range (-40 to +85°C).



Key Specifications

- **SNR of 48.8dB at Nyquist**
- **SFDR of 68dBc at Nyquist**
- **Power consumption ≤ 265mW at f_S = 275MSPS**

Features

- **On-chip reference**
- **Internal track and hold**
- **1.5V_{PP} differential input voltage**
- **600MHz analog input bandwidth**
- **Two's complement or binary output**
- **Over-range indicator**
- **Selectable ÷2 Clock Input**
- **LVCMOS compatible outputs**

Applications

- **High-Performance Data Acquisition**
- **Portable Oscilloscope**
- **Medical Imaging**
- **Cable Head Ends**
- **Power-Amplifier Linearization**
- **Radar and Satellite Antenna Array Processing**
- **Broadband Communications**
- **Local Multipoint Distribution System (LMDS)**
- **Communications Test Equipment**

Resolution, Speed	LVDS Outputs	LVCMOS Outputs
8 Bits 350MSPS	KAD2708L-35	
10 Bits 275MSPS	KAD2710L-27	KAD2710C-27
8 Bits 275MSPS	KAD2708L-27	KAD2708C-27
10 Bits 210MSPS	KAD2710L-21	KAD2710C-21
8 Bits 210MSPS	KAD2708L-21	KAD2708C-21
10 Bits 170MSPS	KAD2710L-17	KAD2710C-17
8 Bits 170MSPS	KAD2708L-17	KAD2708C-17
10 Bits 105MSPS	KAD2710L-10	KAD2710C-10
8 Bits 105MSPS	KAD2708L-10	KAD2708C-10

Table 1. Pin-Compatible Products

300 Unicorn Park Dr., Woburn, MA 01801 Sales: 1-781-497-0060 Sales@kenetinc.com

Absolute Maximum Ratings[1]

Parameter	Min	Max	Unit
AVDD2 to AVSS	-0.4	2.1	V
AVDD3 to AVSS	-0.4	3.7	V
OVDD2 to OVSS	-0.4	2.1	V
Analog Inputs to AVSS	-0.4	AVDD3 + 0.3	V
Clock Inputs to AVSS	-0.4	AVDD2 + 0.3	V
Logic Inputs to AVSS (VREFSEL, CLKDIV)	-0.4	AVDD3 + 0.3	V
Logic Inputs to OVSS (RST, 2SC)	-0.4	OVDD2 + 0.3	V
VREF TO AVSS	-0.4	AVDD3 + 0.3	V
Analog Output Currents		10	mA
Logic Output Currents		10	mA
CMOS Output Currents		20	mA
Operating Temperature	-40	85	°C
Storage Temperature	-65	150	°C
Junction Temperature		150	°C

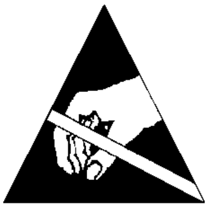
1. *Exposing the device to levels in excess of the maximum ratings may cause permanent damage. Exposure to maximum conditions for extended periods may affect device reliability.*

Thermal Impedance

Parameter	Symbol	Typ	Unit
Junction to Paddle[2]	Φ_{JP}	30	°C/W

2. Paddle soldered to ground plane.

ESD



Electrostatic charge accumulates on humans, tools and equipment, and may discharge through any metallic package contacts (pins, balls, exposed paddle, etc.) of an integrated circuit. Industry-standard protection techniques have been utilized in the design of this product. However, reasonable care must be taken in the storage and handling of ESD sensitive products. Contact Kenet for the specific ESD sensitivity rating of this product.

Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD2 = 1.8V, AVDD3 = 3.3V, OVDD = 1.8V. T_A = -40°C to +85°C, Typ values at 25°C. f_{SAMPLE} = 275MSPS f_{IN} = Nyquist.

DC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Requirements						
1.8V Analog Supply Voltage	AVDD2		1.7	1.8	1.9	V
3.3V Analog Supply Voltage	AVDD3		3.15	3.3	3.45	V
1.8V Output Supply Voltage	OVDD		1.7	1.8	1.9	V
1.8V Analog Supply Current	I_{AVDD2}			44		mA
3.3V Analog Supply Current	I_{AVDD3}			41		mA
1.8V Output Supply Current	I_{OVDD}			26		mA
Power Dissipation	P_D			261		mW

Analog Specifications

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Analog Input						
Full-Scale Differential Analog Input Voltage	V_{IN}		1.4	1.5	1.6	V_{PP}
Gain Temperature Coefficient	A_{VTC}	Full Temp		90		ppm/°C
Full Power Bandwidth	FPBW			600		MHz
Clock Input						
Sampling Clock Frequency Range	f_{SAMPLE}		50		275	MHz
CLKP, CLKN P-P Differential Input Voltage	V_{CDI}		0.5		1.8	V_{PP}
CLKP, CLKN Differential Input Resistance	R_{CDI}			10		MΩ
CLKP, CLKN Common-Mode Input Voltage	V_{CCI}			0.9		V
Reference						
Internal Reference Voltage	V_{REF}		1.18	1.21	1.24	V
Reference Voltage Temperature Coefficient	V_{RTC}	Full Temp		38		ppm/°C
Common-Mode Output Voltage	V_{CM}			0.86		V

AC Specifications

Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Signal to Noise Ratio	SNR	Full Temp	45.8	48.8		dB
Signal to Noise and Distortion	SINAD	Full Temp	45.7	48.7		dB
Effective Number of Bits	ENOB	Full Temp	7.3	7.8		Bits
Spurious Free Dynamic Range	SFDR	Full Temp	63	68		dBc
Two-Tone SFDR	2TSFDR	f_1=133MHz, f_2=135MHz		67		dBc
Integral Nonlinearity	INL		-0.8	±0.2	0.8	LSB
Differential Nonlinearity	DNL		-0.3	±0.2	0.4	LSB
Power Supply Rejection Ratio	PSRR		42	66		dB
Word Error Rate	WER			$1x10^{-12}$		

Digital Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Inputs						
High Input Voltage (VREFSEL)	VREFSEL V_{IH}		0.8*AVDD3			V
Low Input Voltage (VREFSEL)	VREFSEL V_{IL}				0.2*AVDD3	V
Input Current High (VREFSEL)	VREFSEL I_{IH}	VIN = AVDD3	0	1	10	µA
Input Current Low (VREFSEL)	VREFSEL I_{IL}	VIN = AVSS	25	65	75	µA
High Input Voltage (CLKDIV)	CLKDIV V_{IH}		0.8*AVDD3			V
Low Input Voltage (CLKDIV)	CLKDIV V_{IL}				0.2*AVDD3	V
Input Current High (CLKDIV)	CLKDIV I_{IH}	VIN = AVDD3	25	65	75	µA
Input Current Low (CLKDIV)	CLKDIV I_{IL}	VIN = AVSS	0	1	10	µA
High Input Voltage (RST,2SC)	RST,2SC V_{IH}		0.8*OVDD2			V
Low Input Voltage (RST,2SC)	RST,2SC V_{IL}				0.2*OVDD2	V
Input Current High (RST,2SC)	RST,2SC I_{IH}	VIN = OVDD	0	1	10	µA
Input Current Low (RST,2SC)	RST,2SC I_{IL}	VIN = OVSS	25	50	75	µA
Input Capacitance	C_{DI}			3		pF
CMOS Outputs						
Voltage Output High	V_{OH}			1.8		V
Voltage Output Low	V_{OL}			0		V
Output Rise Time	t_R			1.8		ns
Output Fall Time	t_F			1.4		ns

Timing Diagram

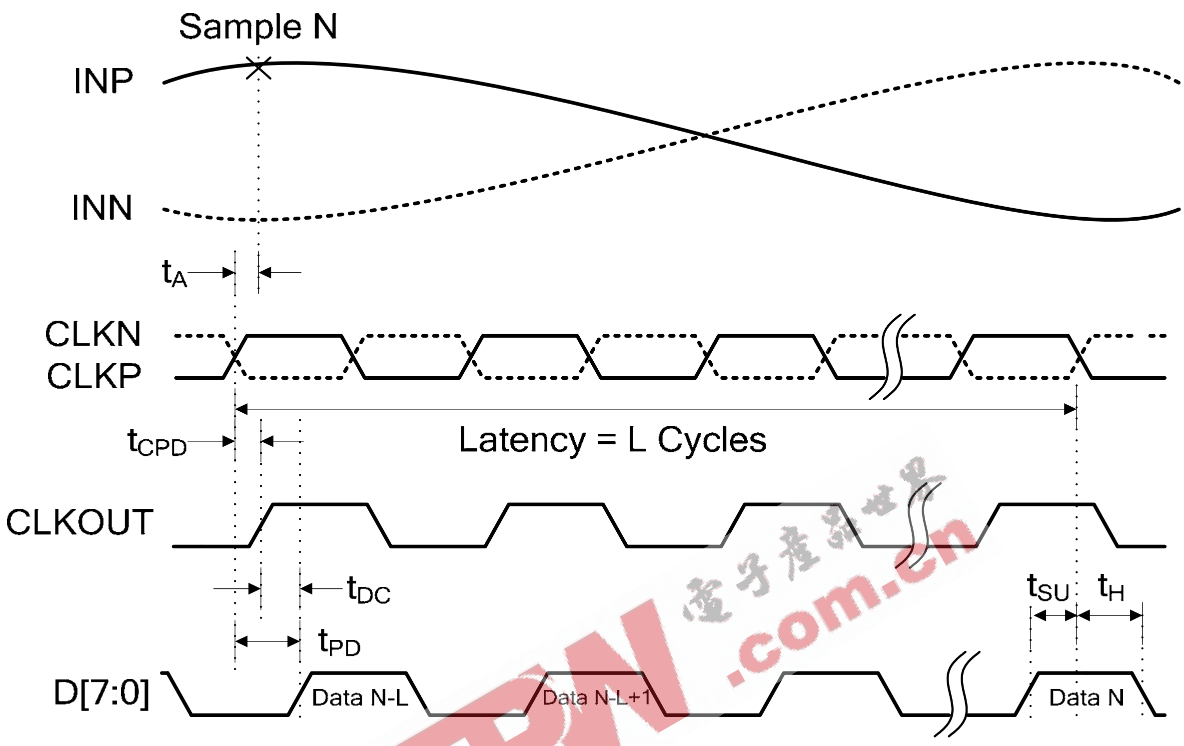


Figure 1. LVCMOS Timing Diagram

Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units
Aperture Delay	t_A		1.7		ns
RMS Aperture Jitter	j_A		200		fs
Input Clock to Data Propagation Delay	t_{PD}		1.8		ns
Input Clock to Output Clock Propagation Delay	t_{CPD}		1.3		ns
Output Clock to Data Propagation Delay	t_{DC}		470		ps
Output Data to Output Clock Setup Time	t_{SU}		3		ns
Output Clock to Output Data Hold Time	t_H		75		ps
Latency (Pipeline Delay)	L		28		cycles
Over Voltage Recovery	t_{OVR}		1		cycle

KAD2708C 8-Bit, 275MSPS Analog-to-Digital Converter

Pin Descriptions

Pin #	Name	Function
1, 14, 18, 20	AVDD2	1.8V Analog Supply
2, 7, 10, 19, 21, 24	AVSS	Analog Supply Return
3	VREF	Reference Voltage Out/In
4	VREFSEL	Reference Voltage Select (0:Int 1:Ext)
5	VCM	Common Mode Voltage Output
6, 15, 16, 25	AVDD3	3.3V Analog Supply
8, 9	INP, INN	Analog Input Positive, Negative
11-13, 29-36, 37, 39, 42, 46, 48, 50, 53, 54, 56, 58, 62, 63, 67	DNC	Do Not Connect
17	CLKDIV	Clock Divide by Two (Active Low)
22, 23	CLKN, CLKP	Clock Input Complement, True
26, 45, 61	OVSS	Output Supply Return
27, 41, 44, 60	OVDD2	1.8V CMOS Supply
28	RST	Power On Reset (Active Low)
38	D0	LVCMOS Bit 0 (LSB) Output
40	D1	LVCMOS Bit 1 Output
43	CLKOUT	LVCMOS Clock Output
47	D2	LVCMOS Bit 2 Output
49	D3	LVCMOS Bit 3 Output
51	D4	LVCMOS Bit 4 Output
53	D5	LVCMOS Bit 5 Output
55	D6	LVCMOS Bit 6 Output
57	D7	LVCMOS Bit 7 Output
59	OR	Over Range
64-66		Connect to OVDD2
68	2SC	Two's Complement Select (Active Low)
Exposed Paddle	AVSS	Analog Supply Return

Pin Configuration

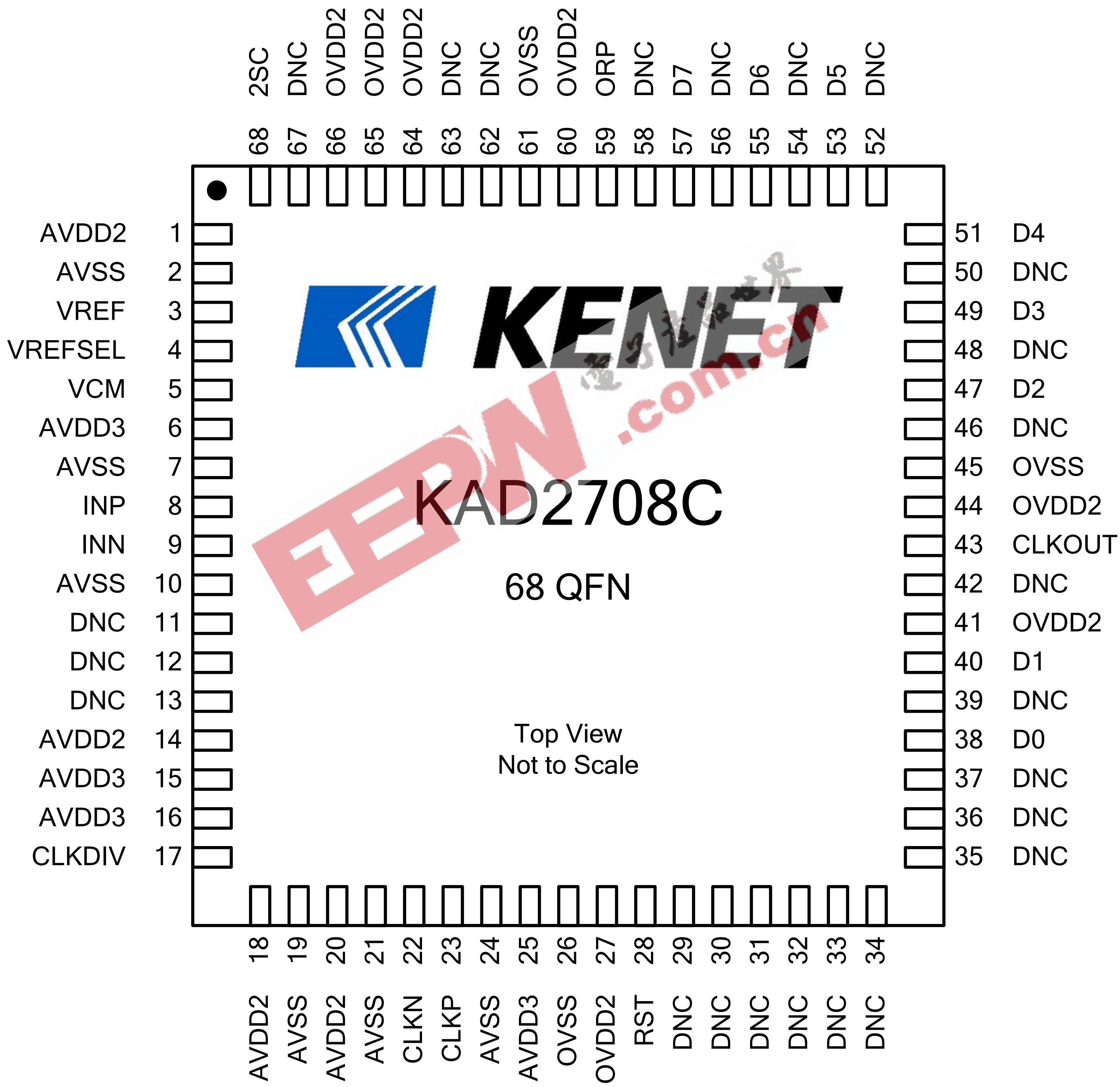


Figure 2. Pin Configuration

Typical Operating Characteristics

AVDD3=3.3V, AVDD2=OVDD2 =1.8V, $T_{AMBIENT}$ (T_A)=25°C, f_{SAMPLE}=275MHz, V_{IN}=6.865MHz @ -0.5dBFS unless noted.

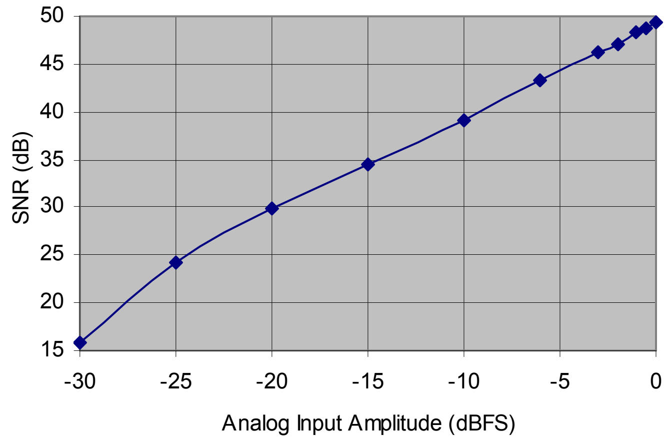


Figure 3. SNR vs. Vin

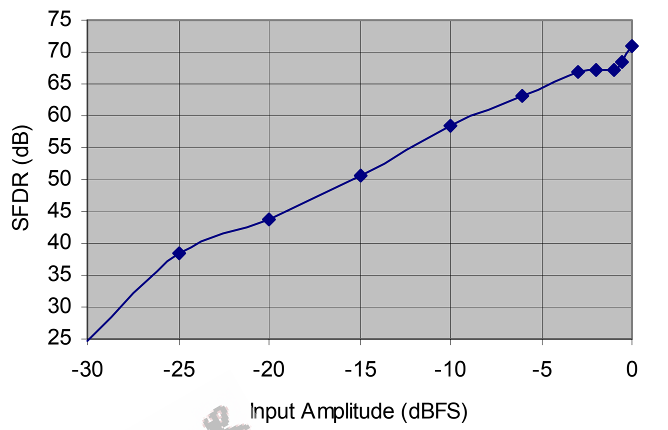


Figure 4. SFDR vs. Vin

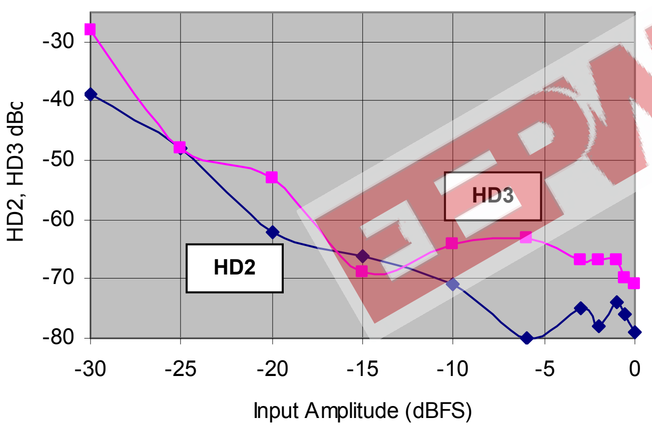


Figure 5. HD2, 3 vs. Vin

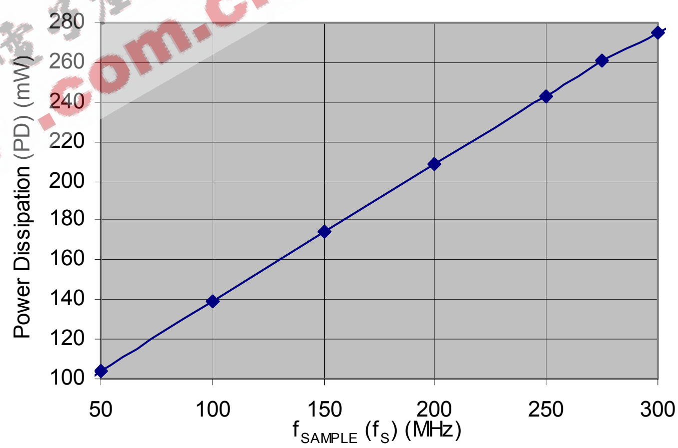


Figure 6. Power Dissipation vs. f_{SAMPLE}

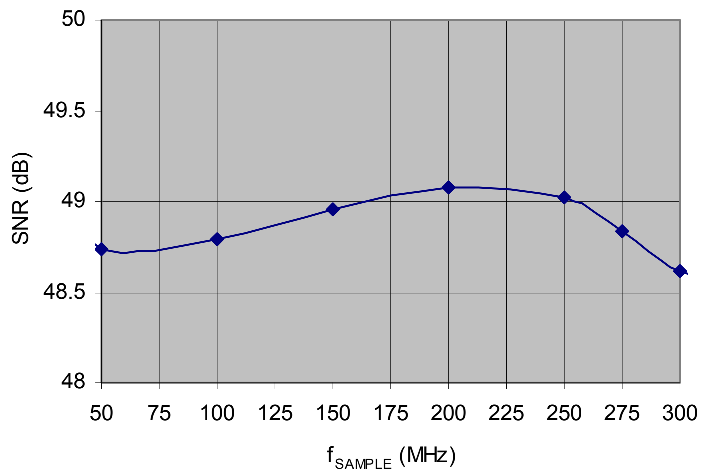


Figure 7. SNR vs. f_{SAMPLE}

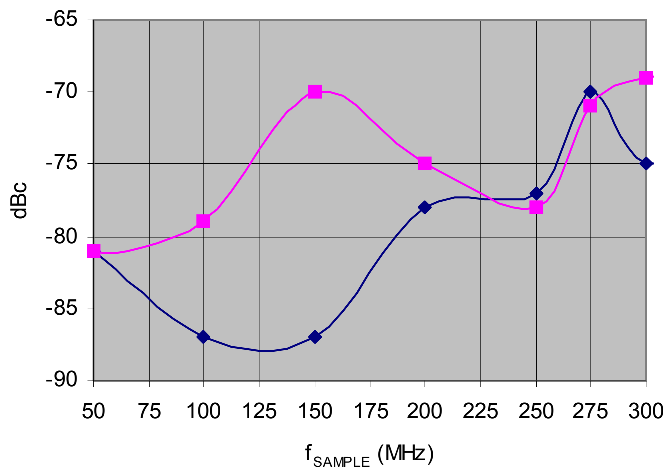


Figure 8. HD2, 3 vs. f_{SAMPLE}

AVDD3=3.3V, AVDD2=OVDD2 =1.8V, $T_{AMBIENT}$ (T_A)=25°C, f_{SAMPLE}=275MHz, V_{IN} = 6.865MHz @ -0.5dBFS unless noted.

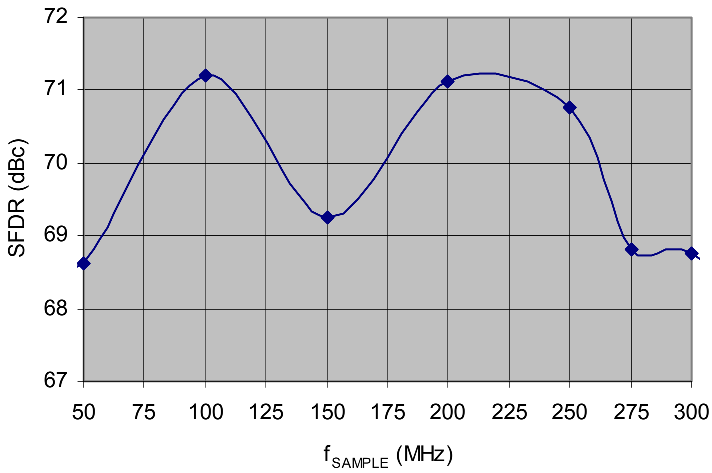


Figure 9. SFDR vs. f_{SAMPLE}

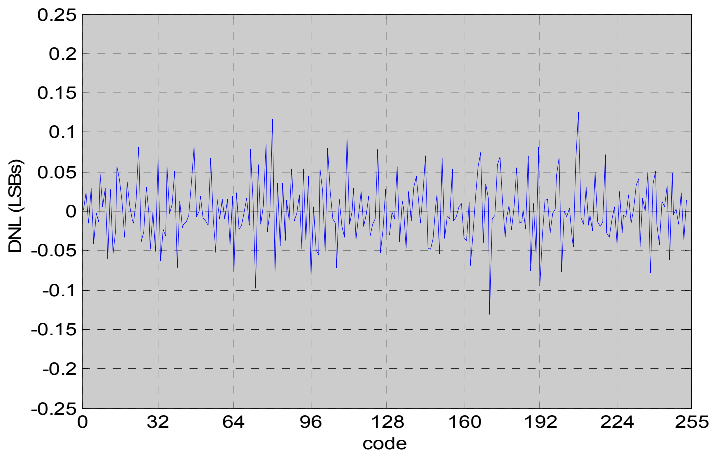


Figure 10. Differential Nonlinearity vs. Output Code

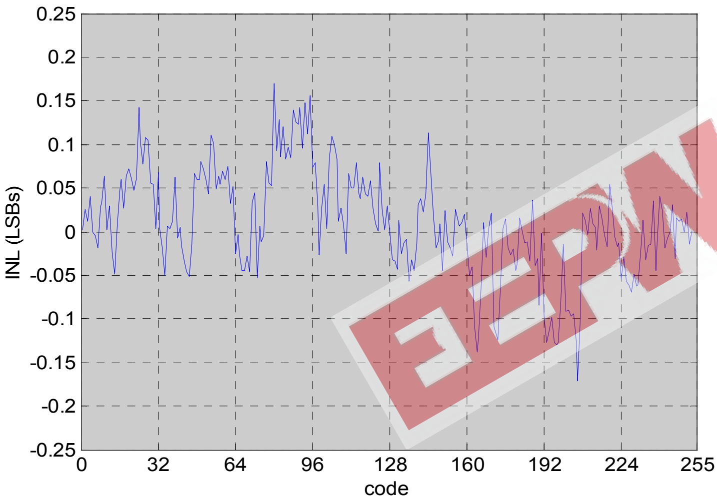


Figure 11. Integral Nonlinearity vs. Output Code

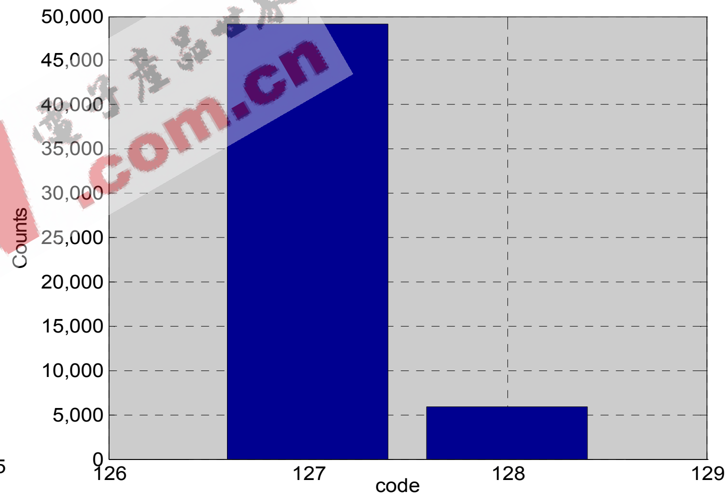


Figure 12. Noise Histogram

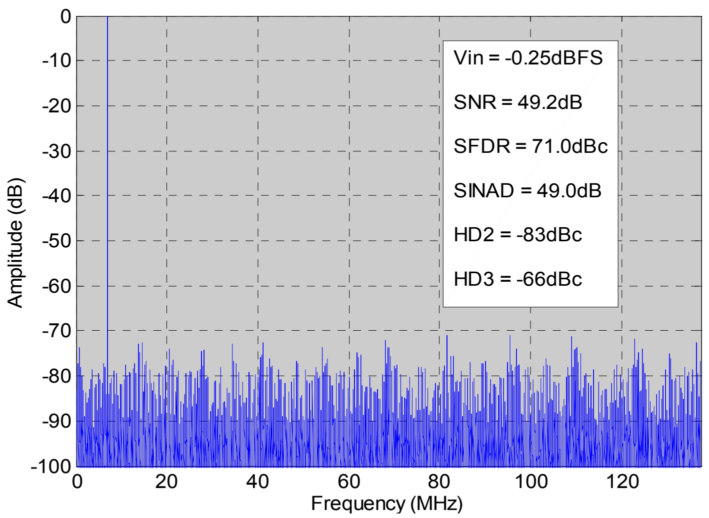


Figure 13. Output Spectrum at 6.865MHz

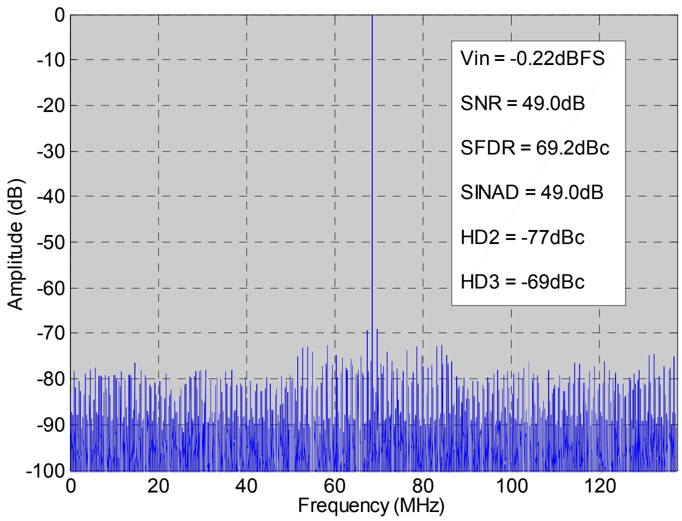


Figure 14. Output Spectrum at 68.465MHz

AVDD3=3.3V, AVDD2=OVDD2 =1.8V, $T_{AMBIENT}$ (T_A)=25°C, f_{SAMPLE}=275MHz unless noted.

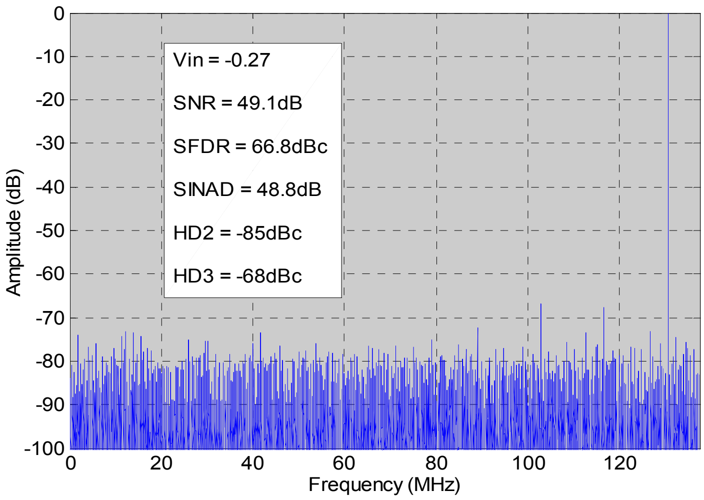


Figure 15. Output Spectrum at 130.565MHz

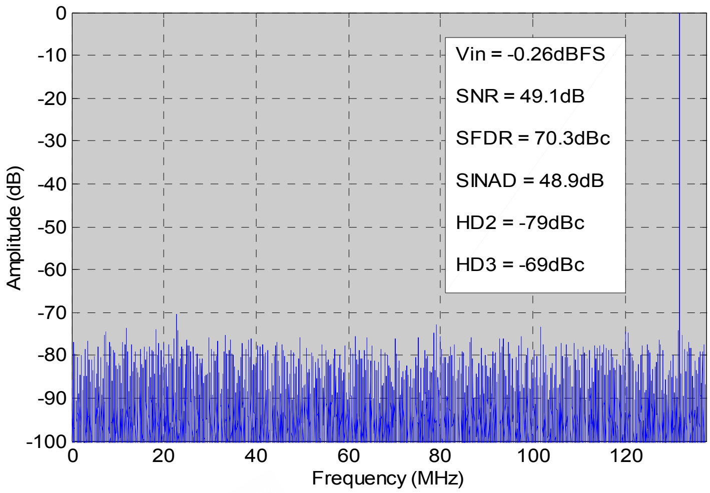


Figure 16. Output Spectrum at 143.155MHz

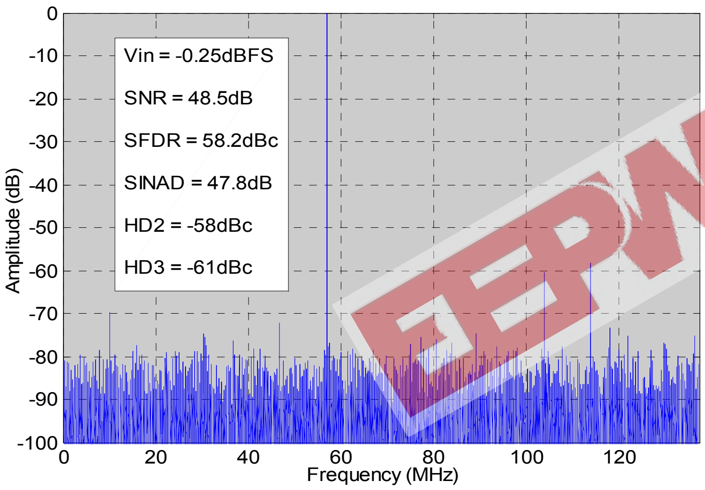


Figure 17. Output Spectrum at 492.965MHz

KAD2708C 8-Bit, 275MSPS Analog-to-Digital Converter

Functional Description

The KAD2708 is based upon a eight bit, 275MSPS A/D converter in a pipelined architecture. The input voltage is captured by a sample & hold circuit and converted to a unit of charge. Proprietary charge domain techniques are used to compare the input to a series of reference charges. These comparisons determine the digital code for each input value. The converter pipeline requires 24 sample clocks to produce a result. Digital error correction is also applied, resulting in a total latency of 28 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

At start-up, a self-calibration is performed to minimize gain and offset errors. The reset pin (RST) is initially held low internally at power-up and will remain in that state until the calibration is complete. The clock frequency should remain fixed during this time.

Calibration accuracy is maintained for the sample rate at which it is performed, and therefore should be repeated if the clock frequency is changed by more than 10%. Recalibration can be initiated via the RST pin, or power cycling, at any time.

Reset

The KAD2708C resets and calibrates automatically on power-up. To force a reset and initiate recalibration of the ADC after power-up, connect an open-drain output device to drive pin 28 (RST) and pull low for at least ten sample clock periods. Do not use a device with a pull-up on the reset pin, as it may prevent the KAD2708 from properly executing the power-on reset.

Voltage Reference

The VREF pin is the full-scale reference, which sets the full-scale input voltage for the chip and requires a bypass capacitor of 0.1uF or larger. An internally generated reference voltage is provided from a bandgap voltage buffer. This buffer can sink or source up to 50µA externally.

An external voltage may be applied to this pin to provide a more accurate reference than the internally generated bandgap voltage or to match the full-scale reference among a system of KAD2708C chips. One option in the latter configuration is to use one KAD2708C's internally generated reference as the external reference voltage for the other chips in the system. Additionally, an externally provided reference can be changed from the nominal value to adjust the full-scale input voltage within a limited range.

To select whether the full-scale reference is internally generated or externally provided, the digital input port VREFSEL should be set appropriately, low for internal or high for external. This pin also has an internal 18kΩ pull-up resistor. To use the internally generated reference VREFSEL can be tied directly to AVSS, and to use an external reference VREFSEL can be allowed to float.

Analog Input

The fully differential ADC input (INP/INN) connects to the sample and hold circuit. The ideal full-scale input voltage is $1.5V_{PP}$, centered at the VCM voltage of 0.86V as shown in Figure 18.

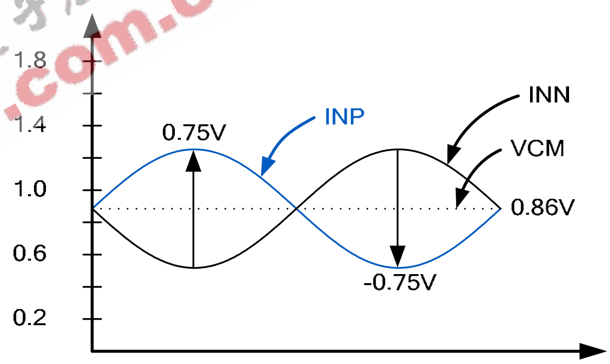


Figure 18. Analog Input Range

Best performance is obtained when the analog inputs are driven differentially in an ac-coupled configuration. The common mode output voltage, VCM, should be used to properly bias each input as shown in Figures 19 and 20. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. The recommended biasing is shown in Figure 19.

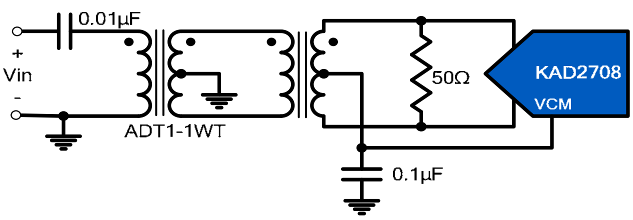


Figure 19. Transformer Input

The value of the termination resistor should be determined based on the desired impedance. The differential input impedance of the KAD2708 is 10MΩ.

A differential amplifier can be used in applications that require dc coupling, at the expense of reduced dynamic performance. In this configuration the amplifier will typically reduce the achievable SNR and distortion performance. A typical differential amplifier configuration is shown in Figure 20.

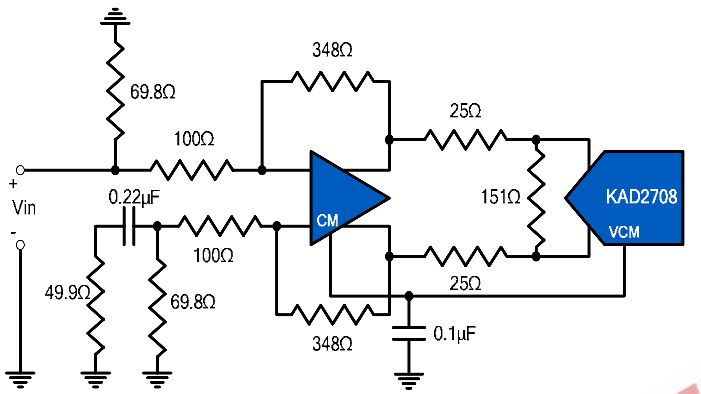


Figure 20. Differential Amplifier Input

Clock Input

The clock input circuit is a differential pair (see Figure 24). Driving these inputs with a high level (up to 1.8V_{PP} on each input) sine or square wave will provide the lowest jitter performance. The recommended drive circuit is shown in Figure 21. The clock inputs can be driven single-ended, but this is not recommended as performance will suffer.

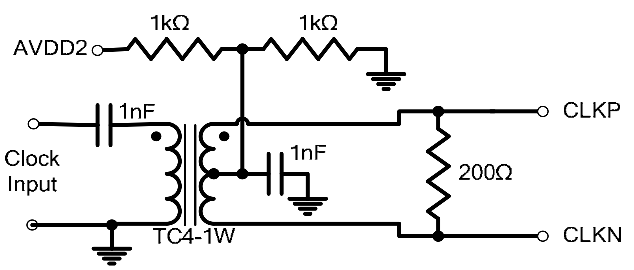


Figure 21. Recommended Clock drive

The CLKDIV pin is a 1.8V CMOS control pin (input) that selects whether the input clock frequency is passed directly to the ADC or divided by two. Applying a low level will divide by two; 1.8V applied (or left floating) will not divide.

Use of the clock divider is optional. The KAD2708C's ADC requires a clock with 50% duty cycle for optimum performance. If such a clock is not available, one option is to generate twice the desired sampling rate, then use the KAD2708C's divide-by-2 to generate a 50%-duty-cycle clock. The divider only uses the rising edge of the clock, so 50% clock duty cycle is assured .

CLKDIV Pin	Divide Ratio
AVSS	2
AVDD	1

Table 3. CLKDIV Pin Settings

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter and maximum SNR is shown in Equation 1 and is illustrated in Figure 22.

$$SNR = 20\log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right)$$

Where tj is the RMS uncertainty in the sampling instant.

Equation 1.

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as differential nonlinearity, aperture jitter and thermal noise.

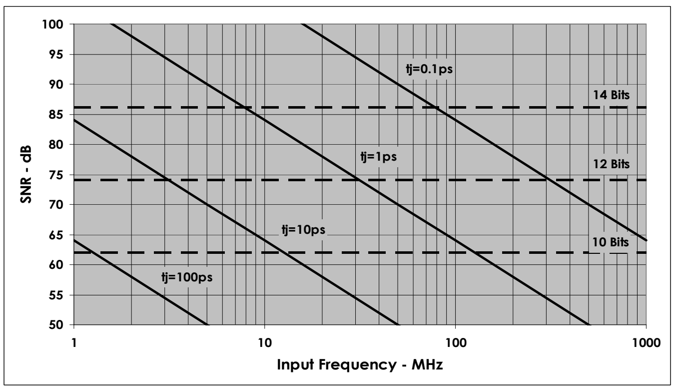


Figure 22. SNR vs. Clock Jitter

Any internal aperture jitter combines with the input clock jitter, in a root-sum-square fashion since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Equivalent Circuits

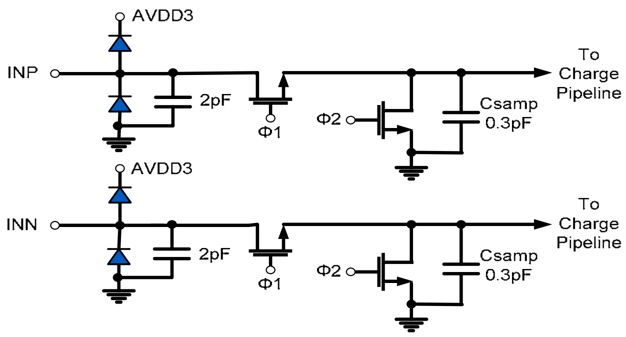


Figure 23. Analog Inputs

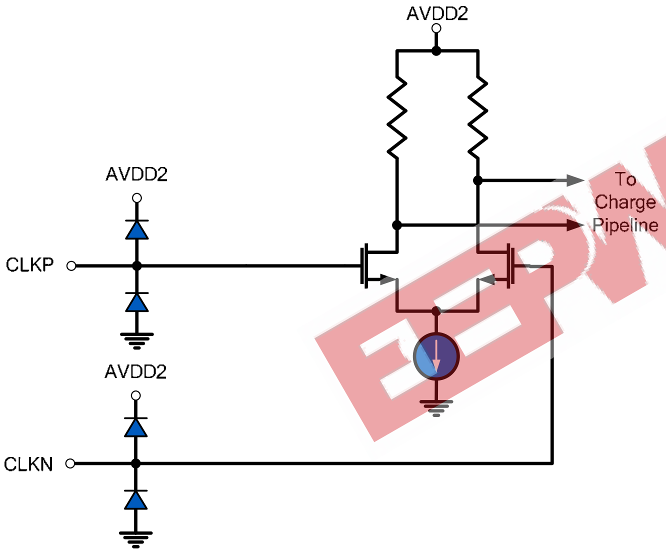


Figure 24. Clock Inputs

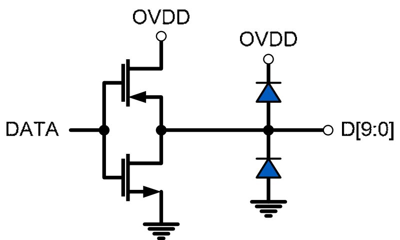


Figure 25. LVCMOS Outputs

Layout Considerations

Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

Clock Input Considerations

Use matched transmission lines to the inputs for the analog input and clock signals. Locate transformers, drivers and terminations as close to the chip as possible.

Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins. Longer traces will increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

LVCMOS Outputs

Output traces and connections must be designed for 50Ω characteristic impedance.

Unused Inputs

Three of the four standard logic inputs (RESET, CLKDIV, 2SC) which will not be operated do not require connection for best ADC performance. These inputs can be left open if they are not used. VREFSEL must be held low for internal reference, but can be left open for external reference.

Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.

Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD-1.76) / 6.02.

Integral Non-Linearity (INL) is the deviation of each individual code from a line drawn from negative full-scale (1/2 LSB below the first code transition) through positive full-scale (1/2 LSB above the last code transition). The deviation of any given code from this line is measured from the center of that code.

Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is VFS/(2N-1) where N is the resolution in bits.

Missing Codes are output codes that are skipped and will never appear at the ADC output. These codes cannot be reached with any input value.

Most Significant Bit (MSB) is the bit that has the largest value or weight. Its value in terms of input voltage is VFS/2.

Pipeline Delay is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the corresponding data.

Power Supply Rejection Ratio (PSRR) is the ratio of a change in power supply voltage to the input voltage necessary to negate the resultant change in output code.

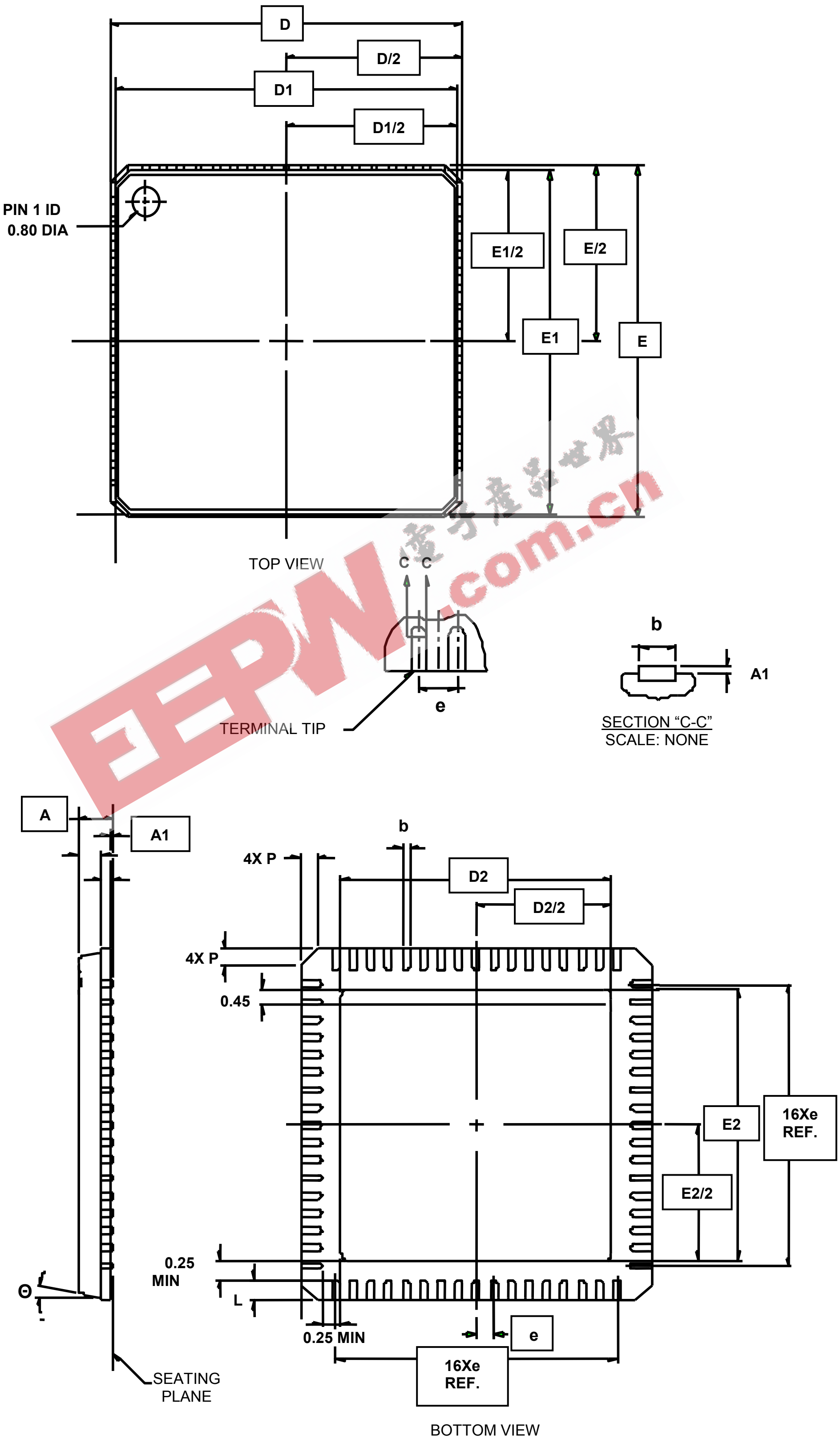
Signal to Noise-and-Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS value of the sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

Signal-to-Noise Ratio (without Harmonics) is the ratio of the RMS signal amplitude to the sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral component. The peak spurious spectral component may or may not be a harmonic.

Two-Tone SFDR is the ratio of the RMS value of either input tone to the RMS value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Outline Dimensions



Package Dimensions (mm)

Ref	Min	Nom	Max	Note
A	-	0.90	1.00	
A1	0.00	0.01	0.05	Per JEDEC MO-220
b	0.18	0.23	0.30	Measured between 0.20 and 0.25mm from plated terminal tip
D		10.00 BSC		
D1		9.75 BSC		
D2	7.55	7.70	7.85	
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
E2	7.55	7.70	7.85	
L	0.50	0.60	0.65	
N		68		Total terminals
N_D		17		Terminals in D (x) direction
N_E		17		Terminals in E (y) direction
Θ	0		12’	
P	0	0.42	0.60	

Ordering Guide

This product is compliant with EU directive 2002/95/EC regarding the Restriction of Hazardous Substances (RoHS). Contact Kenet for a materials declaration for this product.

Model	Speed	Package	Temp. Range
KAD2708C-27Q68	275MSPS	68-QFN EP	-40°C to +85°C
KAD2708C-21Q68	210MSPS	68-QFN EP	-40°C to +85°C
KAD2710C-17Q68	170MSPS	68-QFN EP	-40°C to +85°C
KAD2710C-10Q68	105MSPS	68-QFN EP	-40°C to +85°C