FUJITSU MICROELECTRONICS
DATA SHEET

DS07-12610-3Ea

8-bit Microcontrollers

CMOS

F²MC-8FX MB95120MB series

MB95128MB/F124MB/F124NB/F124JB/F126MB/F126NB/ MB95F126JB/F128MB/F128NB/F128JB/FV100D-103

■ DESCRIPTION

The MB95120MB series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURE

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock
  - Sub PLL clock
- Timer
  - 8/16-bit compound timer × 2 channels
    - Can be used to interval timer, PWC timer, PWM timer and input capture.
  - 16-bit reload timer × 1 channel
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG × 2 channels

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://edevice.fujitsu.com/micom/en-support/

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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- Timebase timer × 1 channel
- Watch prescaler × 1 channel

- LIN-UART × 1 channel
  - LIN function, clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- UART/SIO × 1 channel
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
  - Full duplex double buffer
- I^2C* × 1 channel
  - Built-in wake-up function
- External interrupt × 12 channels
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter × 12 channels
  - 8-bit or 10-bit resolution can be selected
- LCD controller (LCDC)
  - 40 SEG × 4 COM (Max 160 pixels)
  - With blinking function
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode
  - Timebase timer mode
- I/O port
  - The number of maximum ports : Max 87
  - Port configuration
    - General-purpose I/O ports (N-ch open drain) : 2 ports
    - General-purpose I/O ports (CMOS) : 85 ports
- Programmable input voltage levels of port
  Automotive input level / CMOS input level / hysteresis input level
- Dual operation Flash memory
  - Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.
- Flash memory security function
  Protects the content of Flash memory (Flash memory device only)

* : Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent Rights to use, these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

■ MEMORY LINEUP

	Flash memory	RAM
MB95F124MB	16 Kbytes	512 bytes
MB95F124NB		
MB95F124JB		
MB95F126MB	32 Kbytes	1 Kbyte
MB95F126NB		
MB95F126JB		
MB95F128MB	60 Kbytes	2 Kbytes
MB95F128NB		
MB95F128JB		

■ PRODUCT LINEUP

Parameter \ Part number		MB95128MB	MB95F124MB MB95F126MB MB95F128MB	MB95F124NB MB95F126NB MB95F128NB	MB95F124JB MB95F126JB MB95F128JB
Type		MASK ROM product	Flash memory product		
ROM capacity*1		60 Kbytes (Max)			
RAM capacity*1		2 Kbytes (Max)			
Reset output		Yes/No	Yes		No
Option*2	Clock system	Dual clock			
	Low voltage detection reset	Yes/No	No	Yes	
	Clock supervisor	Yes/No	No		Yes
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 µs (at machine clock frequency 16.25 MHz)			
Peripheral functions	Ports (Max 87 ports)	General-purpose I/O port (N-ch open drain) : 2 ports General-purpose I/O port (CMOS) : 85 ports Programmable input voltage levels of port : Automotive input level / CMOS input level / hysteresis input level			
	Timebase timer (1 channel)	Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)			
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Min 105 ms At sub oscillation clock 32.768 kHz : Min 250 ms			
	Wild register	Capable of replacing 3 bytes of ROM data			
	I^2C (1 channel)	Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function			
	UART/SIO (1 channel)	Data transfer capable in UART/SIO Full duplex double buffer Variable data length (5/6/7/8-bit), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable			
	LIN-UART (1 channel)	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable LIN functions available as the LIN master or LIN slave.			
	8/10-bit A/D converter (12 channels)	8-bit or 10-bit resolution can be selected.			

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Parameter \ Part number		MB95128MB	MB95F124MB MB95F126MB MB95F128MB	MB95F124NB MB95F126NB MB95F128NB	MB95F124JB MB95F126JB MB95F128JB
Peripheral functions	LCD controller (LCDC)	COM output : 4 (Max) SEG output : 40 (Max) LCD drive power supply (bias) pin : 4 (Max) 40 SEG × 4 COM : 160 pixels can be displayed. Duty LCD mode Operable in LCD standby mode With blinking function Built-in division resistance for LCD drive			
	16-bit reload timer (1 channel)	Two clock modes and two counter operating modes can be selected. Square waveform output Count clock : 7 internal clocks and external clock can be selected. Counter operating mode : reload mode or one-shot mode can be selected.			
	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as "8-bit timer × 2 channels" or "16-bit timer × 1 channel". Built-in timer function, PWC function, PWM function, capture function and square waveform output Count clock : 7 internal clocks and external clock can be selected.			
	16-bit PPG (2 channels)	PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start			
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as "8-bit PPG × 2 channels" or "16-bit PPG × 1 channel". Counter operating clock : Eight selectable clock sources			
	Watch counter	Count clock : Four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63 (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60) .			
	Watch prescaler (1 channel)	4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)			
	External interrupt (12 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.			
Flash memory		Supports automatic programming, Embedded Algorithm™ *3 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time : 20 years Erase can be performed on each block Block protection with external programming voltage Dual operation Flash memory Flash Security Feature for protecting the content of the Flash			
Standby mode		Sleep, stop, watch, and timebase timer			

*1 : For ROM capacitance and RAM capacitance, refer to "■ MEMORY LINEUP".

*2 : For details of option, refer to "■ MASK OPTION".

*3 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

Note : Part number of evaluation product in MB95120MB series is MB95FV100D-103. When using it, the MCU board (MB2146-303A) is required.

■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value. The maximum value is shown as follows.

Oscillation stabilization wait time	Remarks
$(2^{14}-2)/F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95128MB	MB95F124MB/F124NB/F124JB MB95F126MB/F126NB/F126JB MB95F128MB/F128NB/F128JB	MB95FV100D-103
FPT-100P-M20	○	○	×
FPT-100P-M06	○	○	×
BGA-224P-M08	×	×	○

○ : Available
× : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

• Notes on Using Evaluation Products

The Evaluation product has not only the functions of the MB95120MB series but also those of other products to support software development for multiple series and models of the F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95120MB series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the Flash memory and MASK ROM products, do not use these values in the program.

The Evaluation product do not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. Since the Evaluation, Flash memory product, and MASK ROM product are designed to behave completely the same way in terms of hardware and software.

• Difference of Memory Spaces

If the amount of memory on the Evaluation product is different from that of the Flash memory product or MASK ROM product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

For details of memory space, refer to “■ CPU CORE”.

• Current Consumption

- The current consumption of Flash memory product is typically greater than for MASK ROM product.
- For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

• Package

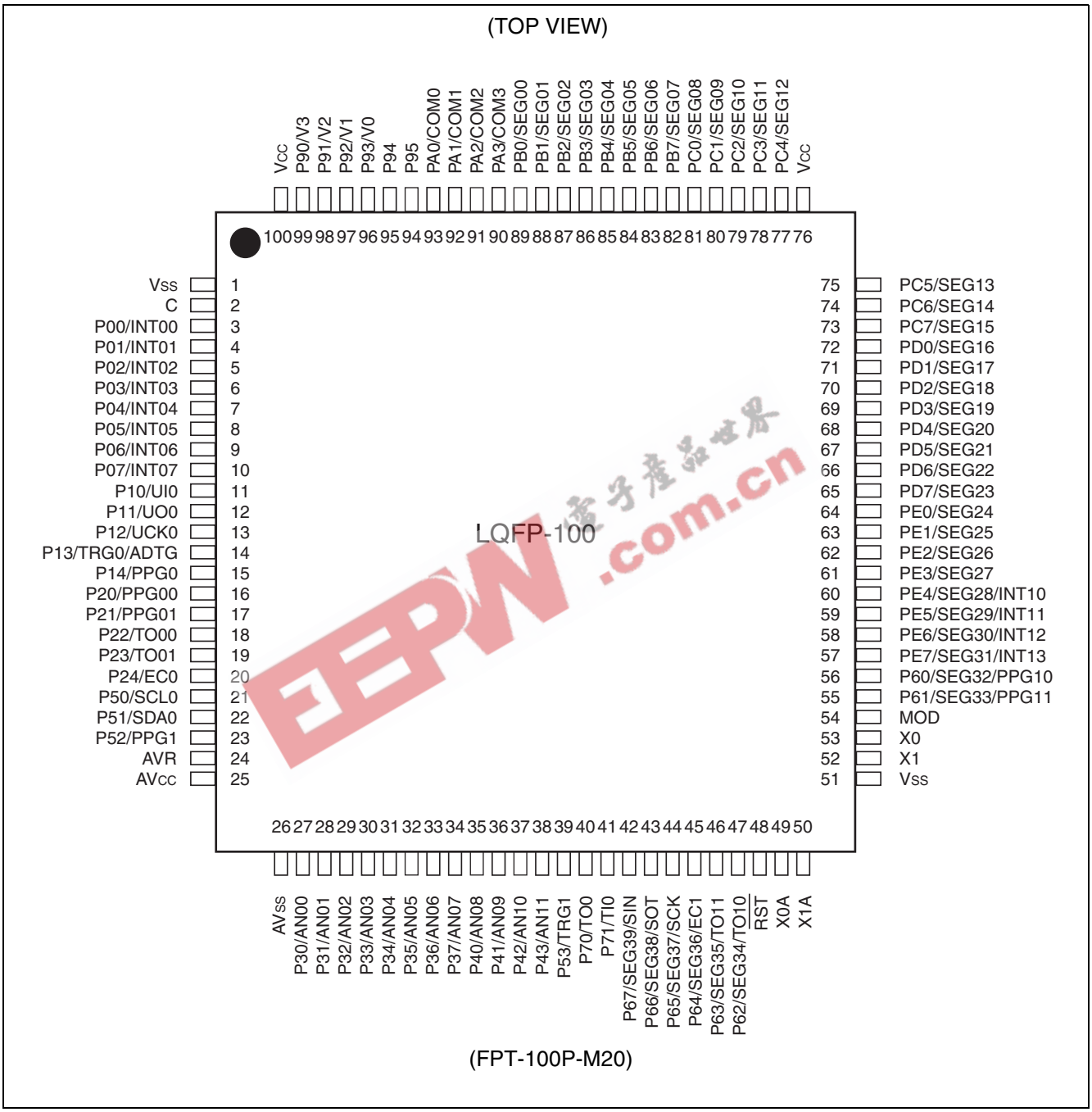
For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

• Operating voltage

The operating voltage are different between the Evaluation, Flash memory products, and MASK ROM product.

For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”.

■ PIN ASSIGNMENT



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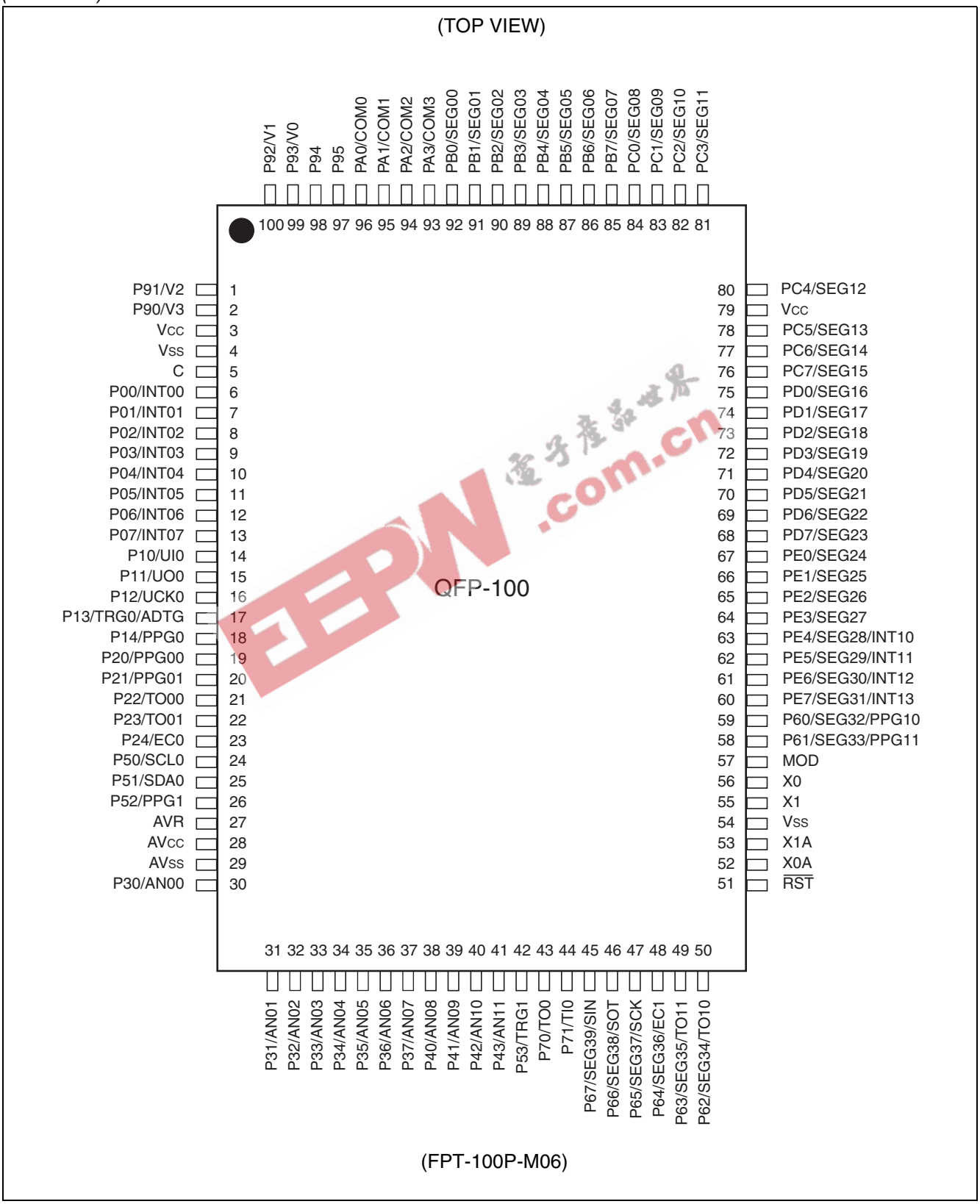
(TOP VIEW)
P92/V1 100
P93/V0 99
P94 98
P95 97
PA0/COM0 96
PA1/COM1 95
PA2/COM2 94
PA3/COM3 93
PB0/SEG00 92
PB1/SEG01 91
PB2/SEG02 90
PB3/SEG03 89
PB4/SEG04 88
PB5/SEG05 87
PB6/SEG06 86
PB7/SEG07 85
PC0/SEG08 84
PC1/SEG09 83
PC2/SEG10 82
PC3/SEG11 81
P91/V2 1
P90/V3 2
VCC 3
VSS 4
C 5
P00/INT00 6
P01/INT01 7
P02/INT02 8
P03/INT03 9
P04/INT04 10
P05/INT05 11
P06/INT06 12
P07/INT07 13
P10/UI0 14
P11/UO0 15
P12/UCK0 16
P13/TRG0/ADTG 17
P14/PPG0 18
P20/PPG00 19
P21/PPG01 20
P22/TO00 21
P23/TO01 22
P24/EC0 23
P50/SCL0 24
P51/SDA0 25
P52/PPG1 26
AVR 27
AVCC 28
AVSS 29
P30/AN00 30
QFP-100
80 PC4/SEG12
79 VCC
78 PC5/SEG13
77 PC6/SEG14
76 PC7/SEG15
75 PD0/SEG16
74 PD1/SEG17
73 PD2/SEG18
72 PD3/SEG19
71 PD4/SEG20
70 PD5/SEG21
69 PD6/SEG22
68 PD7/SEG23
67 PE0/SEG24
66 PE1/SEG25
65 PE2/SEG26
64 PE3/SEG27
63 PE4/SEG28/INT10
62 PE5/SEG29/INT11
61 PE6/SEG30/INT12
60 PE7/SEG31/INT13
59 P60/SEG32/PPG10
58 P61/SEG33/PPG11
57 MOD
56 X0
55 X1
54 VSS
53 X1A
52 X0A
51 RST
31 P31/AN01
32 P32/AN02
33 P33/AN03
34 P34/AN04
35 P35/AN05
36 P36/AN06
37 P37/AN07
38 P40/AN08
39 P41/AN09
40 P42/AN10
41 P43/AN11
42 P53/TRG1
43 P70/TO0
44 P71/TI0
45 P67/SEG39/SIN
46 P66/SEG38/SOT
47 P65/SEG37/SCK
48 P64/SEG36/EC1
49 P63/SEG35/TO11
50 P62/SEG34/TO10
(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
1	4	V_{SS}	—	Power supply pin (GND)
2	5	C	—	Capacitor connection pin
3	6	P00/INT00	C	General-purpose I/O port The pins are shared with external interrupt input. Large current port.
4	7	P01/INT01		
5	8	P02/INT02		
6	9	P03/INT03		
7	10	P04/INT04		
8	11	P05/INT05		
9	12	P06/INT06		
10	13	P07/INT07		
11	14	P10/UI0	G	General-purpose I/O port The pin is shared with UART/SIO ch.0 data input.
12	15	P11/UO0	H	General-purpose I/O port The pin is shared with UART/SIO ch.0 data output.
13	16	P12/UCK0		General-purpose I/O port The pin is shared with UART/SIO ch.0 clock I/O.
14	17	P13/TRG0/ ADTG		General-purpose I/O port The pin is shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG).
15	18	P14/PPG0		General-purpose I/O port The pin is shared with 16-bit PPG ch.0 output.
16	19	P20/PPG00	H	General-purpose I/O port The pins are shared with 8/16-bit PPG ch.0 output.
17	20	P21/PPG01		
18	21	P22/TO00		General-purpose I/O port The pins are shared with 8/16-bit compound timer ch.0 output.
19	22	P23/TO01		
20	23	P24/EC0		General-purpose I/O port The pin is shared with 8/16-bit compound timer ch.0 clock input.
21	24	P50/SCL0	I	General-purpose I/O port The pin is shared with I^2C ch.0 clock I/O.
22	25	P51/SDA0		General-purpose I/O port The pin is shared with I^2C ch.0 data I/O.
23	26	P52/PPG1	H	General-purpose I/O port The pin is shared with 16-bit PPG ch.1 output.
24	27	AVR	—	A/D converter reference input pin
25	28	AV_{CC}	—	A/D converter power supply pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
26	29	AV_{SS}	—	A/D converter power supply pin (GND)
27	30	P30/AN00	J	General-purpose I/O port The pins are shared with A/D converter analog input.
28	31	P31/AN01		
29	32	P32/AN02		
30	33	P33/AN03		
31	34	P34/AN04		
32	35	P35/AN05		
33	36	P36/AN06		
34	37	P37/AN07		
35	38	P40/AN08	J	General-purpose I/O port The pins are shared with A/D converter analog input.
36	39	P41/AN09		
37	40	P42/AN10		
38	41	P43/AN11		
39	42	P53/TRG1	H	General-purpose I/O port The pin is shared with 16-bit PPG ch.1 trigger input.
40	43	P70/TO0	H	General-purpose I/O port The pin is shared with 16-bit reload timer ch.0 output.
41	44	P71/TI0		General-purpose I/O port The pin is shared with 16-bit reload timer ch.0 input.
42	45	P67/SEG39/ SIN	N	General-purpose I/O port The pin is shared with LCDC SEG output (SEG39) and LIN-UART data input (SIN) .
43	46	P66/SEG38/ SOT	M	General-purpose I/O port The pin is shared with LCDC SEG output (SEG38) and LIN-UART data output (SOT) .
44	47	P65/SEG37/ SCK		General-purpose I/O port The pin is shared with LCDC SEG output (SEG37) and LIN-UART clock I/O (SCK) .
45	48	P64/SEG36/ EC1		General-purpose I/O port The pin is shared with LCDC SEG output (SEG36) and 8/16-bit compound timer ch.1 clock input (EC1) .
46	49	P63/SEG35/ TO11		General-purpose I/O port The pins are shared with LCDC SEG output (SEG34, SEG35) and 8/16-bit compound timer ch.1 output (TO10, TO11) .
47	50	P62/SEG34/ TO10		
48	51	$\overline{RST}$	B'	Reset pin
49	52	X0A	A	Sub clock oscillation pin (32 kHz)
50	53	X1A		
51	54	V_{SS}	—	Power supply pin (GND)

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
52	55	X1	A	Main clock oscillation pin
53	56	X0		
54	57	MOD	B	An operating mode designation pin
55	58	P61/SEG33/ PPG11	M	General-purpose I/O port The pins are shared with LCDC SEG output (SEG32, SEG33) and 8/16-bit PPG ch.1 output (PPG10, PPG11) .
56	59	P60/SEG32/ PPG10		
57	60	PE7/SEG31/ INT13	Q	General-purpose I/O port The pins are shared with LCDC SEG output (SEG28 to SEG31) and external interrupt input (INT10 to INT13) .
58	61	PE6/SEG30/ INT12		
59	62	PE5/SEG29/ INT11		
60	63	PE4/SEG28/ INT10		
61	64	PE3/SEG27	M	General-purpose I/O port The pins are shared with LCDC SEG output (SEG24 to SEG27) .
62	65	PE2/SEG26		
63	66	PE1/SEG25		
64	67	PE0/SEG24		
65	68	PD7/SEG23	M	General-purpose I/O port The pins are shared with LCDC SEG output (SEG16 to SEG23) .
66	69	PD6/SEG22		
67	70	PD5/SEG21		
68	71	PD4/SEG20		
69	72	PD3/SEG19		
70	73	PD2/SEG18		
71	74	PD1/SEG17		
72	75	PD0/SEG16		
73	76	PC7/SEG15	M	General-purpose I/O port The pins are shared with LCDC SEG output (SEG13 to SEG15) .
74	77	PC6/SEG14		
75	78	PC5/SEG13		
76	79	V_{CC}	—	Power supply pin

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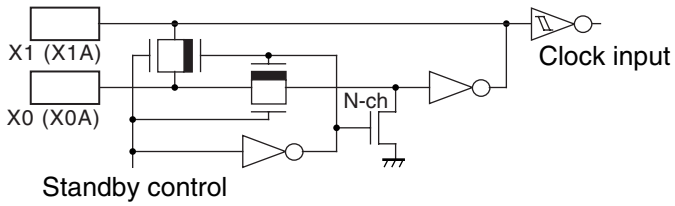
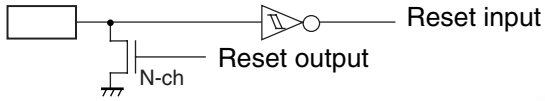
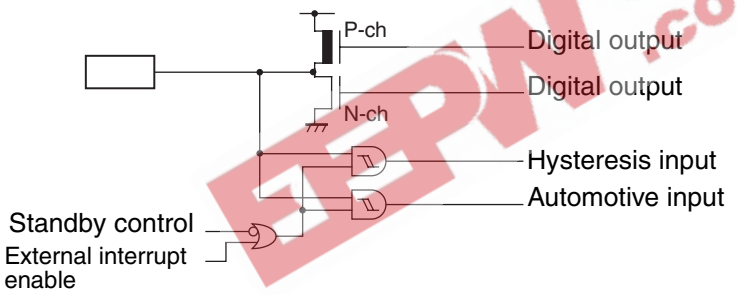
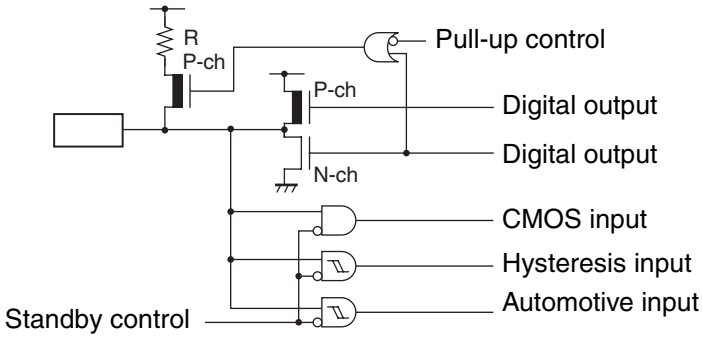
Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
77	80	PC4/SEG12	M	General-purpose I/O port The pins are shared with LCDC SEG output (SEG08 to SEG12) .
78	81	PC3/SEG11		
79	82	PC2/SEG10		
80	83	PC1/SEG09		
81	84	PC0/SEG08		
82	85	PB7/SEG07	M	General-purpose I/O port The pins are shared with LCDC SEG output (SEG00 to SEG07) .
83	86	PB6/SEG06		
84	87	PB5/SEG05		
85	88	PB4/SEG04		
86	89	PB3/SEG03		
87	90	PB2/SEG02		
88	91	PB1/SEG01		
89	92	PB0/SEG00		
90	93	PA3/COM3	M	General-purpose I/O port The pins are shared with LCDC COM output (COM0 to COM3) .
91	94	PA2/COM2		
92	95	PA1/COM1		
93	96	PA0/COM0		
94	97	P95	M	General-purpose I/O port
95	98	P94		
96	99	P93/V0	R	General-purpose I/O port The pins are shared with power supply pins for LCDC drive.
97	100	P92/V1		
98	1	P91/V2		
99	2	P90/V3		
100	3	V_{CC}	—	Power supply pin

*1 : FPT-100P-M20

*2 : FPT-100P-M06

*3 : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation circuit • High-speed side Feedback resistance : approx. 1 MΩ • Low-speed side Feedback resistance : approx. 10 MΩ
B		• Only for input • Hysteresis input
B’		• Reset output • Hysteresis input
C		• CMOS output • Hysteresis input • Automotive input
G		• CMOS output • CMOS input • Hysteresis input • With pull-up control • Automotive input

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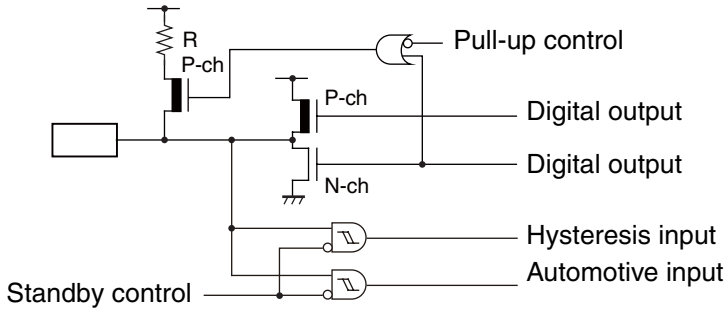
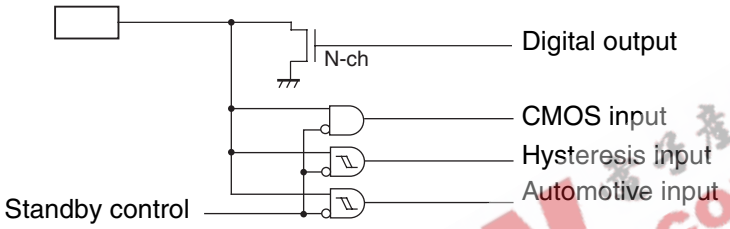
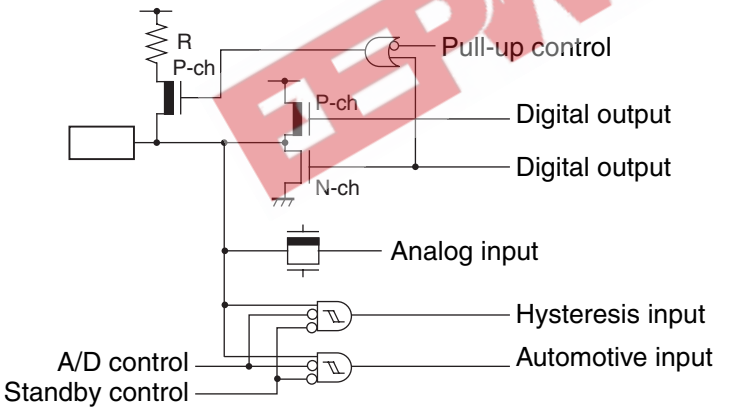
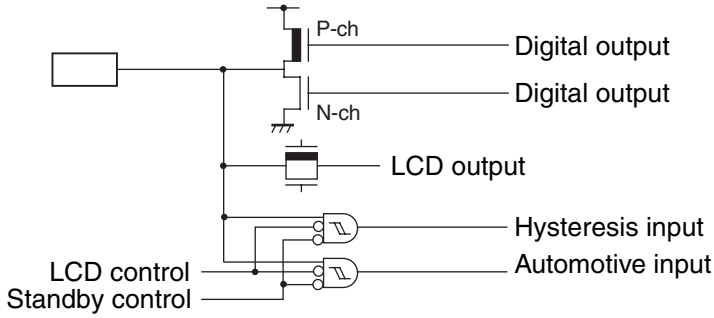
Type	Circuit	Remarks
H		• CMOS output • Hysteresis input • With pull-up control • Automotive input
I		• N-ch open drain output • CMOS input • Hysteresis input • Automotive input
J		• CMOS output • Hysteresis input • Analog input • With pull-up control • Automotive input
M		• CMOS output • LCD output • Hysteresis input • Automotive input

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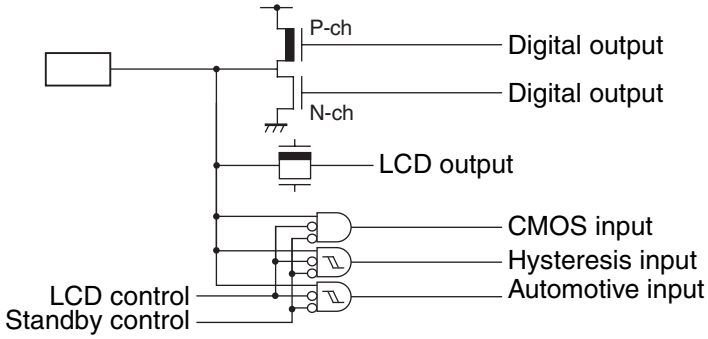
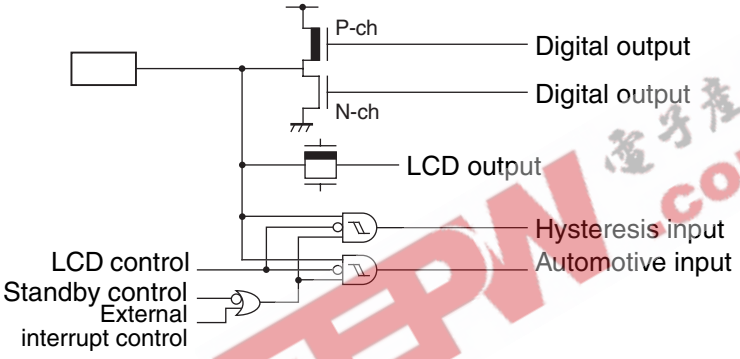
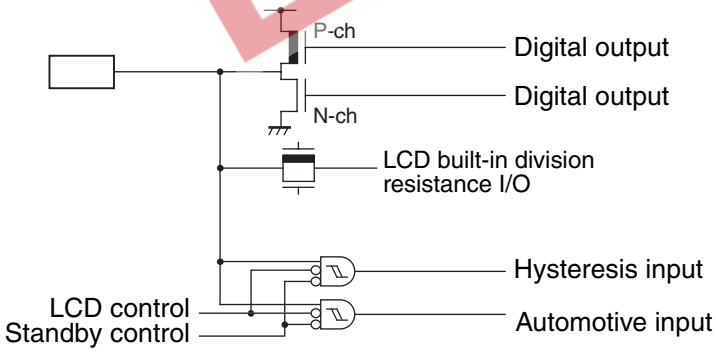
Type	Circuit	Remarks
N		• CMOS output • LCD output • CMOS input • Hysteresis input • Automotive input
Q		• CMOS output • LCD output • Hysteresis input • Automotive input
R		• CMOS output • LCD power supply • Hysteresis input • Automotive input

■ HANDLING DEVICES

• Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage (AV_{CC} , AVR) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

• Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the V_{CC} power-supply voltage.

For stabilization, in principle, keep the variation in V_{CC} ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard V_{CC} value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

• Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

PIN CONNECTION

• Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage.

Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it open.

• Treatment of Power Supply Pins on A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converter is not in use.

Noise riding on the AV_{CC} pin may cause accuracy degradation. So, connect approx. 0.1 µF ceramic capacitor as a bypass capacitor between AV_{CC} and AV_{SS} pins in the vicinity of this device.

• Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS} near this device.

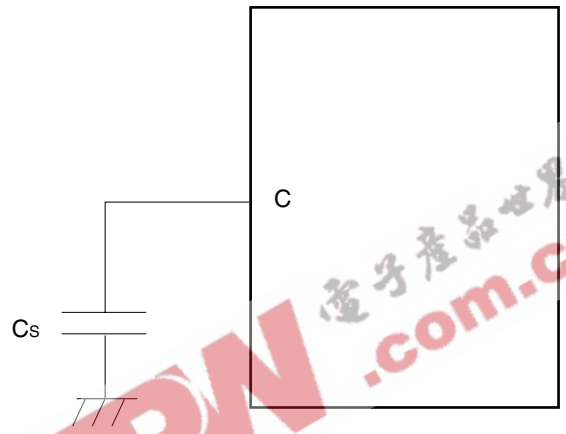
• Mode Pin (MOD)

Connect the MOD pin directly to V_{CC} or V_{SS} pins.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitance value higher than C_S. For connection of smoothing capacitor C_S, refer to the diagram below.

• C pin connection diagram



• Analog Power Supply

Always set the same potential to AV_{CC} and V_{CC} pins. When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN11 pins.

■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported Parallel Programmers and Adapters

The following table lists supported parallel programmers and adapters.

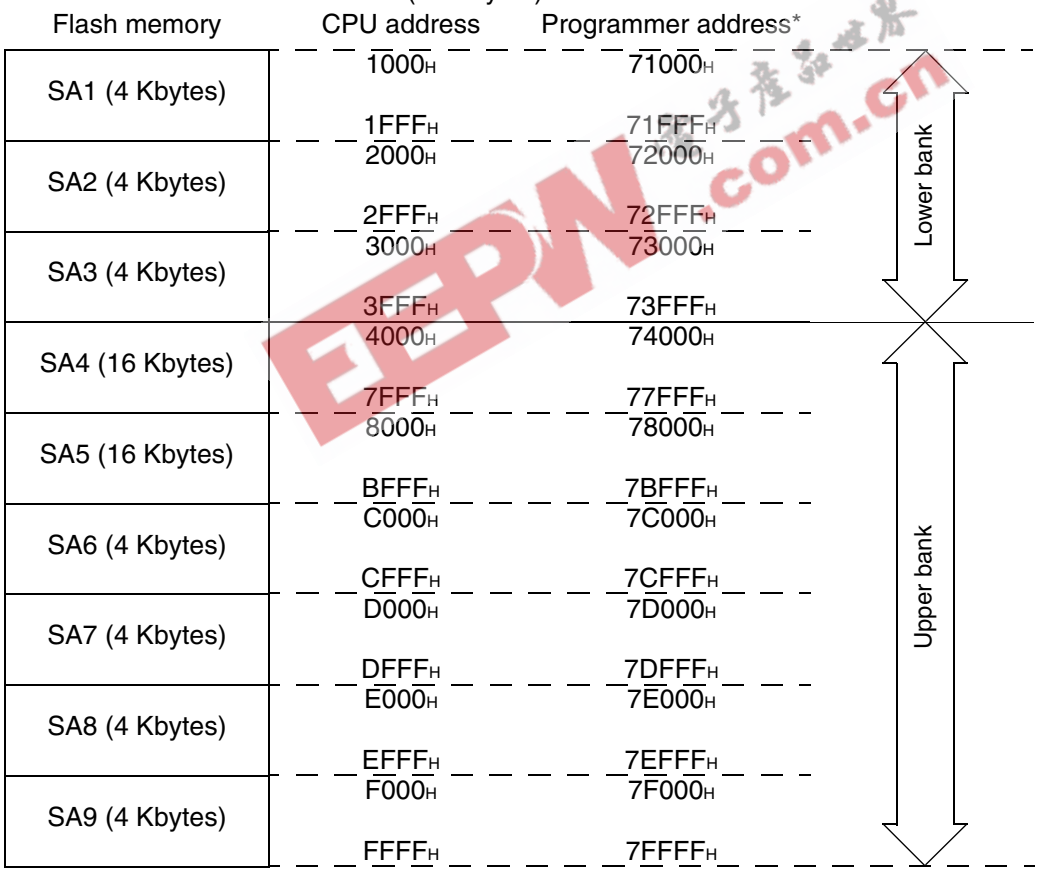
Package	Applicable adapter model	Parallel programmers
FPT-100P-M20	TEF110-95F128HSPFV	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more) AF9723+AF9834 (Ver 02.08E or more)
FPT-100P-M06	TEF110-95F128HSPF	

Note : For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

• Sector Configuration

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

• MB95F128MB/F128NB/F128JB (60 Kbytes)



*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• Programming Method

1) Set the type code of the parallel programmer to 17222.

2) Load program data to programmer addresses 71000H to 7FFFFH.

3) Programmed by parallel programmer

• MB95F126MB/F126NB/F126JB (32 Kbytes)

Flash memory	CPU address	Programmer address*
SA5 (16 Kbytes)	8000H	78000H
	BFFFH	7BFFFH
SA6 (4 Kbytes)	C000H	7C000H
	CFFFH	7CFFFH
SA7 (4 Kbytes)	D000H	7D000H
	DFFFH	7DFFFH
SA8 (4 Kbytes)	E000H	7E000H
	EFFFH	7EFFFH
SA9 (4 Kbytes)	F000H	7F000H
	FFFFH	7FFFFH

*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

• **Programming Method**

1) Set the type code of the parallel programmer to 17222.

2) Load program data to programmer addresses 78000H to 7FFFFH.

3) Programmed by parallel programmer

• MB95F124MB/F124NB/F124JB (16 Kbytes)

Flash memory	CPU address	Programmer address*
SA6 (4 Kbytes)	C000H	7C000H
	CFFFH	7CFFFH
SA7 (4 Kbytes)	D000H	7D000H
	DFFFH	7DFFFH
SA8 (4 Kbytes)	E000H	7E000H
	EFFFH	7EFFFH
SA9 (4 Kbytes)	F000H	7F000H
	FFFFH	7FFFFH

*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

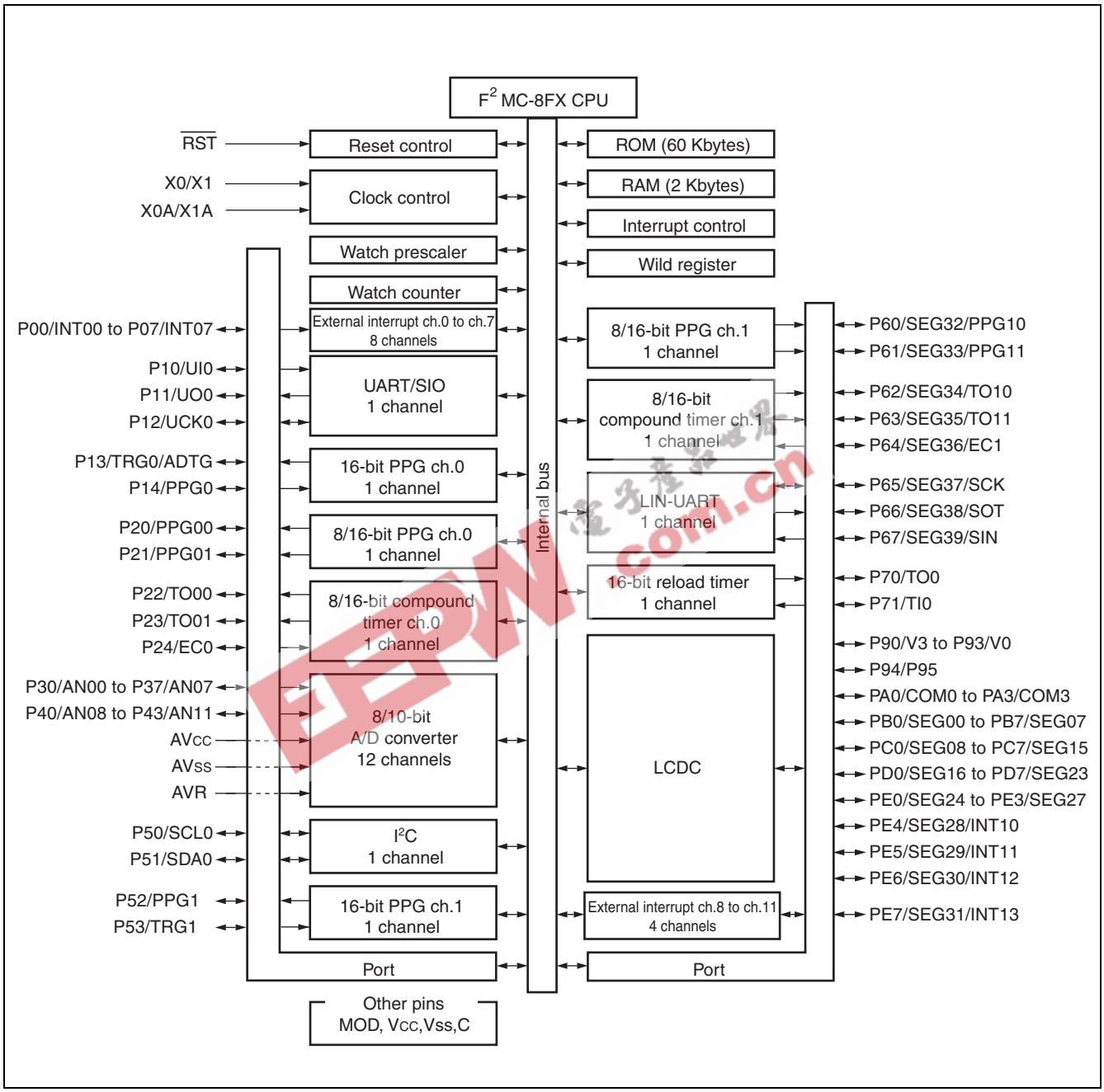
• **Programming Method**

1) Set the type code of the parallel programmer to 17222.

2) Load program data to programmer addresses 7C000H to 7FFFFH.

3) Programmed by parallel programmer

■ BLOCK DIAGRAM

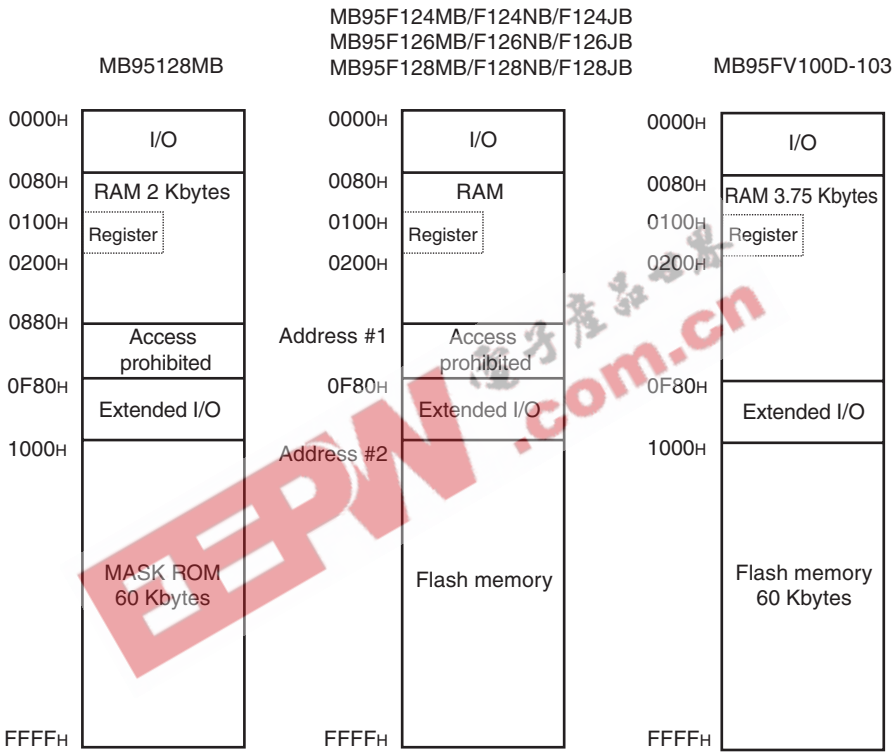


■ CPU CORE

1. Memory space

Memory space of the MB95120MB series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special - purpose areas such as the general - purpose registers and vector table. Memory map of the MB95120MB series is shown below.

• Memory Map

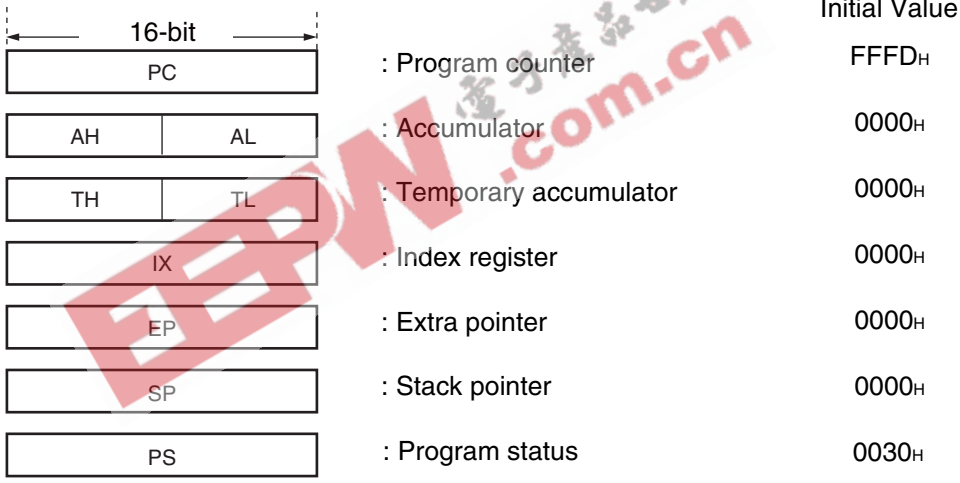


	Flash memory	RAM	Address #1	Address #2
MB95F124MB	16 Kbytes	512 bytes	0280H	C000H
MB95F124NB				
MB95F124JB				
MB95F126MB	32 Kbytes	1 Kbyte	0480H	8000H
MB95F126NB				
MB95F126JB				
MB95F128MB	60 Kbytes	2 Kbytes	0880H	1000H
MB95F128NB				
MB95F128JB				

2. Register

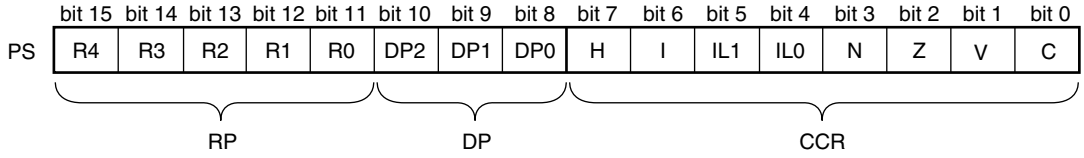
The MB95120MB series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

Program counter (PC)	:	A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	:	A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
Index register (IX)	:	A 16-bit register for index modification
Extra pointer (EP)	:	A 16-bit pointer to point to a memory address.
Stack pointer (SP)	:	A 16-bit register to indicate a stack area.
Program status (PS)	:	A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register



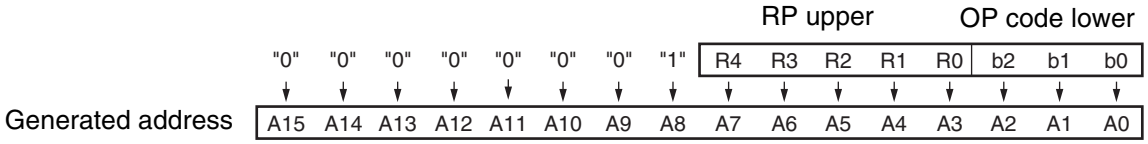
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR) . (Refer to the diagram below.)

• Structure of the program status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

• Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080_H to $00FF_H$.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX_B (no effect to mapping)	0000_H to $007F_H$	0000_H to $007F_H$ (without mapping)
000_B (initial value)	0080_H to $00FF_H$	0080_H to $00FF_H$ (without mapping)
001_B		0100_H to $017F_H$
010_B		0180_H to $01FF_H$
011_B		0200_H to $027F_H$
100_B		0280_H to $02FF_H$
101_B		0300_H to $037F_H$
110_B		0380_H to $03FF_H$
111_B		0400_H to $047F_H$

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when this flag is set to “0”. The flag is cleared to “0” when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

IL1	IL0	Interrupt level	Priority
0	0	0	High
0	1	1	↕
1	0	2	↕
1	1	3	Low (no interruption)

N flag : Set to “1” if the MSB is set to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is set to “0”.

Z flag : Set to “1” when an arithmetic operation results in “0”. Cleared to “0” otherwise.

V flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” otherwise.

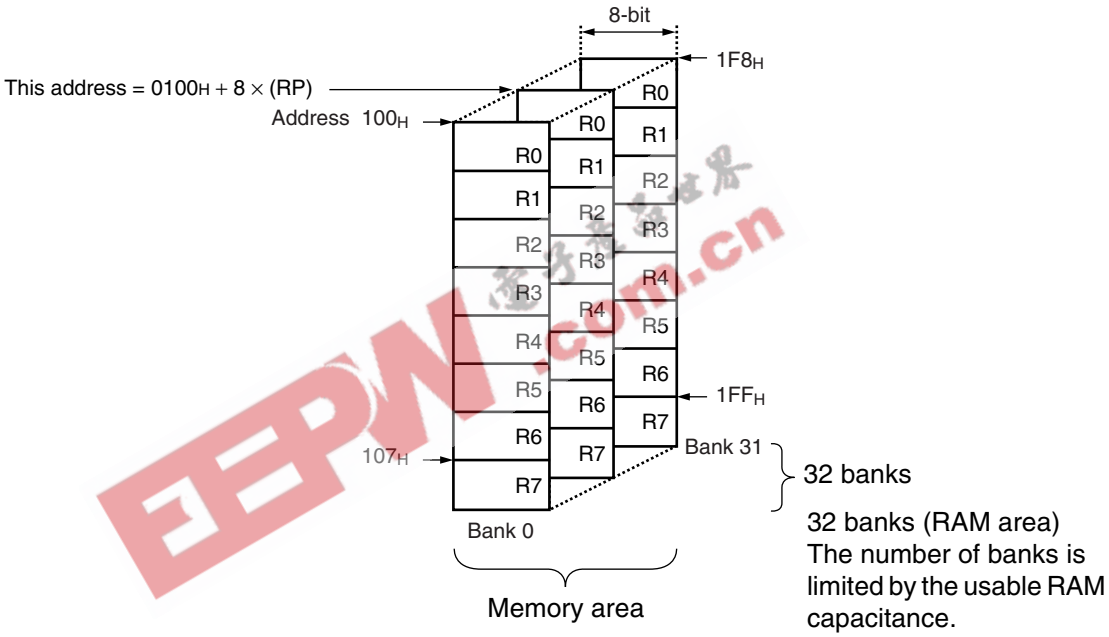
C flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8 registers. Up to a total of 32 banks can be used on the MB95120MB series. The bank currently in use is indicated by the register bank pointer (RP).8-register. Up to a total of 32 banks can be used on the MB95120MB series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	00000000B
0007H	SYCC	System clock control register	R/W	1010X011B
0008H	STBC	Standby control register	R/W	00000000B
0009H	RSRR	Reset source register	R/W	XXXXXXXXB
000AH	TBTC	Timebase timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00000000B
000DH	—	(Disabled)	—	—
000EH	PDR2	Port 2 data register	R/W	00000000B
000FH	DDR2	Port 2 direction register	R/W	00000000B
0010H	PDR3	Port 3 data register	R/W	00000000B
0011H	DDR3	Port 3 direction register	R/W	00000000B
0012H	PDR4	Port 4 data register	R/W	00000000B
0013H	DDR4	Port 4 direction register	R/W	00000000B
0014H	PDR5	Port 5 data register	R/W	00000000B
0015H	DDR5	Port 5 direction register	R/W	00000000B
0016H	PDR6	Port 6 data register	R/W	00000000B
0017H	DDR6	Port 6 direction register	R/W	00000000B
0018H	PDR7	Port 7 data register	R/W	00000000B
0019H	DDR7	Port 7 direction register	R/W	00000000B
001AH, 001BH	—	(Disabled)	—	—
001CH	PDR9	Port 9 data register	R/W	00000000B
001DH	DDR9	Port 9 direction register	R/W	00000000B
001EH	PDRA	Port A data register	R/W	00000000B
001FH	DDRA	Port A direction register	R/W	00000000B
0020H	PDRB	Port B data register	R/W	00000000B
0021H	DDRB	Port B direction register	R/W	00000000B
0022H	PDRC	Port C data register	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0023H	DDRC	Port C direction register	R/W	00000000B
0024H	PDRD	Port D data register	R/W	00000000B
0025H	DDRD	Port D direction register	R/W	00000000B
0026H	PDRE	Port E data register	R/W	00000000B
0027H	DDRE	Port E direction register	R/W	00000000B
0028H to 002CH	—	(Disabled)	—	—
002DH	PUL1	Port 1 pull-up register	R/W	00000000B
002EH	PUL2	Port 2 pull-up register	R/W	00000000B
002FH	PUL3	Port 3 pull-up register	R/W	00000000B
0030H	PUL4	Port 4 pull-up register	R/W	00000000B
0031H	PUL5	Port 5 pull-up register	R/W	00000000B
0032H	PUL7	Port 7 pull-up register	R/W	00000000B
0033H to 0035H	—	(Disabled)	—	—
0036H	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000B
0037H	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000B
0038H	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000B
0039H	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000B
003AH	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000B
003BH	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000B
003CH	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000B
003DH	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000B
003EH	TMCSRH0	16-bit reload timer control status register (upper byte) ch.0	R/W	00000000B
003FH	TMCSRL0	16-bit reload timer control status register (lower byte) ch.0	R/W	00000000B
0040H, 0041H	—	(Disabled)	—	—
0042H	PCNTH0	16-bit PPG status control register (upper byte) ch.0	R/W	00000000B
0043H	PCNTL0	16-bit PPG status control register (lower byte) ch.0	R/W	00000000B
0044H	PCNTH1	16-bit PPG status control register (upper byte) ch.1	R/W	00000000B
0045H	PCNTL1	16-bit PPG status control register (lower byte) ch.1	R/W	00000000B
0046H, 0047H	—	(Disabled)	—	—
0048H	EIC00	External interrupt circuit control register ch.0/ch.1	R/W	00000000B
0049H	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
004A$_H$	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000$_B$
004C$_H$	EIC01	External interrupt circuit control register ch.8/ch.9	R/W	00000000$_B$
004D$_H$	EIC11	External interrupt circuit control register ch.10/ch.11	R/W	00000000$_B$
004E$_H$, 004F$_H$	—	(Disabled)	—	—
0050$_H$	SCR	LIN-UART serial control register	R/W	00000000$_B$
0051$_H$	SMR	LIN-UART serial mode register	R/W	00000000$_B$
0052$_H$	SSR	LIN-UART serial status register	R/W	00001000$_B$
0053$_H$	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000$_B$
0054$_H$	ESCR	LIN-UART extended status control register	R/W	00000100$_B$
0055$_H$	ECCR	LIN-UART extended communication control register	R/W	000000XX$_B$
0056$_H$	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000$_B$
0057$_H$	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000$_B$
0058$_H$	SSR0	UART/SIO serial status register ch.0	R/W	00000001$_B$
0059$_H$	TDR0	UART/SIO serial output data register ch.0	R/W	00000000$_B$
005A$_H$	RDR0	UART/SIO serial input data register ch.0	R	00000000$_B$
005B$_H$ to 005F$_H$	—	(Disabled)	—	—
0060$_H$	IBCR00	I^{2}C bus control register 0 ch.0	R/W	00000000$_B$
0061$_H$	IBCR10	I^{2}C bus control register 1 ch.0	R/W	00000000$_B$
0062$_H$	IBSR0	I^{2}C bus status register ch.0	R	00000000$_B$
0063$_H$	IDDR0	I^{2}C data register ch.0	R/W	00000000$_B$
0064$_H$	IAAR0	I^{2}C address register ch.0	R/W	00000000$_B$
0065$_H$	ICCR0	I^{2}C clock control register ch.0	R/W	00000000$_B$
0066$_H$ to 006B$_H$	—	(Disabled)	—	—
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register (upper byte)	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register (lower byte)	R/W	00000000$_B$
0070$_H$	WCSR	Watch counter status register	R/W	00000000$_B$
0071$_H$	—	(Disabled)	—	—
0072$_H$	FSR	Flash memory status register	R/W	000X0000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0073H	SWRE0	Flash memory sector writing control register 0	R/W	00000000B
0074H	SWRE1	Flash memory sector writing control register 1	R/W	00000000B
0075H	—	(Disabled)	—	—
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	Register bank pointer (RP) , Mirror of direct bank pointer (DP)	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(Disabled)	—	—
0F80H	WRARH0	Wild register address setting register (upper byte) ch.0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (lower byte) ch.0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch.0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (upper byte) ch.1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (lower byte) ch.1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch.1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (upper byte) ch.2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (lower byte) ch.2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch.2	R/W	00000000B
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000B
0F93H	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000B
0F94H	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000B
0F95H	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000B
0F96H	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000B
0F97H	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	00000000B
0F98H	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	00000000B
0F99H	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000B
0F9AH	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F9B$_H$	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000$_B$
0F9C$_H$	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	11111111$_B$
0F9D$_H$	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	11111111$_B$
0F9E$_H$	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	11111111$_B$
0F9F$_H$	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	11111111$_B$
0FA0$_H$	PPS11	8/16-bit PPG1 cycle setting buffer register ch.1	R/W	11111111$_B$
0FA1$_H$	PPS10	8/16-bit PPG0 cycle setting buffer register ch.1	R/W	11111111$_B$
0FA2$_H$	PDS11	8/16-bit PPG1 duty setting buffer register ch.1	R/W	11111111$_B$
0FA3$_H$	PDS10	8/16-bit PPG0 duty setting buffer register ch.1	R/W	11111111$_B$
0FA4$_H$	PPGS	8/16-bit PPG start register	R/W	00000000$_B$
0FA5$_H$	REVC	8/16-bit PPG output inversion register	R/W	00000000$_B$
0FA6$_H$	TMRH0/ TMRLRH0	16-bit reload timer timer/reload register (upper byte) ch.0	R/W	00000000$_B$
0FA7$_H$	TMRL0/ TMRLRL0	16-bit reload timer timer/reload register (lower byte) ch.0	R/W	00000000$_B$
0FA8$_H$, 0FA9$_H$	—	(Disabled)	—	—
0FAA$_H$	PDCRH0	16-bit PPG down counter register (upper byte) ch.0	R	00000000$_B$
0FAB$_H$	PDCRL0	16-bit PPG down counter register (lower byte) ch.0	R	00000000$_B$
0FAC$_H$	PCSRH0	16-bit PPG cycle setting buffer register (upper byte) ch.0	R/W	11111111$_B$
0FAD$_H$	PCSRL0	16-bit PPG cycle setting buffer register (lower byte) ch.0	R/W	11111111$_B$
0FAE$_H$	PDUTH0	16-bit PPG duty setting buffer register (upper byte) ch.0	R/W	11111111$_B$
0FAF$_H$	PDUTL0	16-bit PPG duty setting buffer register (lower byte) ch.0	R/W	11111111$_B$
0FB0$_H$	PDCRH1	16-bit PPG down counter register (upper byte) ch.1	R	00000000$_B$
0FB1$_H$	PDCRL1	16-bit PPG down counter register (lower byte) ch.1	R	00000000$_B$
0FB2$_H$	PCSRH1	16-bit PPG cycle setting buffer register (upper byte) ch.1	R/W	11111111$_B$
0FB3$_H$	PCSRL1	16-bit PPG cycle setting buffer register (lower byte) ch.1	R/W	11111111$_B$
0FB4$_H$	PDUTH1	16-bit PPG duty setting buffer register (upper byte) ch.1	R/W	11111111$_B$
0FB5$_H$	PDUTL1	16-bit PPG duty setting buffer register (lower byte) ch.1	R/W	11111111$_B$
0FB6$_H$ to 0FBB$_H$	—	(Disabled)	—	—
0FBC$_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000$_B$
0FBD$_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000$_B$
0FBE$_H$	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch.0	R/W	00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FBF$_H$	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch.0	R/W	00000000$_B$
0FC0$_H$, 0FC1$_H$	—	(Disabled)	—	—
0FC2$_H$	AIDRH	A/D input disable register (upper byte)	R/W	00000000$_B$
0FC3$_H$	AIDRL	A/D input disable register (lower byte)	R/W	00000000$_B$
0FC4$_H$	LCDCC	LCDC control register	R/W	00010000$_B$
0FC5$_H$	LCDCE1	LCDC enable register 1	R/W	00110000$_B$
0FC6$_H$	LCDCE2	LCDC enable register 2	R/W	00000000$_B$
0FC7$_H$	LCDCE3	LCDC enable register 3	R/W	00000000$_B$
0FC8$_H$	LCDCE4	LCDC enable register 4	R/W	00000000$_B$
0FC9$_H$	LCDCE5	LCDC enable register 5	R/W	00000000$_B$
0FCA$_H$	LCDCE6	LCDC enable register 6	R/W	00000000$_B$
0FCB$_H$	LCDCB1	LCDC blinking setting register 1	R/W	00000000$_B$
0FCC$_H$	LCDCB2	LCDC blinking setting register 2	R/W	00000000$_B$
0FCD$_H$ to 0FE0$_H$	LCDRAM	LCDC display RAM	R/W	00000000$_B$
0FE1$_H$, 0FE2$_H$	—	(Disabled)	—	—
0FE3$_H$	WCDR	Watch counter data register	R/W	00111111$_B$
0FE4$_H$, 0FE5$_H$	—	(Disabled)	—	—
0FE6$_H$	ILSR3	Input level select register 3	R/W	00000000$_B$
0FE7$_H$	ILSR2	Input level select register 2	R/W	00000000$_B$
0FE8$_H$, 0FE9$_H$	—	(Disabled)	—	—
0FEA$_H$	CSVCR	Clock supervisor control register	R/W	00011100$_B$
0FEB$_H$ to 0FED$_H$	—	(Disabled)	—	—
0FEE$_H$	ILSR	Input level select register	R/W	00000000$_B$
0FEF$_H$	WICR	Interrupt pin select circuit control register	R/W	01000000$_B$
0FF0$_H$ to 0FFF$_H$	—	(Disabled)	—	—

(Continued)

(Continued)

- R/W access symbols
  - R/W : Readable/Writable
  - R : Read only
  - W : Write only
- Initial value symbols
  - 0 : The initial value of this bit is “0”.
  - 1 : The initial value of this bit is “1”.
  - X : The initial value of this bit is undefined.

Note : Do not write to the “ (Disabled) ”. Reading the “ (Disabled) ” returns an undefined value.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA$_H$	FFFB$_H$	L00 [1 : 0]	High
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8$_H$	FFF9$_H$	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6$_H$	FFF7$_H$	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4$_H$	FFF5$_H$	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2$_H$	FFF3$_H$	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0$_H$	FFF1$_H$	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ6	FFEE$_H$	FFEF$_H$	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC$_H$	FFED$_H$	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA$_H$	FFEB$_H$	L08 [1 : 0]	
8/16-bit PPG ch.1 (Lower)	IRQ9	FFE8$_H$	FFE9$_H$	L09 [1 : 0]	
8/16-bit PPG ch.1 (Upper)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1 : 0]	
16-bit reload timer ch.0	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1 : 0]	
I^{2}C ch.0	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1 : 0]	
16-bit PPG ch.1	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1 : 0]	
Watch prescaler/watch counter	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1 : 0]	
External interrupt ch.8	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1 : 0]	
External interrupt ch.9					
External interrupt ch.10					
External interrupt ch.11					
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1 : 0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1 : 0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	Vcc AVcc	Vss − 0.3	Vss + 6.0	V	*2
	AVR	Vss − 0.3	Vss + 6.0		*2
Power supply voltage for LCD	V0 to V3	V_{SS} − 0.3	V_{SS} + 6.0	V	*3
Input voltage*1	V_I	Vss − 0.3	Vss + 6.0	V	*4
Output voltage*1	V_O	Vss − 0.3	Vss + 6.0	V	*4
Maximum clamp current	I_{CLAMP}	− 2.0	+ 2.0	mA	Applicable to pins*5
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins*5
“L” level maximum output current	I_{OL1}	—	15	mA	Other than P00 to P07
	I_{OL2}		15		P00 to P07
“L” level average current	I_{OLAV1}	—	4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
“H” level maximum output current	I_{OH1}	—	− 15	mA	Other than P00 to P07
	I_{OH2}		− 15		P00 to P07
“H” level average current	I_{OHAV1}	—	− 4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		− 8		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	− 100	mA	
“H” level total average output current	ΣI_{OHAV}	—	− 50	mA	Total average output current = operating current × operating ratio (Total of pins)

(Continued)

(Continued)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	− 40	+ 105	°C	
Storage temperature	Tstg	− 55	+ 150	°C	

*1 : The parameter is based on AV_{SS} = V_{SS} = 0.0 V.

*2 : Apply equal potential to AVcc and Vcc. AVR should not exceed AVcc + 0.3 V.

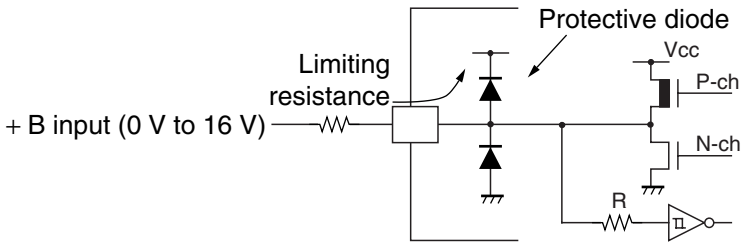
*3 : V0 to V3 should not exceed V_{CC} + 0.3 V.

*4 : V_I and Vo should not exceed V_{CC} + 0.3 V. V_I must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*5 : Applicable to pins : P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53

- Use within recommended operating conditions.
- Use at DC voltage (current).
- +B signal is an input signal that exceeds V_{CC} voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

• Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

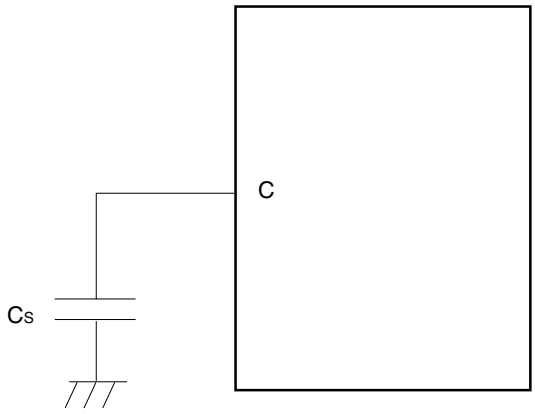
Parameter	Symbol	Condition	Value Min	Value Max	Unit	Remarks	
Power supply voltage	V_{CC}, AV_{CC}	—	2.42*1,*2	5.5*1	V	In normal operating	Other than MB95FV100D-103
			2.3	5.5		Hold condition in STOP mode	
			2.7	5.5		In normal operating	MB95FV100D-103
			2.3	5.5		Hold condition in STOP mode	
Power supply voltage for LCD	V0 to V3		V_{SS}	V_{CC}	V	The range of liquid crystal power supply (The optimal value depends on liquid crystal display elements used.)	
A/D converter reference input voltage	AVR		4.0	AV_{CC}	V		
Smoothing capacitor	C_S		0.1	1.0	µF	*3	
Operating temperature	T_A		− 40	+ 105	°C	Other than MB95FV100D-103	
			+ 5	+ 35	°C	MB95FV100D-103	

*1 : The values vary with the operating frequency, machine clock or analog guarantee range.

*2 : The value is 2.88 V when the low voltage detection reset is used.

*3 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of V_{CC} pin must have a capacitor value higher than C_S. For connection of smoothing capacitor C_S, refer to the diagram below.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = AV_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IH1}	P10 (selectable at UI0), P67 (selectable at SIN)	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input (When selecting CMOS input level)
	V_{IH2}	P50, P51 (selectable at I²C)	—	0.7 V_{CC}	—	V_{SS} + 5.5	V	
	V_{IHA}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHS1}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHS2}	P50, P51	—	0.8 V_{CC}	—	V_{SS} + 5.5	V	
	V_{IHM}	$\overline{RST}$, MOD	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input (Flash memory product)
			—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input (MASK ROM product)
“L” level input voltage	V_{IL}	P10 (selectable at UI0), P50, P51 (selectable at I²C) P67 (selectable at SIN)	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	Hysteresis input (When selecting CMOS input level)
	V_{ILA}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Port inputs if Automotive input levels are selected

(Continued)

(V_{CC} = AV_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{ILS}	P00 to P07, P10 to P14, P20 to P24, P30 to P37, P40 to P43, P50 to P53, P60 to P67, P70, P71, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	$\overline{RST}$, MOD	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	CMOS input (Flash memory product)
			—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input (MASK ROM product)
Open-drain output application voltage	V_{D1}	P50, P51	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pin other than P00 to P07	I_{OH} = − 4.0 mA	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P00 to P07	I_{OH} = − 8.0 mA	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pin other than P00 to P07, $\overline{RST}$*1	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P00 to P07	I_{OL} = 12 mA	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	Port other than P50, P51	0.0 V < V_I < V_{CC}	− 5	—	+ 5	µA	When the pull-up prohibition setting
Open-drain output leakage current	I_{LIOD}	P50, P51	0.0 V < V_I < V_{SS} + 5.5 V	—	—	5	µA	

(Continued)

(V_{CC} = AV_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistor	R_{PULL}	P10 to P14, P20 to P24, P30 to P37, P40 to P43, P52, P53, P70, P71	V_I = 0.0 V	25	50	100	kΩ	When the pull-up permission setting
Pull-down resistor	R_{MOD}	MOD	V_I = V_{CC}	50	100	200	kΩ	MASK ROM product only
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, V_{CC}, V_{SS}	f = 1 MHz	—	5	15	pF	
Power supply current*2	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 20 MHz F_{MP} = 10 MHz Main clock mode (divided by 2)	—	9.5	12.5	mA	Flash memory product (at other than Flash memory writing and erasing)
				—	30.0	35.0	mA	Flash memory product (at Flash memory writing and erasing)
				—	7.2	9.5	mA	MASK ROM product
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	15.2	20.0	mA	Flash memory product (at other than Flash memory writing and erasing)
				—	35.7	42.5	mA	Flash memory product (at Flash memory writing and erasing)
				—	11.6	15.2	mA	MASK ROM product

(Continued)

(V_{CC} = AV_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCS}	V_{CC} (External clock operation)	F_{CH} = 20 MHz F_{MP} = 10 MHz Main Sleep mode (divided by 2)	—	4.5	7.5	mA	
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main Sleep mode (divided by 2)	—	7.2	12.0	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub clock mode (divided by 2)	—	45	100	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub sleep mode (divided by 2)	—	10	81	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25 °C	—	4.6	27.0	µA	
	I_{CCMPLL}		F_{CH} = 4 MHz F_{MP} = 10 MHz Main PLL mode (multiplied by 2.5)	—	9.3	12.5	mA	Flash memory product
				—	7.0	9.5	mA	MASK ROM product
			F_{CH} = 6.4 MHz F_{MP} = 16 MHz Main PLL mode (multiplied by 2.5)	—	14.9	20.0	mA	Flash memory product
				—	11.2	15.2	mA	MASK ROM product

(Continued)

(Continued)

(V_{CC} = AV_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I_{CCSPLL}	V_{CC} (External clock operation)	F_{CL} = 32 kHz F_{MPL} = 128 kHz Sub PLL mode (multiplied by 4), T_A = + 25 °C	—	160	400	µA	
	I_{CTS}		F_{CH} = 10 MHz Timebase timer mode T_A = + 25 °C	—	0.40	1.10	mA	
	I_{CCH}		Sub stop mode T_A = + 25 °C	—	3.5	20	µA	
	I_A	AV_{CC}	F_{CH} = 16 MHz At operating of A/D conversion	—	2.4	4.7	mA	
	I_{AH}		F_{CH} = 16 MHz At stopping of A/D conversion T_A = + 25 °C	—	1	5	µA	
LCD internal division resistance	R_{LCD}	—	Between V3 and V_{SS}	—	300	—	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 3.6 V	—	—	5	kΩ	
SEG00 to SEG39 output impedance	R_{VSEG}	SEG00 to SEG39	—	—	—	7	kΩ	
LCD leak current	I_{LCDL}	V0 to V3, COM0 to COM3 SEG00 to SEG39	—	− 1	—	+ 1	µA	

*1 : Product without clock supervisor only.

*2 :
- The power-supply current is determined by the external clock. When both low voltage detection option and clock supervisor are selected, the power-supply current will be a value of adding current consumption of the low voltage detection circuit (I_{LVD}) and current consumption of built-in CR oscillator (I_{CSV}) to the specified value.
- Refer to “4. AC Characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

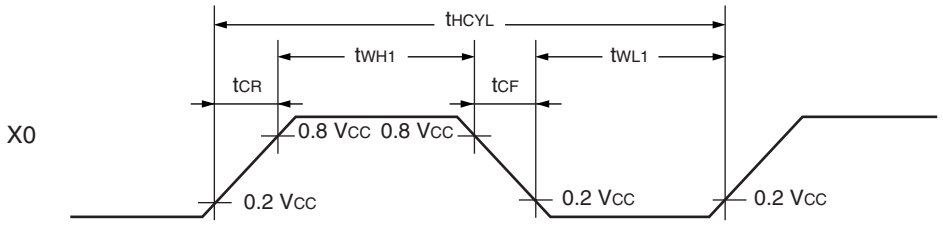
4. AC Characteristics

(1) Clock Timing

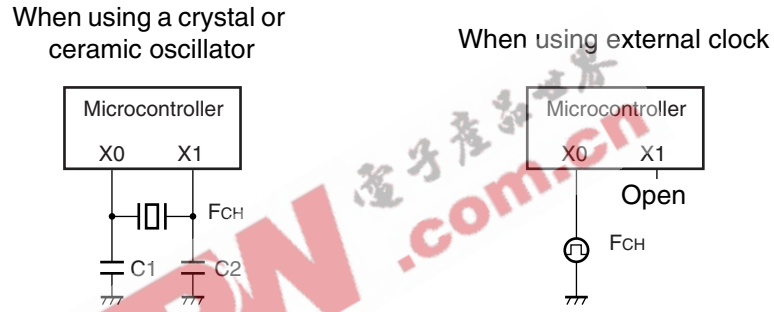
(V_{CC} = 2.42 V to 5.5 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1.00	—	16.25	MHz	When using main oscillation circuit
				1.00	—	32.50	MHz	When using external clock
				3.00	—	10.00	MHz	Main PLL multiplied by 1
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.50	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When using sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL V_{CC} = 2.3 V to 3.6 V
Clock cycle time	t_{HCYL}	X0, X1		61.5	—	1000	ns	When using main oscillation circuit
				30.8	—	1000	ns	When using external clock
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When using sub oscillation circuit
Input clock pulse width	t_{WH1} t_{WL1}	X0		61.5	—	—	ns	When using external clock Duty ratio is about 30% to 70%.
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A		—	—	5	ns	When using external clock

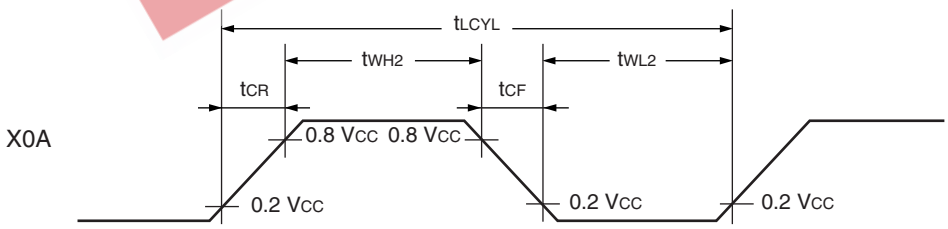
• Input wave form for using external clock (main clock)



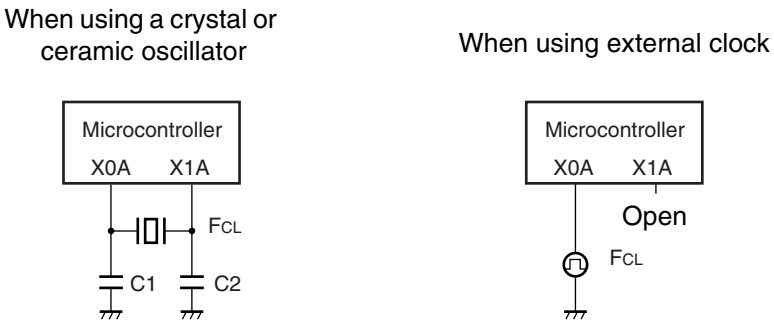
• Figure of Main Clock Input Port External Connection



• Input wave form for using external clock (sub clock)



• Figure of Sub clock Input Port External Connection



(2) Source Clock/Machine Clock

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Source clock cycle time*1 (Clock before setting division)	t_{SCLK}	—	61.5	2000	ns	When using main clock Min : F_{CH} = 8.125 MHz, PLL multiplied by 2 Max : F_{CH} = 1 MHz, divided by 2
			7.6	61.0	µs	When using sub clock Min : F_{CL} = 32 kHz, PLL multiplied by 4 Max : F_{CL} = 32 kHz, divided by 2
Source clock frequency	F_{SP}		0.50	16.25	MHz	When using main clock
	F_{SPL}		16.384	131.072	kHz	When using sub clock
Machine clock cycle time*2 (Minimum instruction execution time)	t_{MCLK}		61.5	32000	ns	When using main clock Min : F_{SP} = 16.25 MHz, no division Max : F_{SP} = 0.5 MHz, divided by 16
			7.6	976.5	µs	When using sub clock Min : F_{SPL} = 131 kHz, no division Max : F_{SPL} = 16 kHz, divided by 16
Machine clock frequency	F_{MP}		0.031	16.250	MHz	When using main clock
	F_{MPL}		1.024	131.072	kHz	When using sub clock

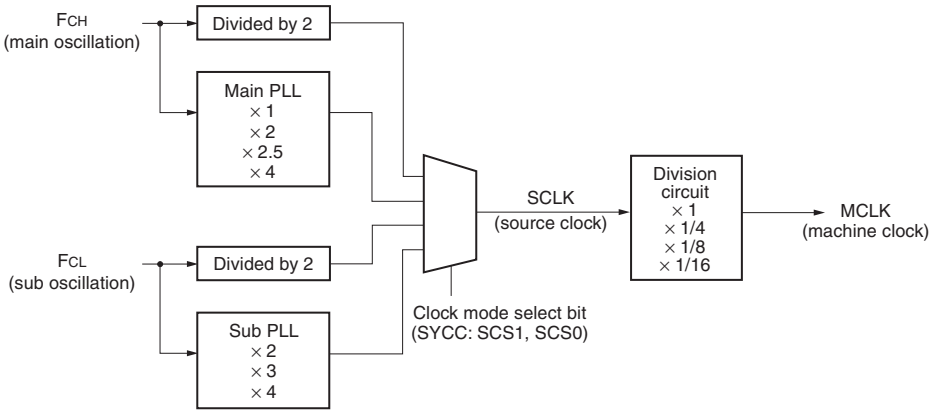
*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

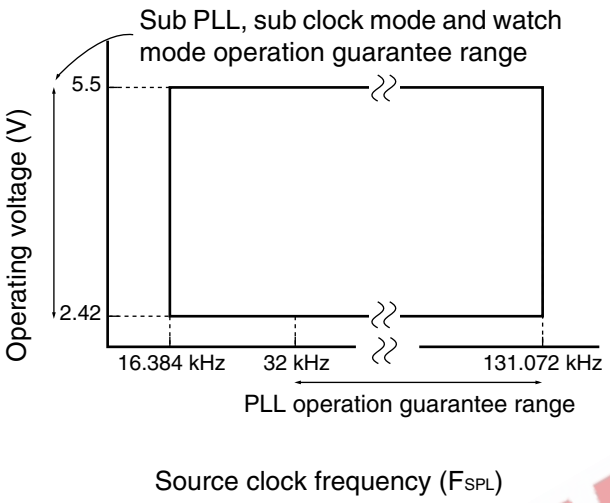
*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

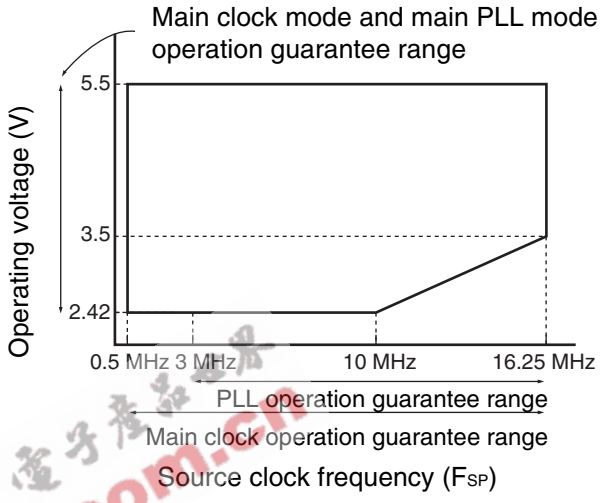
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• Outline of clock generation block

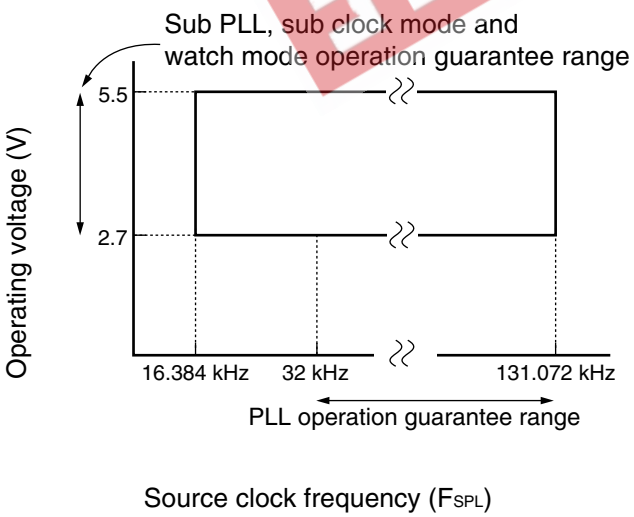


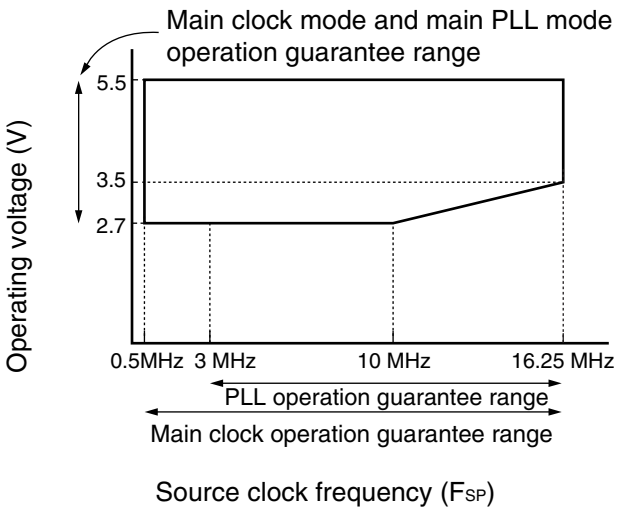
- **Operating voltage - Operating frequency (T_A = − 40 °C to + 105 °C)**
  - MB95F124MB/F124NB/F124JB/F126MB/F126NB/F126JB/F128MB/F128NB/F128JB



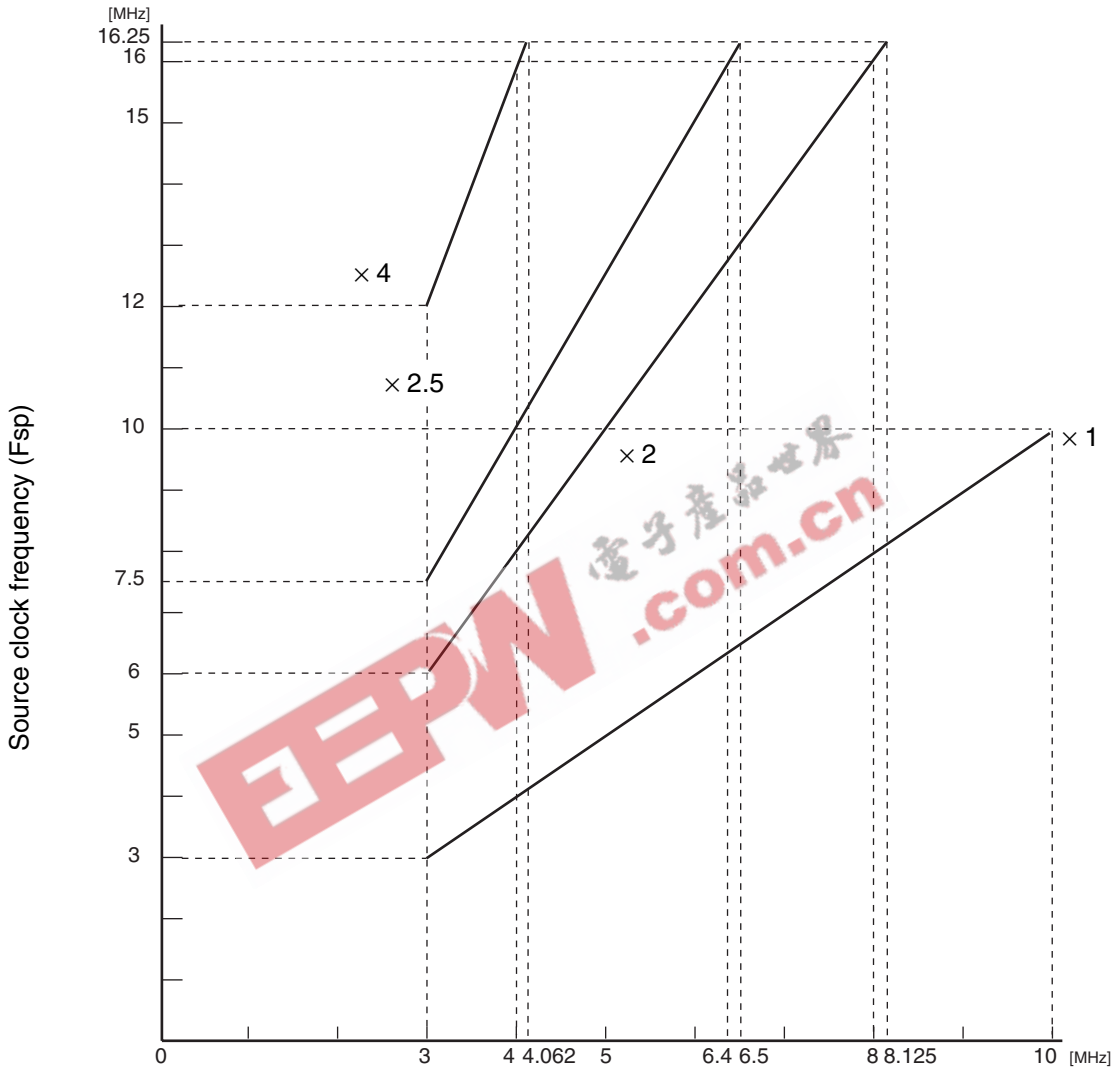


- **Operating voltage - Operating frequency (T_A = + 5 °C to + 35 °C)**
  - MB95FV100D-103





• Main PLL operation frequency



(3) External Reset

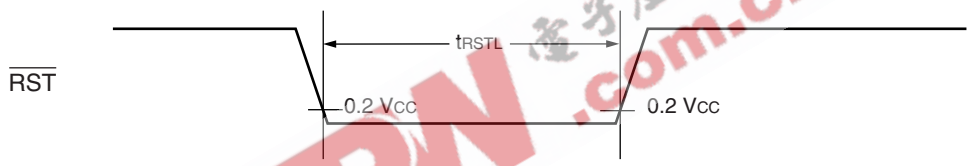
(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	$\overline{RST}$	—	2 t_{MCLK}*1	—	ns	At normal operating
				Oscillation time of oscillator*2 + 100	—	µs	At stop mode, sub clock mode, sub sleep mode, and watch mode
				100	—		At timebase timer mode

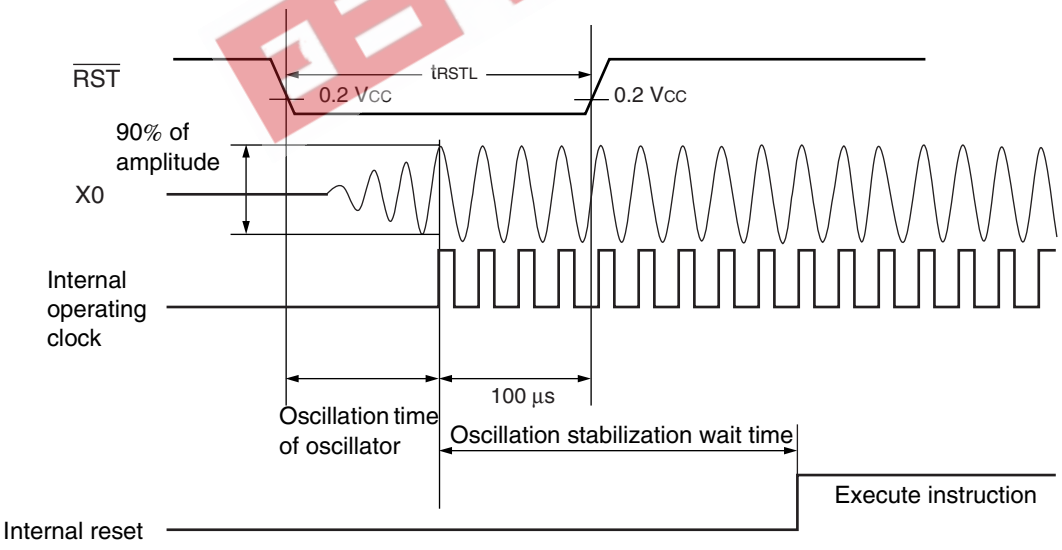
*1 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.

*2 : Oscillation start time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of µs and several ms. In the external clock, the oscillation time is 0 ms.

• At normal operating



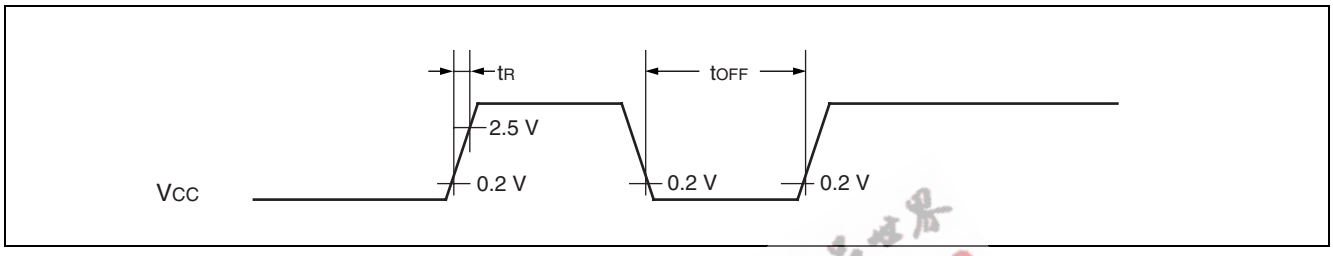
• At stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



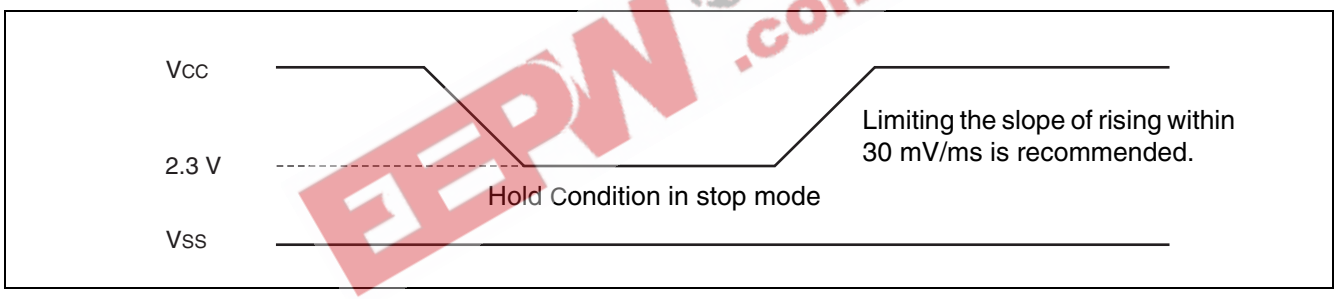
(4) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	—	—	50	ms	
Power supply cutoff time	t_{OFF}		—	1	—	ms	Waiting time until power-on



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 30 mV/ms as shown below.

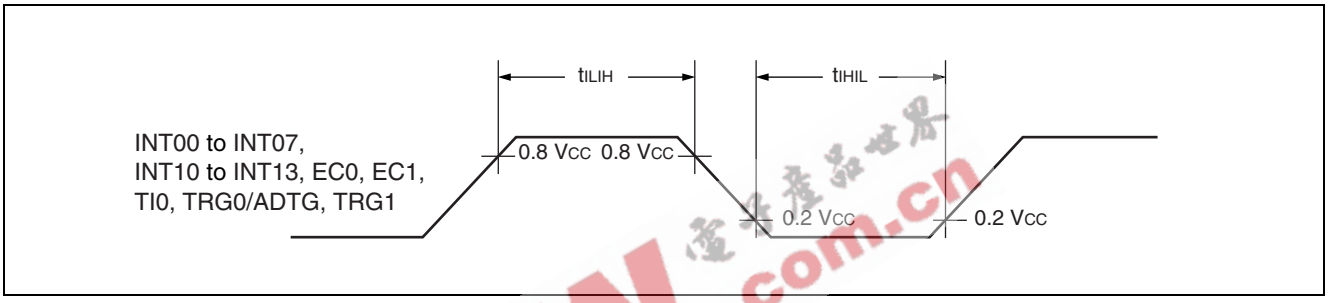


(5) Peripheral Input Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, INT10 to INT13, EC0, EC1, TI0, TRG0/ADTG, TRG1	—	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}			2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



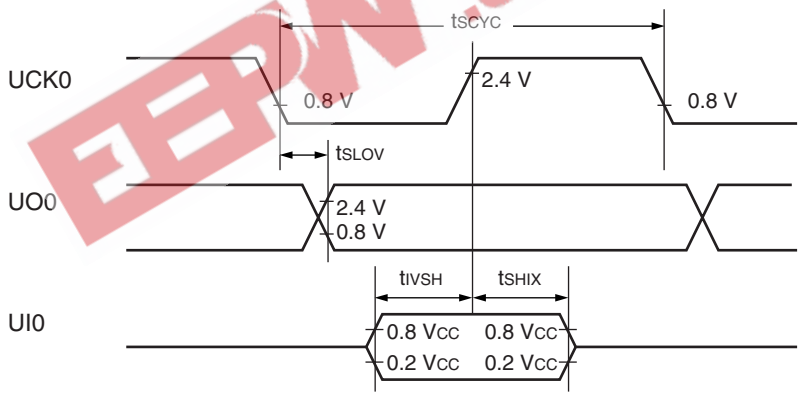
(6) UART/SIO, Serial I/O Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

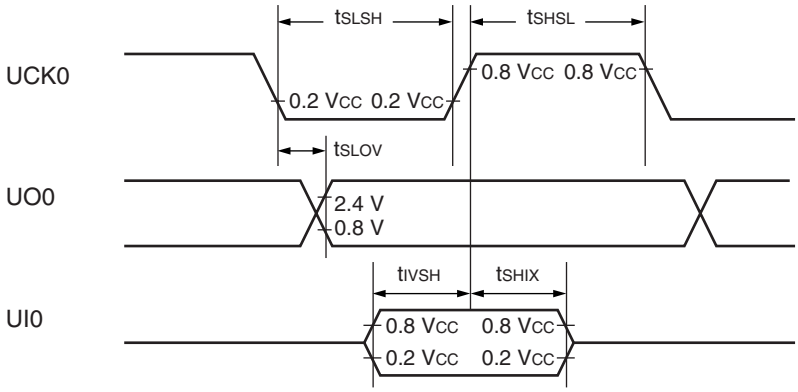
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation output pin : C_L = 80 pF + 1TTL.	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation output pin : C_L = 80 pF + 1TTL.	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		0	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

• Internal shift clock mode



• External shift clock mode



(7) LIN-UART Timing

Sampling at the rising edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 105 °C)

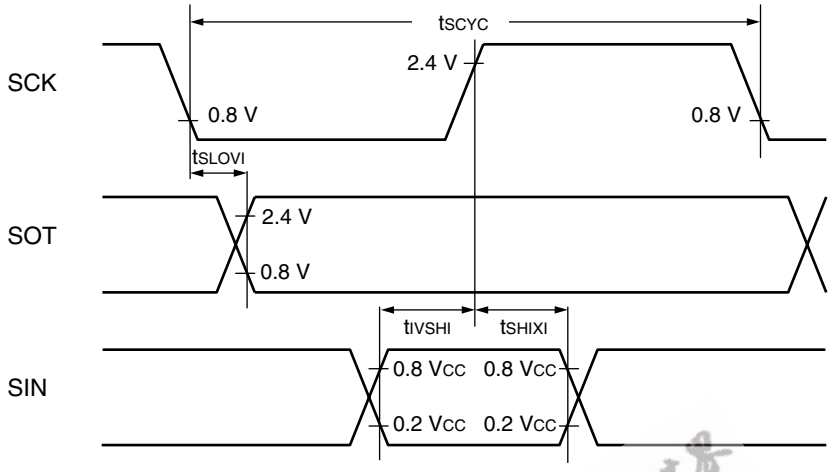
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

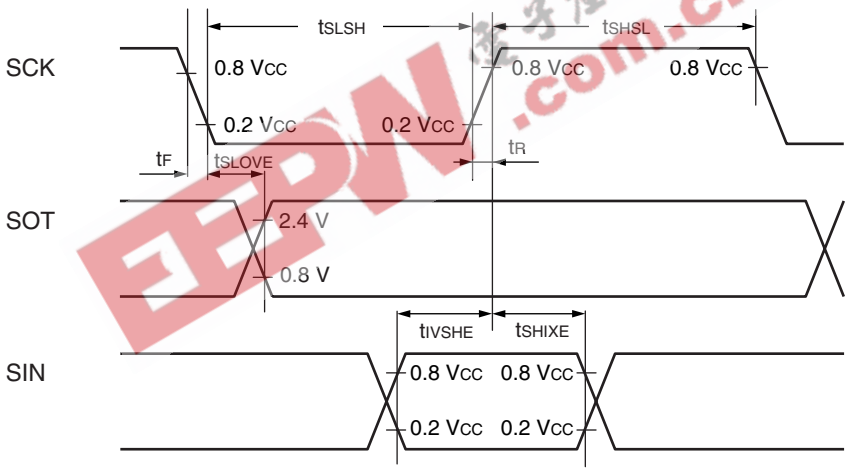
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 105 °C)

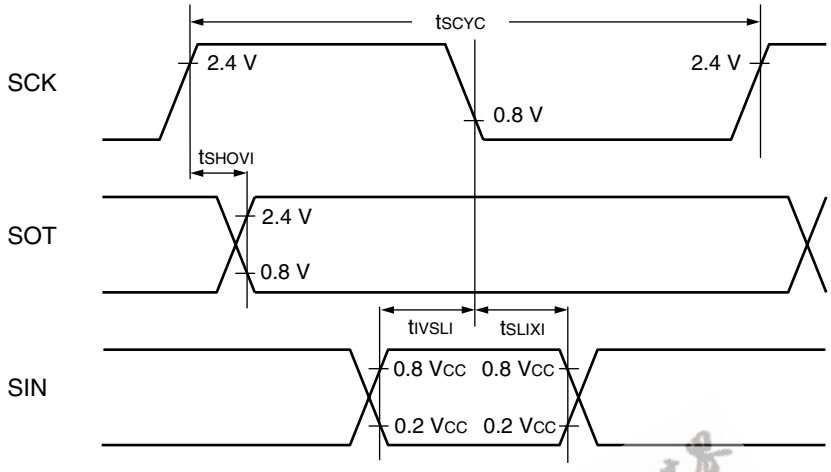
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

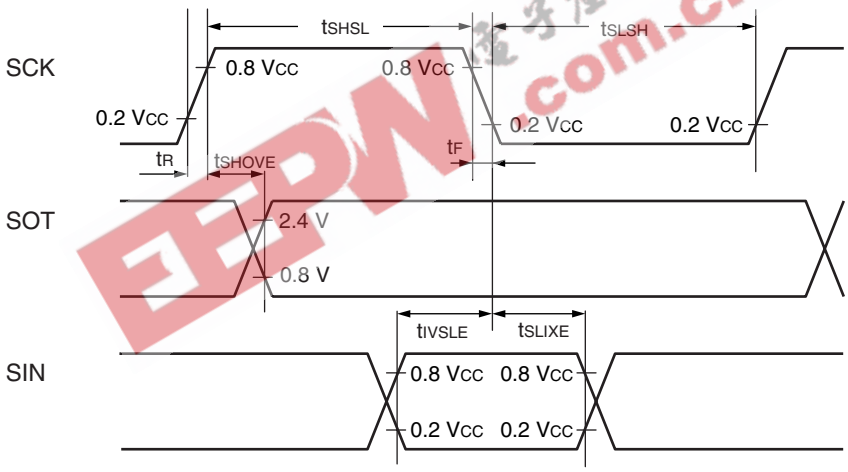
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling at the rising edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

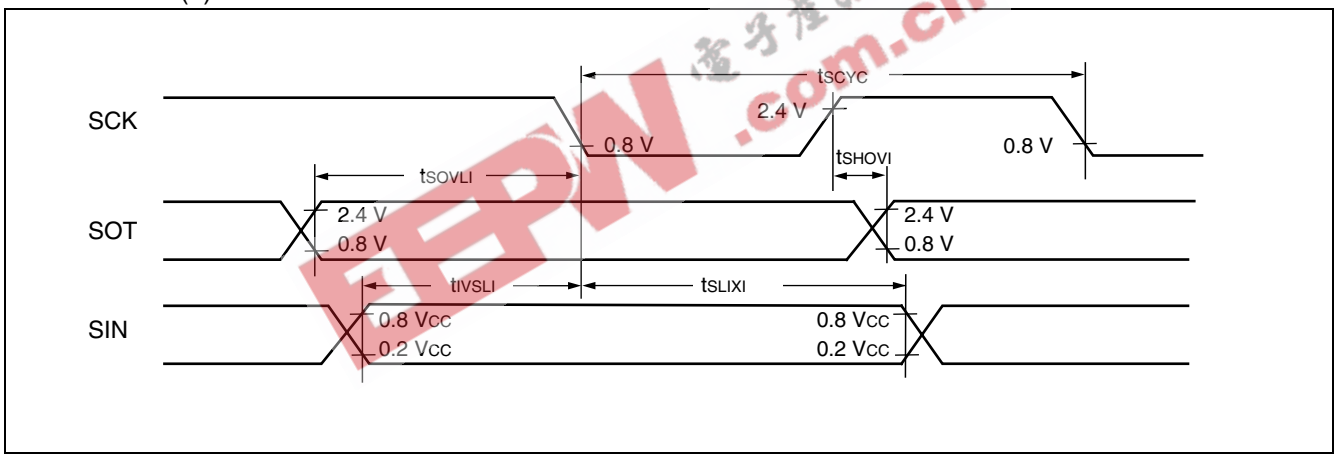
(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.



Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

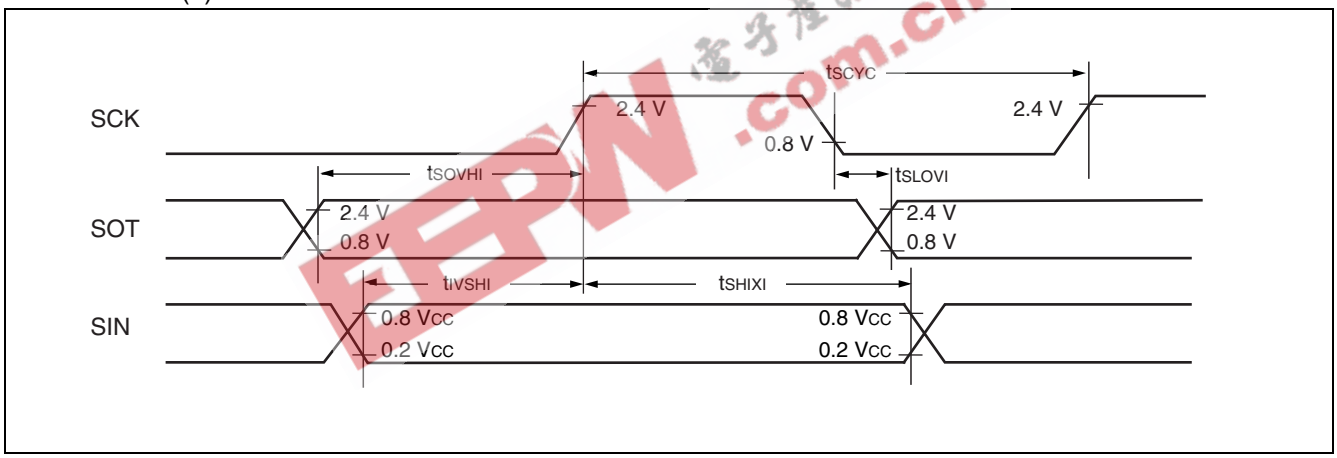
(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 105 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.



(8) I²C Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0 SDA0		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL0		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL0		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0 SDA0		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL0 SDA0		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL0 SDA0		0.25*4	—	0.1*4	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0 SDA0		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL0 SDA0		4.7	—	1.3	—	µs

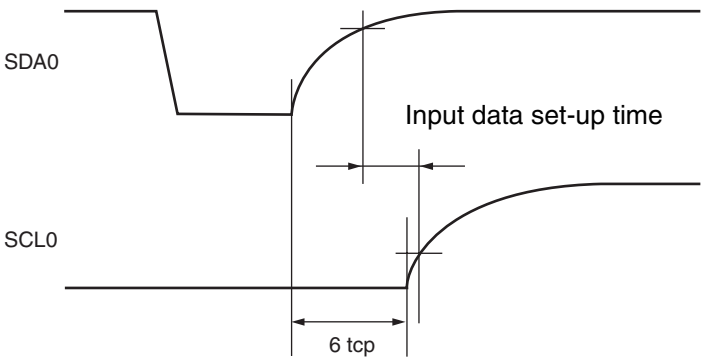
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HD;DAT}$ have only to be met if the device dose not stretch the “L” width (t_{LOW}) of the SCL signal.

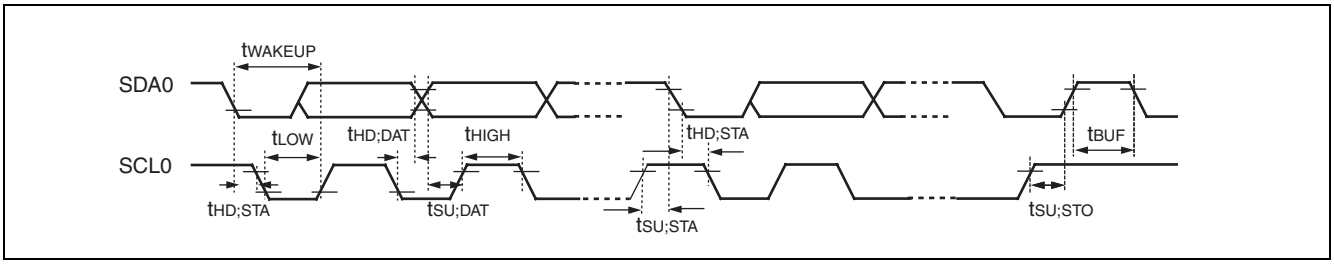
*3 : A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must then be met.

*4 : Refer to “ • Note of SDA and SCL set-up time”.

• Note of SDA and SCL set-up time



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.


tWAKEUP
SDA0
SCL0
tLOW
tHD;DAT
tHIGH
tHD;STA
tBUF
tHD;STA
tSU;DAT
tSU;STA
tSU;STO

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 105 °C)

Parameter	Sym-bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	t_{LOW}	SCL0	R = 1.7 kΩ, C = 50 pF*1	(2 + nm / 2) t_{MCLK} – 20	—	ns	Master mode
SCL clock "H" width	t_{HIGH}	SCL0		(nm / 2) t_{MCLK} – 20	(nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL0 SDA0		(–1 + nm / 2) t_{MCLK} – 20	(–1 + nm) t_{MCLK} + 20	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL0 SDA0		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL0 SDA0		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL0 SDA0		(2 nm + 4) t_{MCLK} – 20	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		3 t_{MCLK} – 20	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		(–2 + nm / 2) t_{MCLK} – 20	(–1 + nm / 2) t_{MCLK} + 20	ns	Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0		(nm / 2) t_{MCLK} – 20	(1 + nm / 2) t_{MCLK} + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock "L" width	t_{LOW}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
SCL clock "H" width	t_{HIGH}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception

(Continued)

(Continued)

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
Stop condition detection	$t_{SU;STO}$	SCL0 SDA0	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0 SDA0		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0 SDA0		t_{MCLK} – 20	—	ns	At reception
SDA↓→SCL↑ (at wakeup function)	$t_{WAKE-UP}$	SCL0 SDA0		Oscillation stabilization wait time + 2 t_{MCLK} – 20	—	ns	

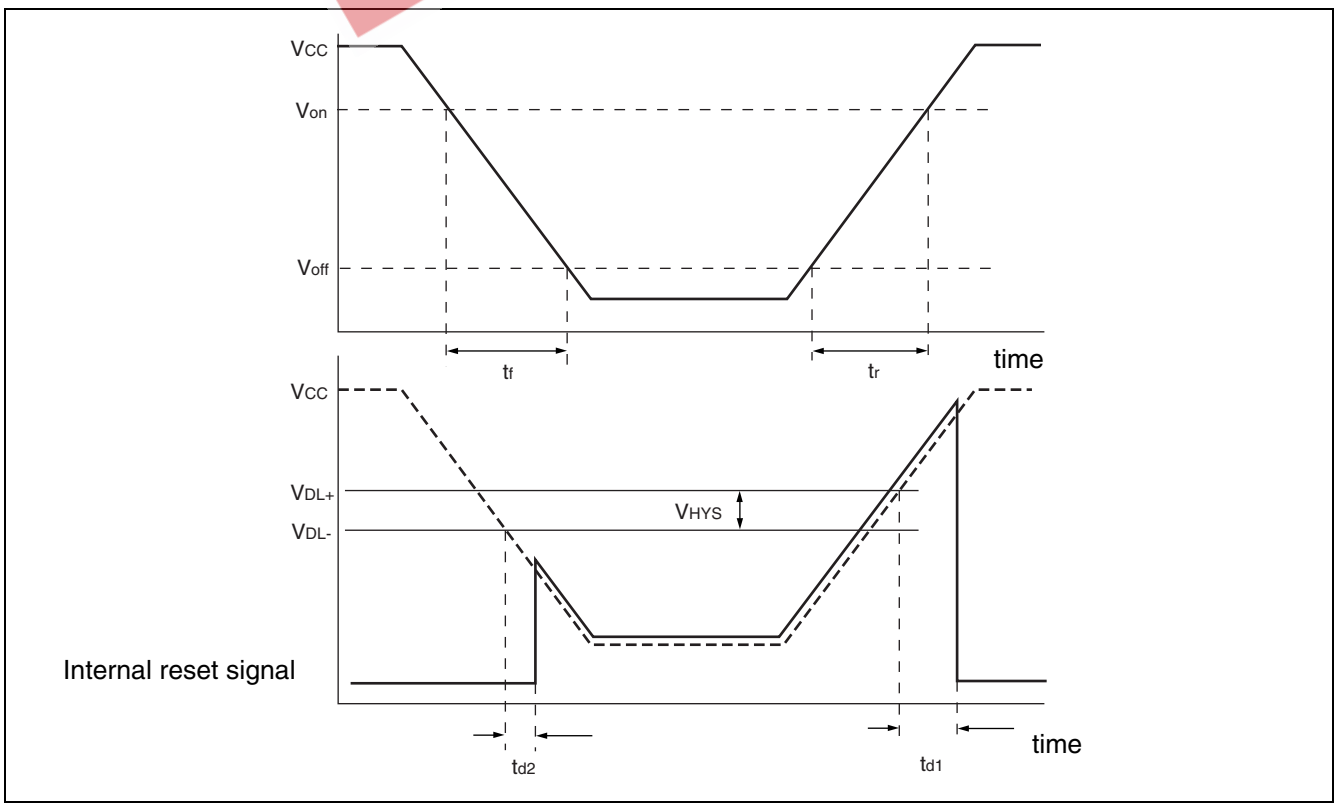
*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 :
- Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of I²C clock control register (ICCR) .
- n is CS2 bit to CS0 bit (bit 2 to bit 0) of I²C clock control register (ICCR) .
- Actual timing of I²C is determined by m and n values set by the machine clock (t_{MCLK}) and CS4 to CS0 of ICCR0 register.
- Standard-mode :
  m and n can be set at the range : 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22) , (5, 4) , (6, 4) , (7, 4) , (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38) , (5, 8) , (6, 8) , (7, 8) , (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
- Fast-mode :
  m and n can be set at the range : 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  Setting of m and n determines the machine clock that can be used below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22) , (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz

(9) Low Voltage Detection

(AVss = Vss = 0.0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Release voltage	V_{DL+}	—	2.52	2.70	2.88	V	At power-supply rise
Detection voltage	V_{DL-}		2.42	2.60	2.78	V	At power-supply fall
Hysteresis width	V_{HYS}		70	100	—	mV	
Power-supply start voltage	V_{off}		—	—	2.3	V	
Power-supply end voltage	V_{on}		4.9	—	—	V	
Power-supply voltage change time (at power supply rise)	t_r		0.3	—	—	µs	Slope of power supply that reset release signal generates
			—	3000	—	µs	Slope of power supply that reset release signal generates within rating (V_{DL+})
Power-supply voltage change time (at power supply fall)	t_f		300	—	—	µs	Slope of power supply that reset detection signal generates
			—	300	—	µs	Slope of power supply that reset detection signal generates within rating (V_{DL-})
Reset release delay time	t_{d1}		—	—	400	µs	
Reset detection delay time	t_{d2}		—	—	30	µs	
Current consumption	I_{LVD}		—	38	50	µA	Current consumption of low voltage detection circuit only



(10) Clock Supervisor Clock

(Vcc = AVcc = 5 V ± 10%, AVss = Vss = 0.0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_{OUT}	—	50	100	200	kHz	
Oscillation start time	t_{wk}		—	—	10	µs	
Current consumption	I_{CSV}		—	20	36	µA	Current consumption of built-in CR oscillator, at 100 kHz oscillation

5. A/D Converter

(1) A/D Converter Electrical Characteristics

(AVcc = Vcc = 4.0 V to 5.5 V, AVss = Vss = 0.0 V, T_A = − 40 °C to + 105 °C)

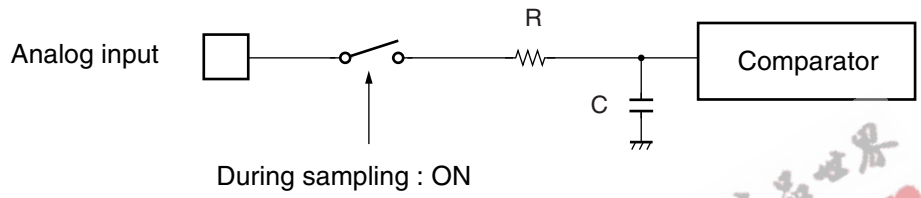
Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error			− 3.0	—	+ 3.0	LSB	
Linearity error			− 2.5	—	+ 2.5	LSB	
Differential linear error			− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}		AVss − 1.5 LSB	AVss + 0.5 LSB	AVss + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}		AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—		0.9	—	16500	µs	4.5 V ≤ AVcc ≤ 5.5 V
			1.8	—	16500	µs	4.0 V ≤ AVcc < 4.5 V
Sampling time	—		0.6	—	∞	µs	4.5 V ≤ AVcc ≤ 5.5 V, At external impedance < 5.4 kΩ
			1.2	—	∞	µs	4.0 V ≤ AVcc < 4.5 V, At external impedance < 2.4 kΩ
Analog input current	I_{AIN}		−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}		AVss	—	AVR	V	
Reference voltage	—		AVss + 4.0	—	AVcc	V	AVR pin
Reference voltage supply current	I_R		—	600	900	µA	AVR pin, During A/D operation
	I_{RH}		—	—	5	µA	AVR pin, At stop mode

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit

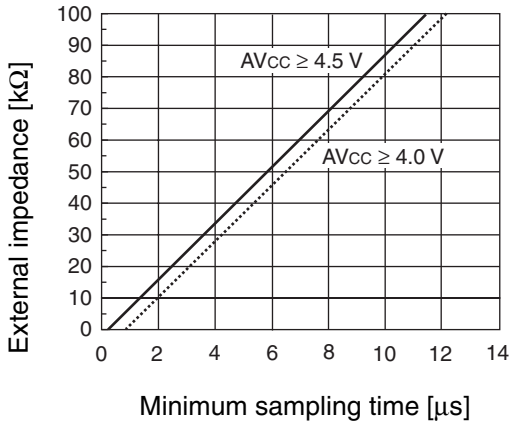


	R	C
4.5 V ≤ AVcc ≤ 5.5 V	2.0 kΩ (Max)	16 pF (Max)
4.0 V ≤ AVcc < 4.5 V	8.2 kΩ (Max)	16 pF (Max)

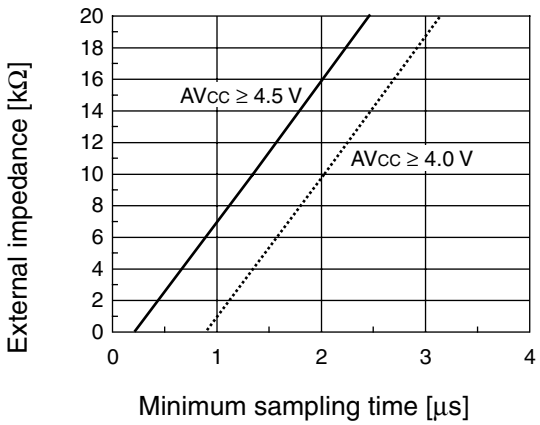
Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

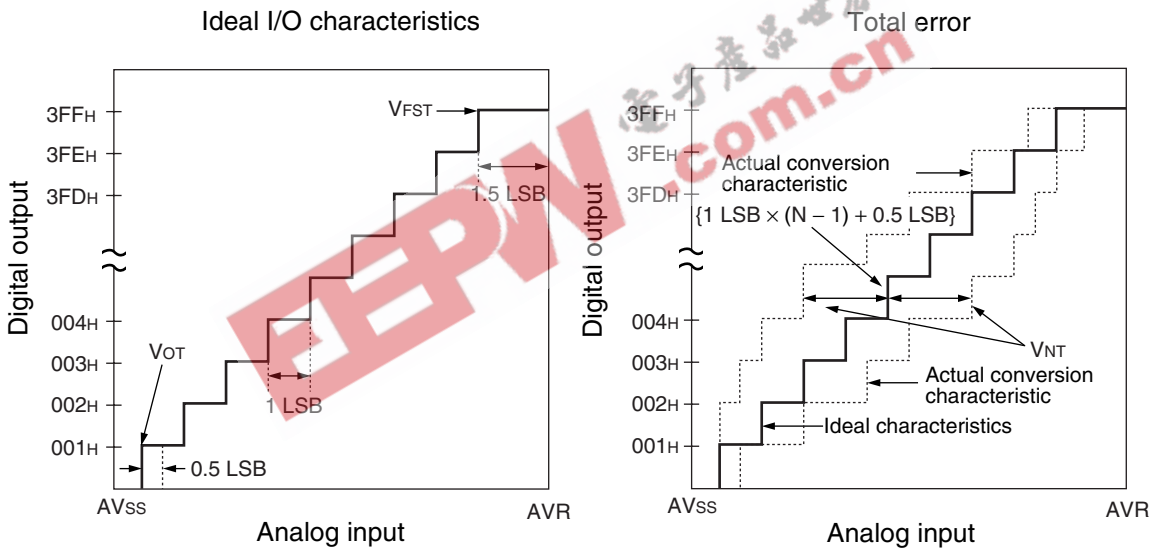


- **About errors**

As |AVcc – AVss| becomes smaller, values of relative errors grow larger.

(3) Definition of A/D Converter Terms

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device and the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.



$$1\ \text{LSB} = \frac{\text{AVR} - \text{AV}_{SS}}{1024}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H.

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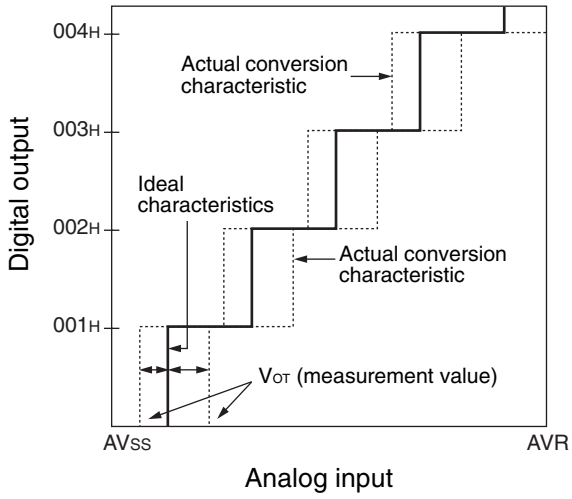
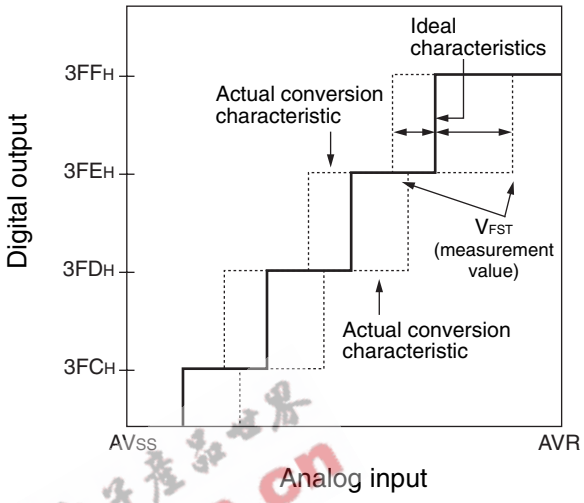
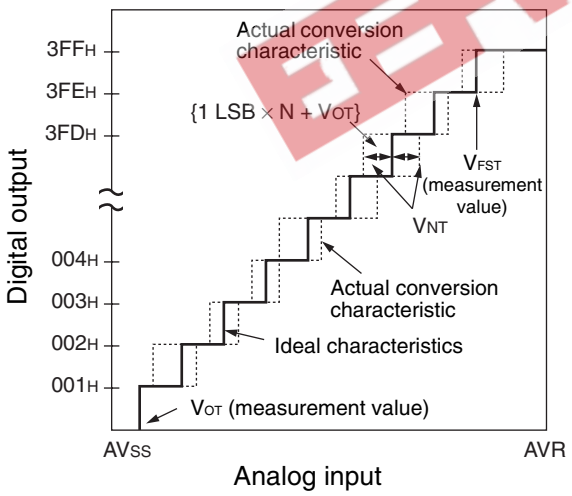
Zero transition error



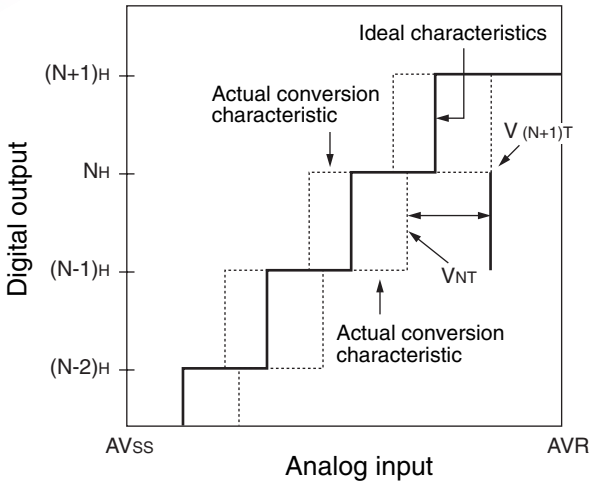
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D Converter digital output value
V_{NT} : A voltage at which digital output transits from $(N - 1)_H$ to N_H.
V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = AVR − 1.5 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	—	—	0.2*1	0.5*2	s	Excludes 00H programming prior erasure.
Sector erase time (16 Kbytes sector)		—	0.5*1	7.5*2	s	Excludes 00H programming prior erasure.
Byte programming time		—	32	3600	µs	Excludes system-level overhead.
Program/erase cycle		10000	—	—	cycle	
Power supply voltage at program/erase		4.5	—	5.5	V	
Flash memory data retention time		20*3	—	—	year	Average T_A = +85 °C

*1 : T_A = + 25 °C, V_{CC} = 5.0 V, 10000 cycles

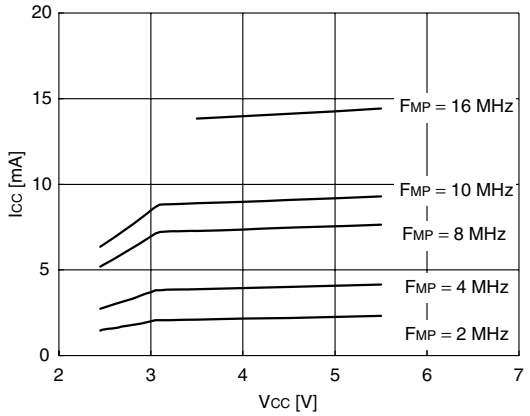
*2 : T_A = + 85 °C, V_{CC} = 4.5 V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

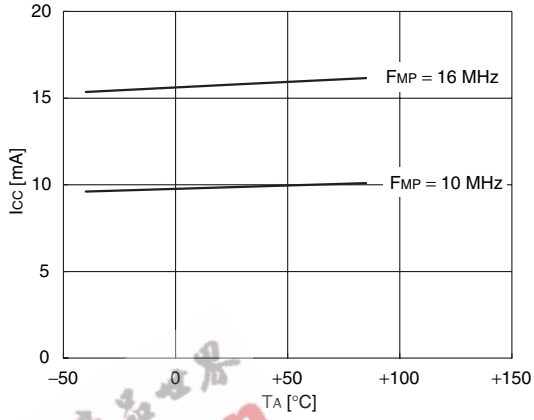
■ EXAMPLE CHARACTERISTICS

• Power supply current temperature

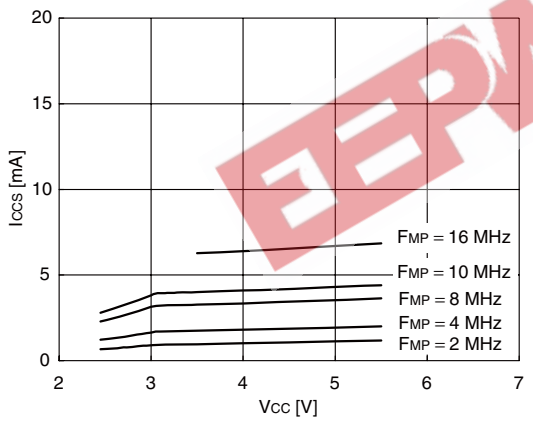
I_{CC} – V_{CC}
T_A = + 25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode, at external clock operating



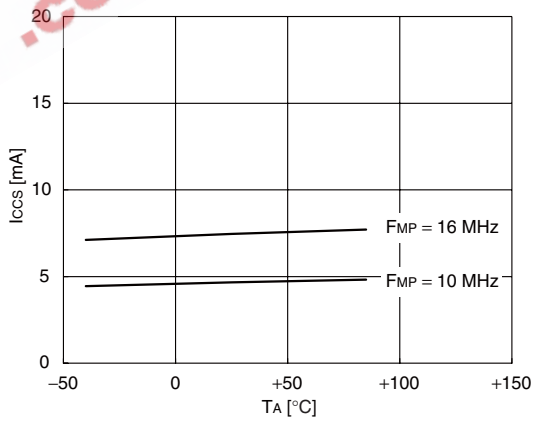
I_{CC} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode, at external clock operating



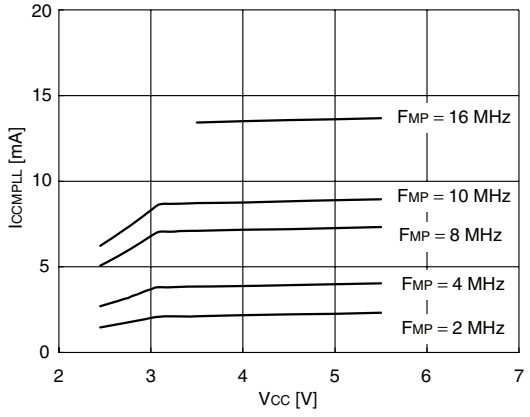
I_{CCS} – V_{CC}
T_A = + 25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode, at external clock operating



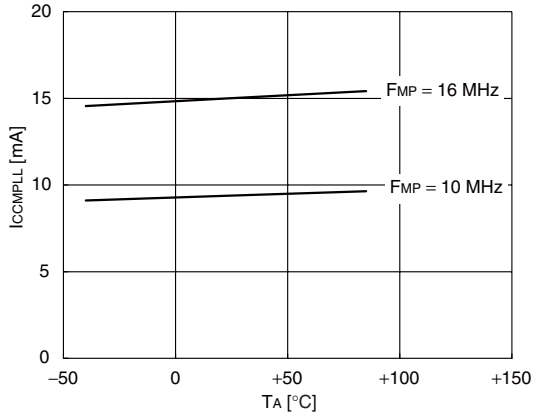
I_{CCS} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode, at external clock operating



I_{CCMPLL} – V_{CC}
T_A = + 25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz
(Multiply-by-2.5)
Main PLL mode, at external clock operating



I_{CCMPLL} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz
(Multiply-by-2.5)
Main PLL mode, at external clock operating



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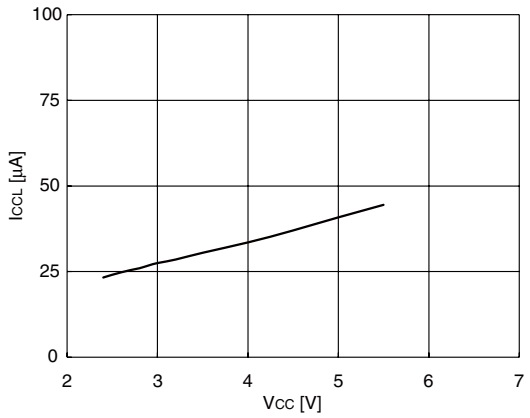
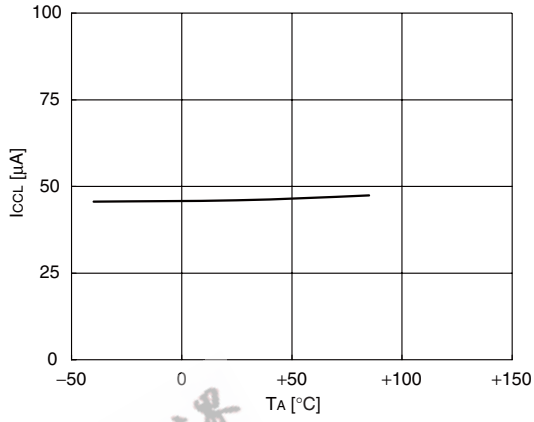
I_{CCL} – V_{CC}

T_A = + 25 °C, F_{MPL} = 16 kHz (divided by 2)
Sub clock mode, at external clock operating



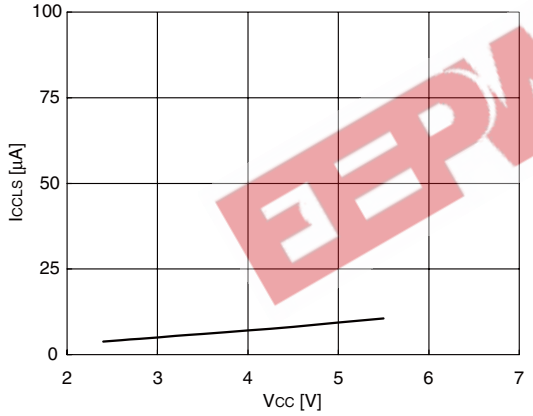
I_{CCL} – T_A

V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Sub clock mode, at external clock operating



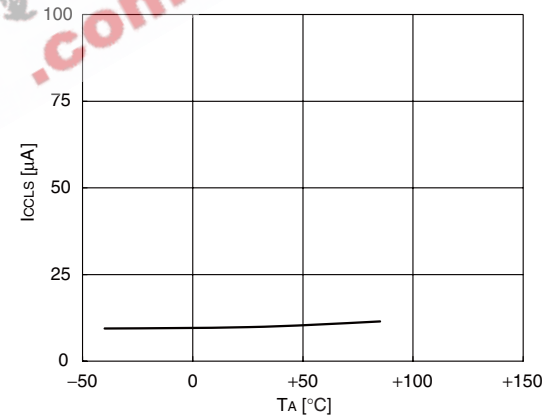
I_{CCLS} – V_{CC}

T_A = + 25 °C, F_{MPL} = 16 kHz (divided by 2)
Sub sleep mode, at external clock operating



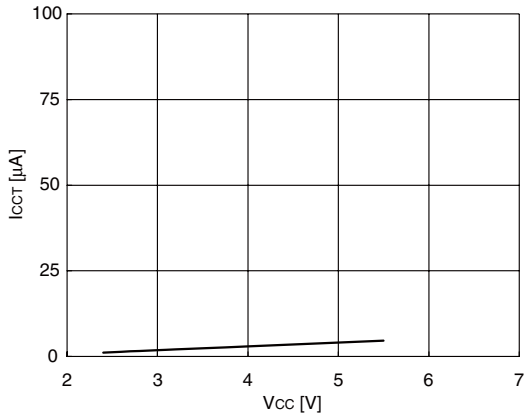
I_{CCLS} – T_A

V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Sub sleep mode, at external clock operating



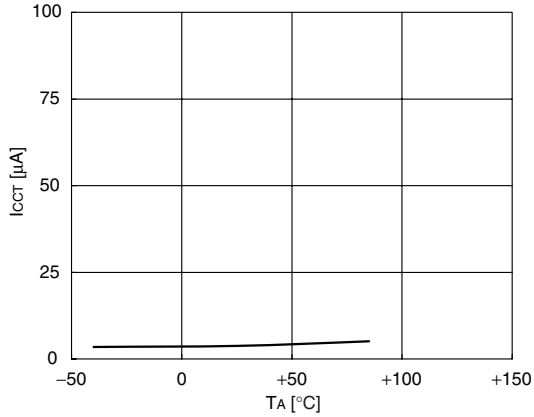
I_{CCT} – V_{CC}

T_A = + 25 °C, F_{MPL} = 16 kHz (divided by 2)
Clock mode, at external clock operating



I_{CCT} – T_A

V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Clock mode, at external clock operating



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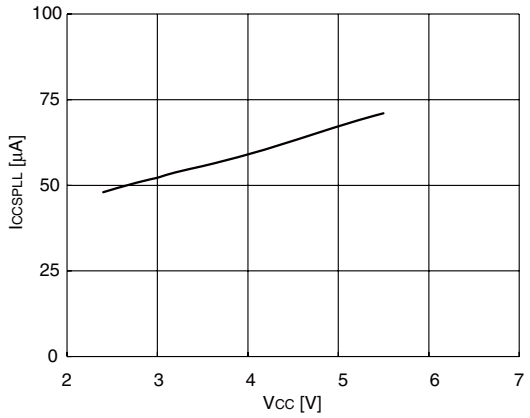
I_{CCSPLL} – V_{CC}

T_A = + 25 °C, F_{MPL} = 128 kHz (Multiply-by-4)

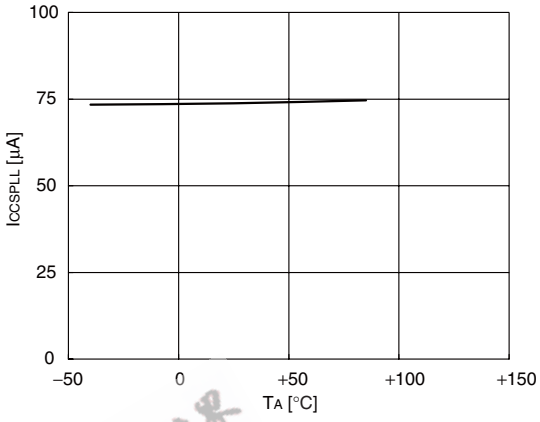
Sub PLL mode, at external clock operating



I_{CCSPLL} – T_A

V_{CC} = 5.5 V, F_{MPL} = 128 kHz (Multiply-by-4)

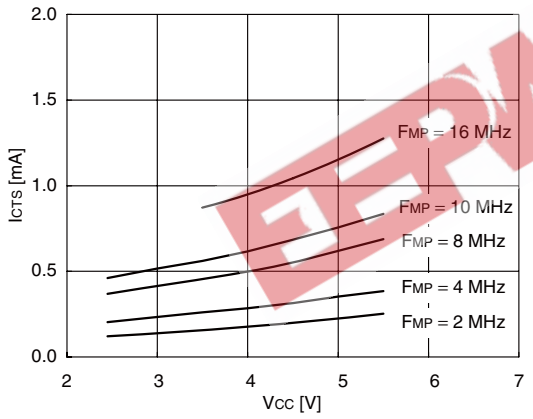
Sub PLL mode, at external clock operating



I_{CTS} – V_{CC}

T_A = + 25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)

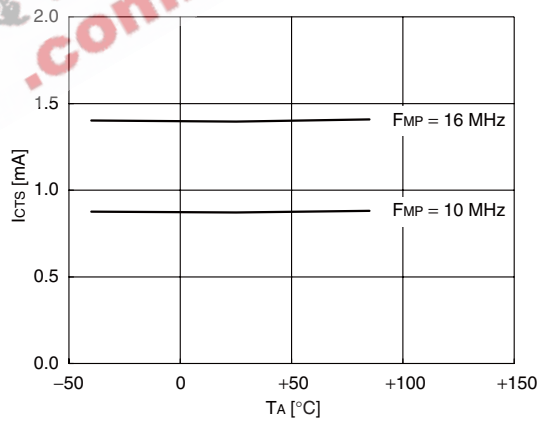
Time-base timer mode, at external clock operating



I_{CTS} – T_A

V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)

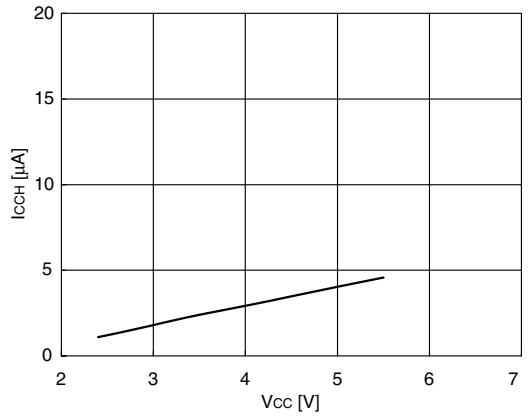
Time-base timer mode, at external clock operating



I_{CCH} – V_{CC}

T_A = + 25 °C, F_{MPL} = (stop)

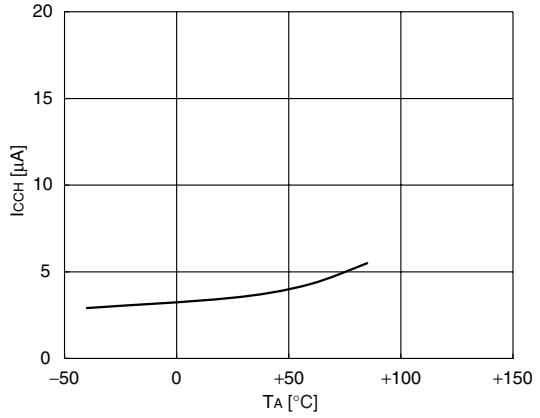
Sub stop mode, at external clock stopping



I_{CCH} – T_A

V_{CC} = 5.5 V, F_{MPL} = (stop)

Sub stop mode, at external clock stopping

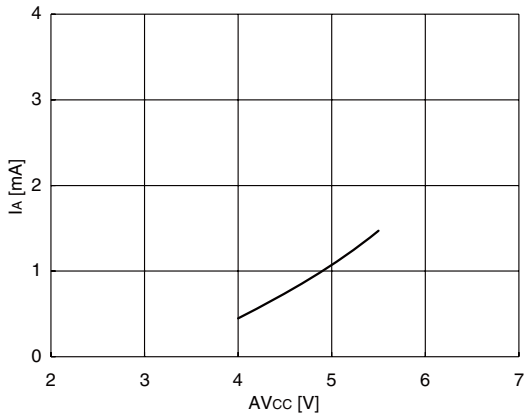


(Continued)

(Continued)

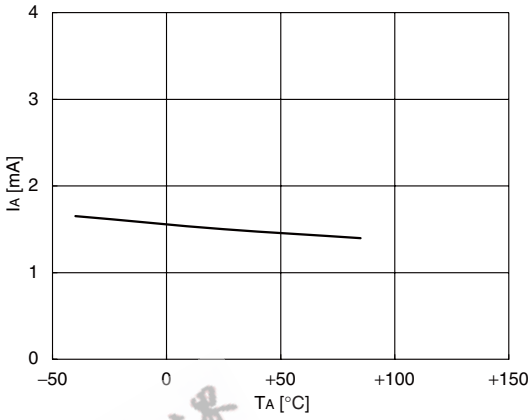
I_A – AV_{CC}

T_A = + 25 °C, F_{MP} = 16 MHz (divided by 2)
Main clock mode, at external clock operating



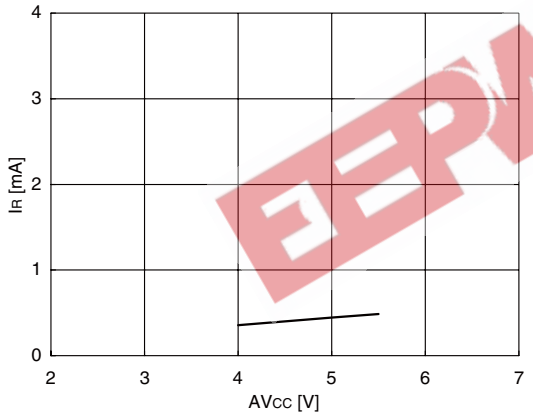
I_A – T_A

V_{CC} = 5.5 V, F_{MP} = 16 MHz (divided by 2)
Main clock mode, at external clock operating



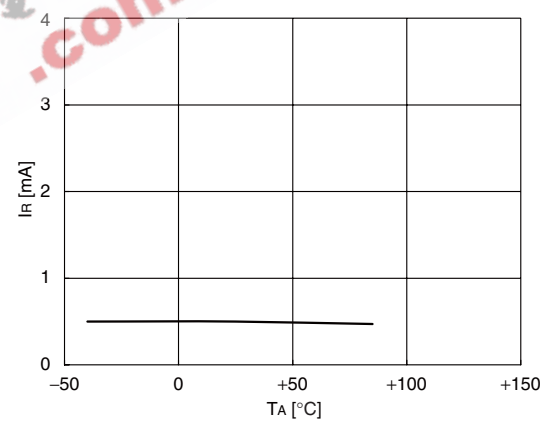
I_R – AV_{CC}

T_A = + 25 °C, F_{MP} = 16 MHz (divided by 2)
Main clock mode, at external clock operating



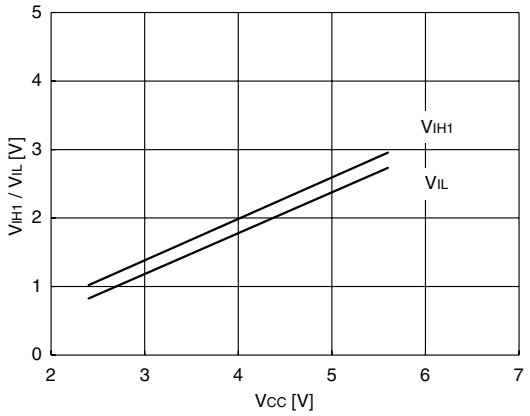
I_R – T_A

V_{CC} = 5.5 V, F_{MP} = 16 MHz (divided by 2)
Main clock mode, at external clock operating

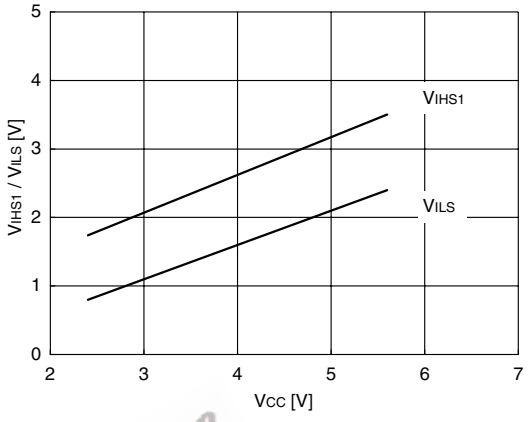


• **Input voltage**

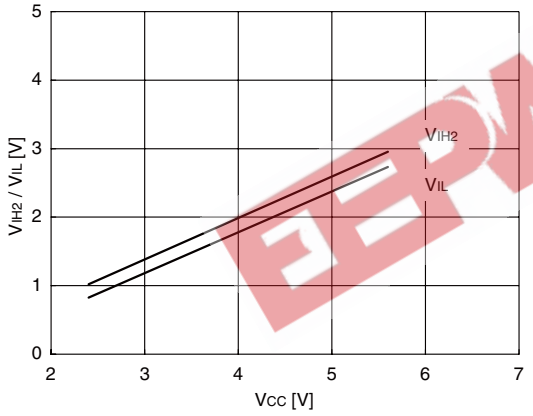
V_{IH1} – V_{CC} and V_{IL} – V_{CC}
T_A = + 25 °C



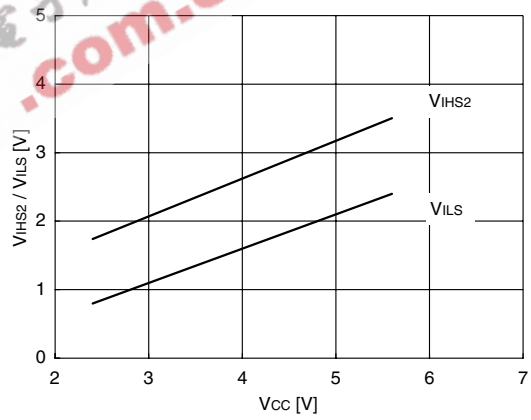
V_{IHS1} – V_{CC} and V_{ILS} – V_{CC}
T_A = + 25 °C



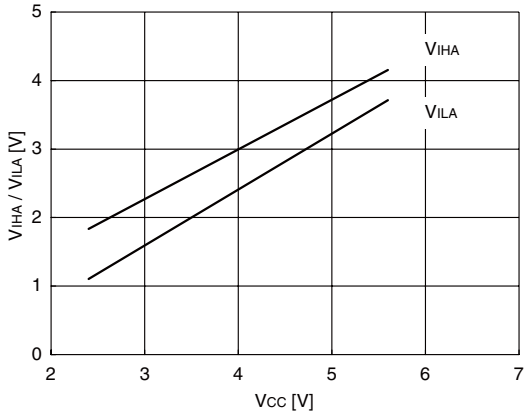
V_{IH2} – V_{CC} and V_{IL} – V_{CC}
T_A = + 25 °C



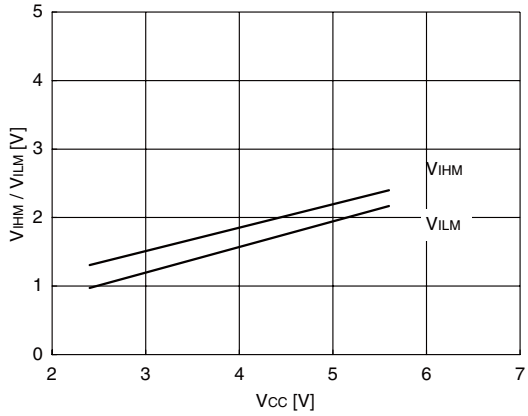
V_{IHS2} – V_{CC} and V_{ILS} – V_{CC}
T_A = + 25 °C



V_{IHA} – V_{CC} and V_{ILA} – V_{CC}
T_A = + 25 °C

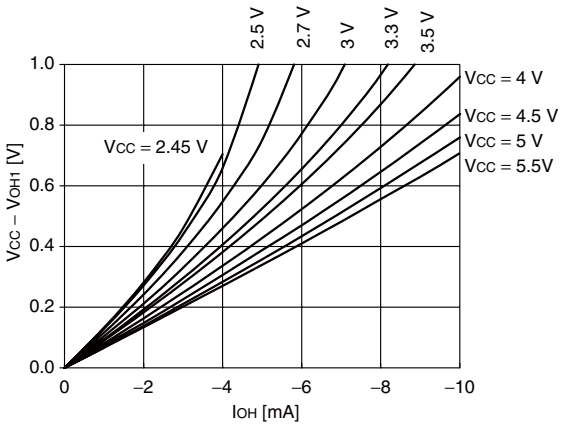


V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = + 25 °C

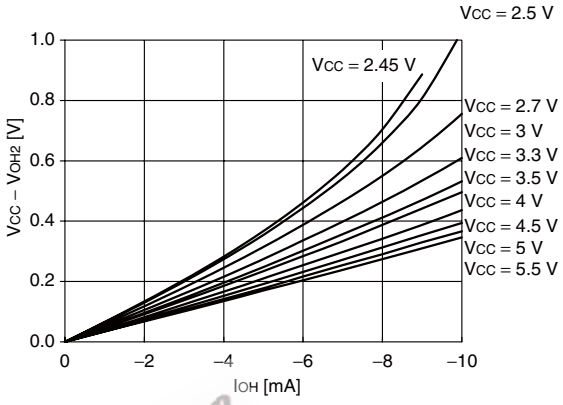


• **Output voltage**

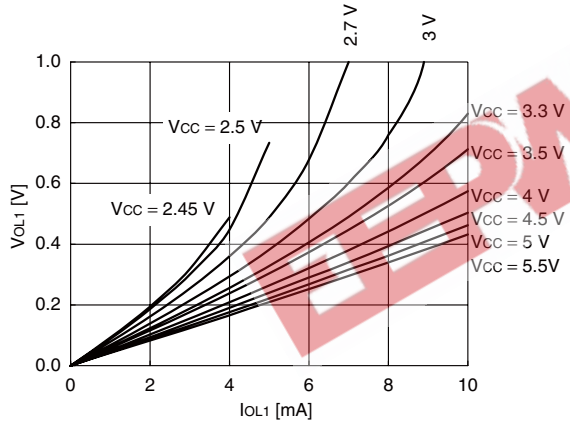
$(V_{CC}-V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



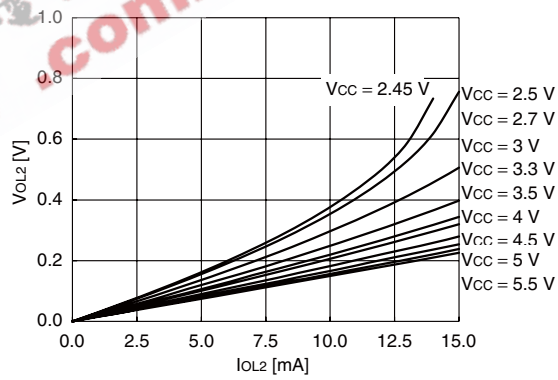
$(V_{CC}-V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



$V_{OL1} - I_{OL1}$
$T_A = +25\ °C$

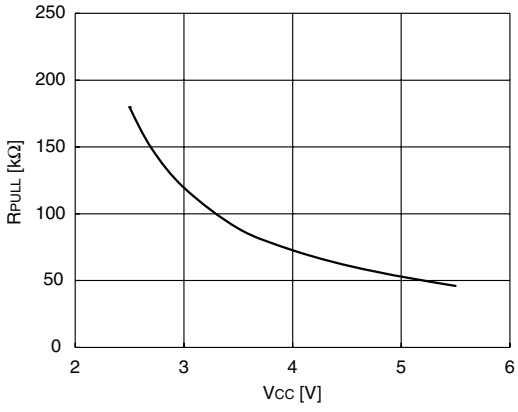


$V_{OL2} - I_{OL2}$
$T_A = +25\ °C$



• **Pull-up**

$R_{PULL} - V_{CC}$
$T_A = +25\ °C$



■ MASK OPTION

No.	Part number	MB95128MB	MB95F124MB/F124NB/F124JB MB95F126MB/126NB/F126JB MB95F128MB/F128NB/F128JB	MB95FV100D-103
	Specifying procedure	**Specify when ordering MASK**	**Setting disabled**	**Setting disabled**
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Dual-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	Specify when ordering MASK	Specified by part number	Changing by the switch on MCU board
3	Clock supervisor* • With clock supervisor • Without clock supervisor	Specify when ordering MASK	Specified by part number	Changing by the switch on MCU board
4	Reset output* • With reset output • Without reset output	Specify when ordering MASK	Specified by part number	MCU board switch set as following ; • With supervisor : Without reset output • Without supervisor : With reset output
5	Oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2)/F_{CH}$

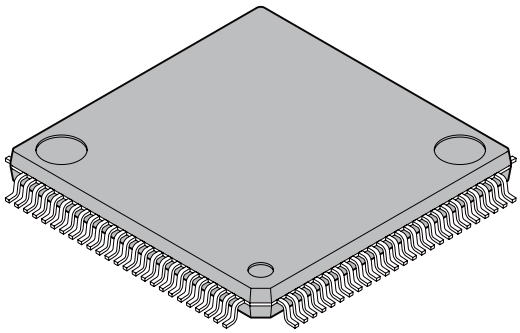
* : Refer to table below about clock mode select, low voltage detection reset, clock supervisor select and reset output.

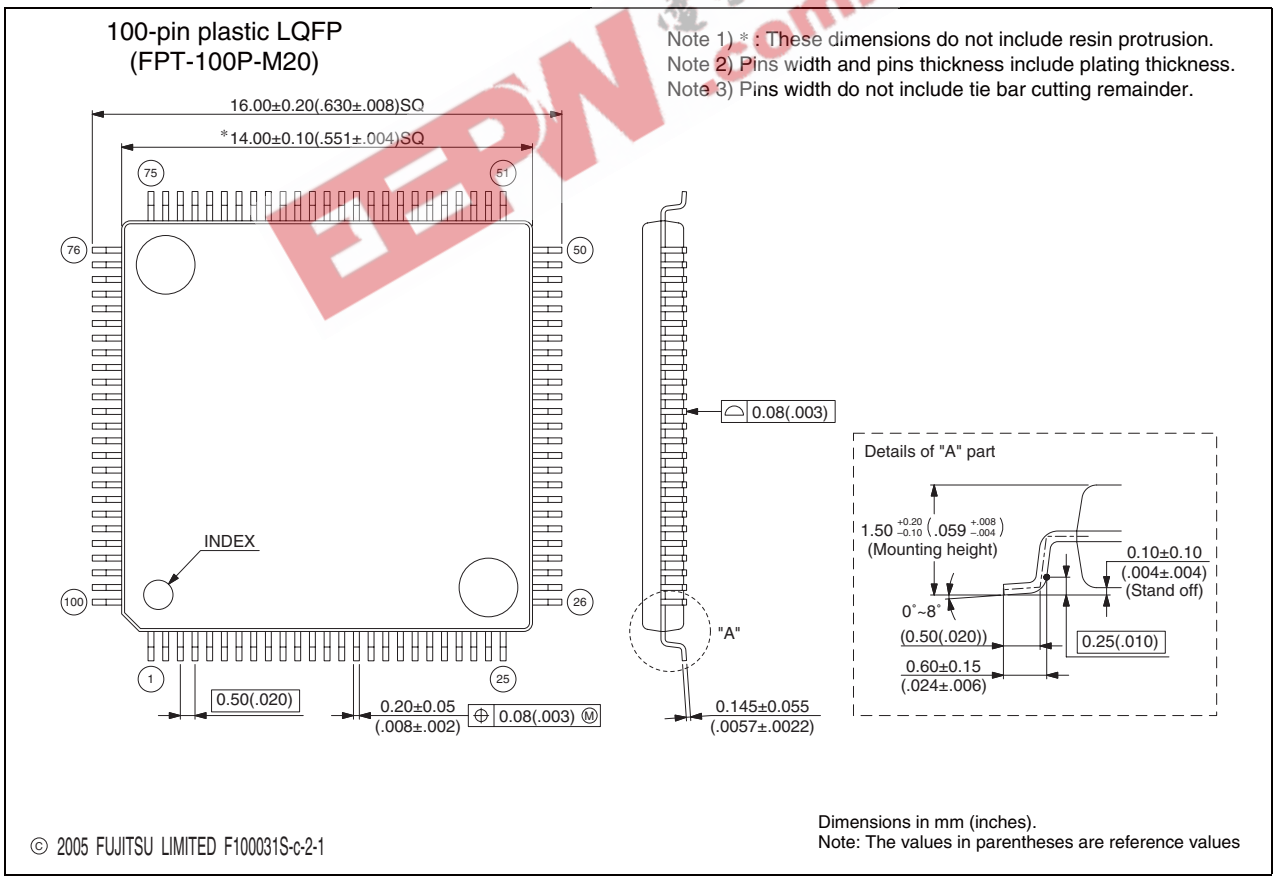
Part number	Clock mode select	Low voltage detection reset	Clock supervisor	Reset output
MB95128MB	Dual-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
MB95F124MB		No	No	Yes
MB95F124NB		Yes	No	Yes
MB95F124JB		Yes	Yes	No
MB95F126MB		No	No	Yes
MB95F126NB		Yes	No	Yes
MB95F126JB		Yes	Yes	No
MB95F128MB		No	No	Yes
MB95F128NB		Yes	No	Yes
MB95F128JB		Yes	Yes	No
MB95FV100D-103	Single-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No
	Dual-system	No	No	Yes
		Yes	No	Yes
		Yes	Yes	No

■ ORDERING INFORMATION

Part number	Package
MB95128MBPMC MB95F124MBPMC MB95F124NBPMC MB95F124JBPMC MB95F126MBPMC MB95F126NBPMC MB95F126JBPMC MB95F128MBPMC MB95F128NBPMC MB95F128JBPMC	100-pin plastic LQFP (FPT-100P-M20)
MB95128MBPF MB95F124MBPF MB95F124NBPF MB95F124JBPF MB95F126MBPF MB95F126NBPF MB95F126JBPF MB95F128MBPF MB95F128NBPF MB95F128JBPF	100-pin plastic QFP (FPT-100P-M06)
MB2146-303A (MB95FV100D-103PBT)	MCU board (224-pin plastic PFBGA (BGA-224P-M08))

■ PACKAGE DIMENSIONS

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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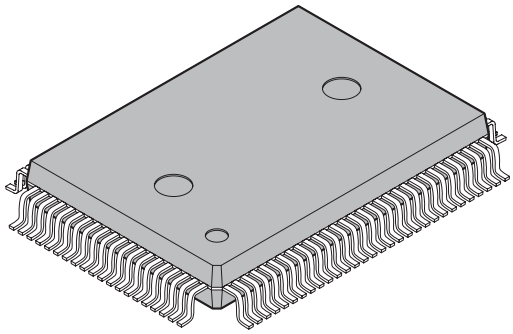
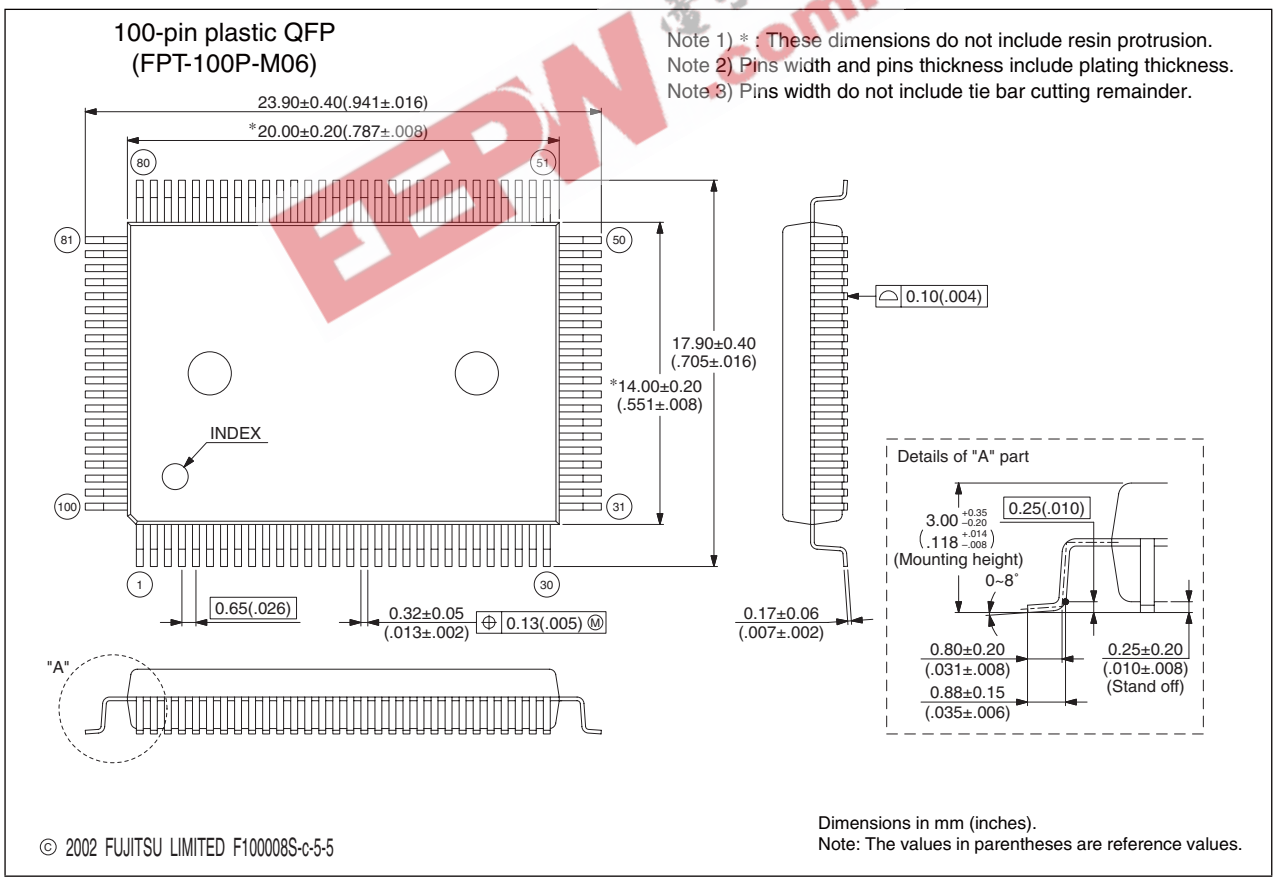
100-pin plastic QFP		
 (FPT-100P-M06)	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Added the MB95128MB (MASK ROM product)
26	■ I/O MAP	Changed as follows for R/W of Reset source register R → R/W
35	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	For the operating temperature, the max rating is changed; + 85 °C → + 105 °C
37 to 42, 44, 47 to 51, 53, 55 to 57, 59 to 63	Temperature conditions on table	Changed as follows T_A = − 40 °C to + 85 °C → T_A = − 40 °C to + 105 °C
42	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing	Added “Main PLL multiplied by 4” in the Clock frequency
44	(2) Source Clock/Machine Clock	• Changed in the remarks of source clock cycle time (when using main clock) Min : F_{CH} = 16.25 MHz, PLL multiplied by 1 → Min : F_{CH} = 8.125 MHz, PLL multiplied by 2 • Changed the footnote of *1; PLL multiplication of main clock (select from 1, 2, 2.5 multiplication) → PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication) • Added “ × 4” in the Main PLL of “• Outline of clock generation block“
45		Changed as follows • Operating voltage − Operating frequency (T_A = − 40 °C to + 85 °C) → • Operating voltage − Operating frequency (T_A = − 40 °C to + 105 °C)
46		Changed the figure of • Main PLL operation frequency
57	(8) I²C Timing	Added the *4
68 to 73	■ EXAMPLE CHARACTERISTICS	Added the ■ EXAMPLE CHARACTERISTICS

The vertical lines marked in the left side of the page show the changes.

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Edited Strategic Business Development Dept.