MC14599
See Page 6-174

MC14597B
MC14598B

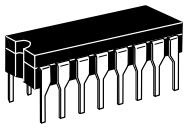
8-Bit Bus-Compatible Latches

The MC14597B and MC14598B are 8–bit latches, one addressed with an internal counter and the other addressed with an external binary address. The 8 latch–outputs are high drive, three–state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

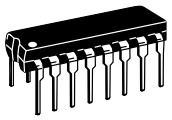
With MC14597B, a 3–bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2. A $\overline{\text{Full}}$ Flag is provided on the MC14597B to indicate the position of the Address counter.

All 8 outputs from the latches are available in parallel when $\overline{\text{Enable}}$ is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

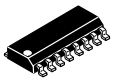
- Serial Data Input
- Three–State Bus Compatible Parallel Outputs
- Three–State Control Pin ($\overline{\text{Enable}}$) TTL Compatible Input
- Open Drain $\overline{\text{Full}}$ Flag (Multiple Latch Wire–O Ring)
- Master Reset
- Level Shifting Inputs on All Except $\overline{\text{Enable}}$
- Diode Protection — All Inputs
- Supply Voltage Range — 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range
  With Fanout as Follows:
  1 TTL Load
  4 LSTTL Loads



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

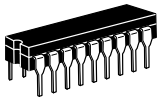


D SUFFIX
SOIC
CASE 751B

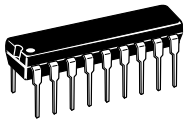
ORDERING INFORMATION

MC14597BCP	Plastic
MC14597BCL	Ceramic
MC14597BDW	SOIC

T_A = – 55° to 125°C for all packages.



L SUFFIX
CERAMIC
CASE 726



P SUFFIX
PLASTIC
CASE 707

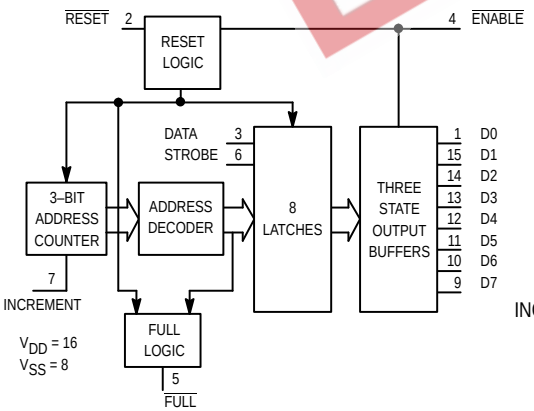
ORDERING INFORMATION

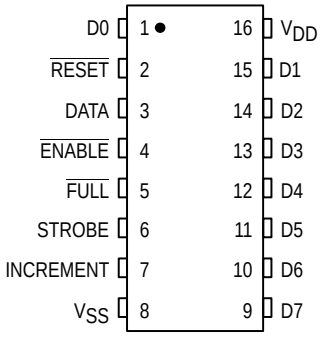
MC14598BCP	Plastic
MC14598BCL	Ceramic

T_A = – 55° to 125°C for all packages.

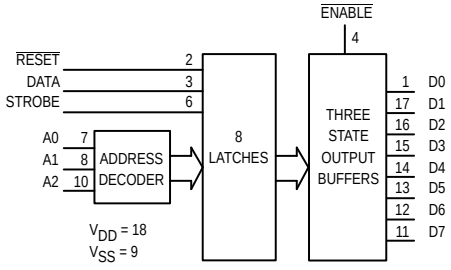
BLOCK DIAGRAMS

MC14597B





MC14598B

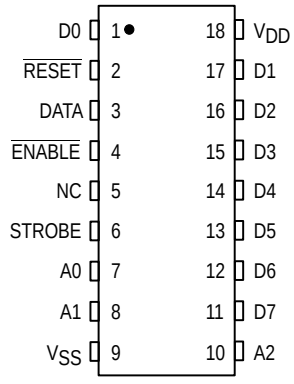


OUTPUT TRUTH TABLE

$\overline{\text{Enable}}$	Outputs
1	High Impedance
0	D_n

D_n = State of nth latch

NC = NO CONNECTION



REV 3
1/94

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}	Input Voltage, Enable (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
V_{in}	Input Voltage, All other Inputs (DC or Transient)	– 0.5 to V_{DD} + 12	V
V_{out}	Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, Iout	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
"P and D/DW" Packages: – 7.0 mW/C From 65°C To 125°C Ceramic
"L" Packages: – 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage** — $\overline{\text{Enable}}$	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	—	0.8	—	1.1	0.8	—	0.8	
(V_O = 9.0 or 1.0 Vdc)			10	—	1.6	—	2.2	1.6	—	1.6	
(V_O = 13.5 or 1.5 Vdc)			15	—	2.4	—	3.4	2.4	—	2.4	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	2.0	—	2.0	1.9	—	2.0	—	
(V_O = 1.0 or 9.0 Vdc)			10	6.0	—	6.0	3.1	—	6.0	—	
(V_O = 1.5 or 13.5 Vdc)			15	10	—	10	4.3	—	10	—	
Input Voltage Other Inputs	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc)	"1" Level	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)			10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)			15	11	—	11	8.25	—	11	—	
Output Drive Current ($\overline{\text{Full}}$ — Sink Only)	Source	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc)			5.0	– 1.0	–	– 1.0	– 2.0	—	– 1.0	—	
(V_{OH} = 9.5 Vdc)			10	—	—	—	– 6.0	—	—	—	
(V_{OH} = 13.5 Vdc)			1 5	—	—	—	– 12	—	—	—	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	1.6	—	1.6	3.2	—	1.6	—	mAdc
(V_{OL} = 0.5 Vdc)			10	—	—	—	6.0	—	—	—	
(V_{OL} = 1.5 Vdc)			15	—	—	—	12	—	—	—	
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Three–State Leakage Current		I_{TL}	15	—	±0.1	—	±0.00001	±0.1	—	±3.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	
**Total Supply Current at an External Load Capacitance of 130 pF		I_T	5.0	I_T = (2.0 µA/kHz) f + I_{DD}							µAdc
			10	I_T = (4.0 µA/kHz) f + I_{DD}							
				I_T = (6.0 µA/kHz) f + I_{DD}							

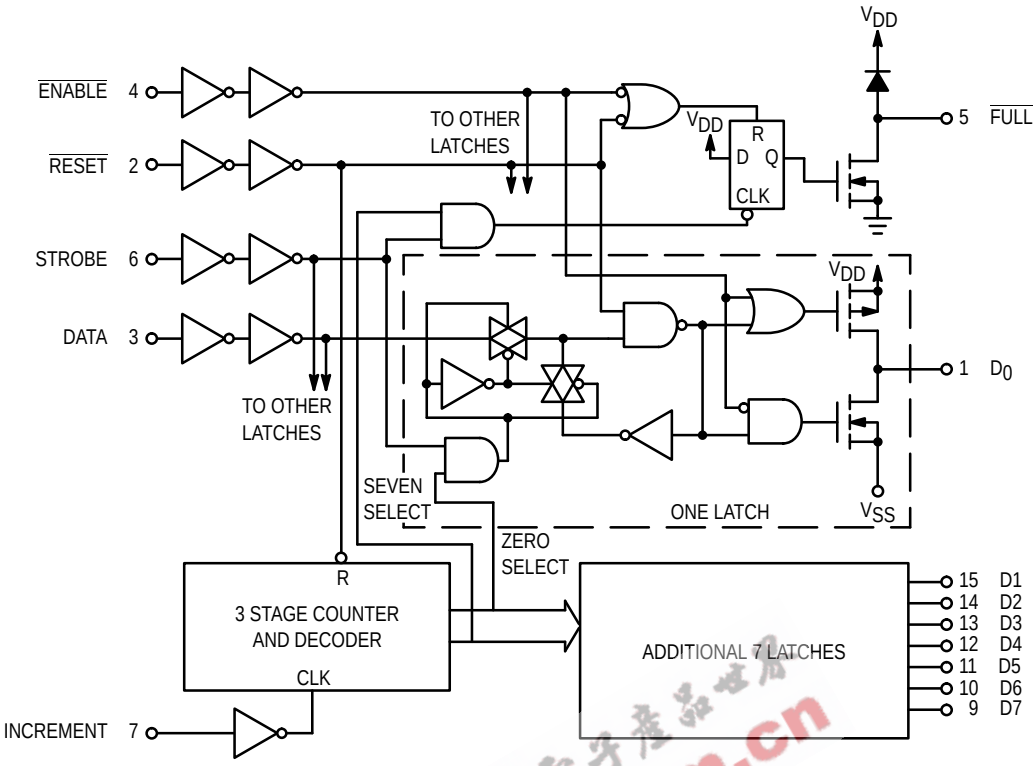
†Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
** The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (T_A = 25°C, C_L = 130 pF + 1 TTL Load)

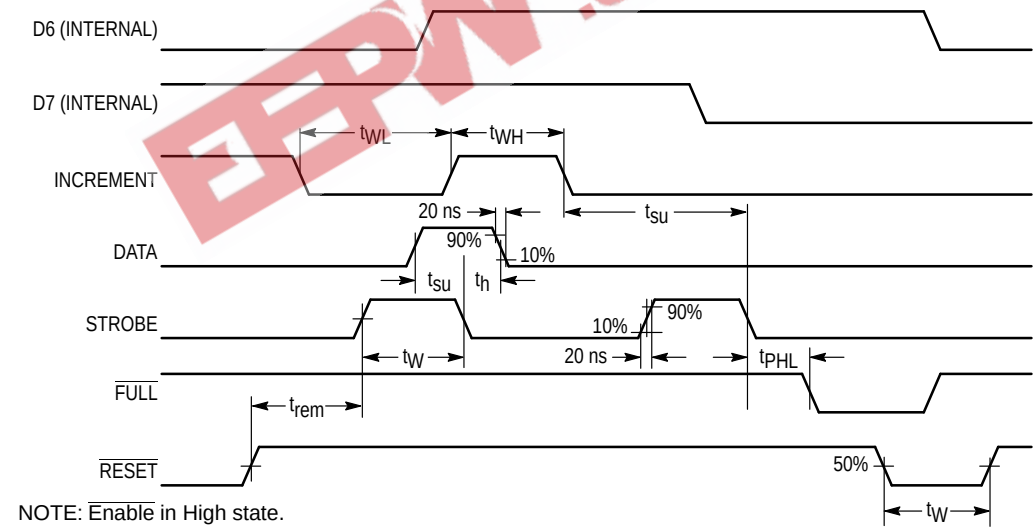
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (0.5 ns/pF) C_L + 35 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.2 ns/pF) C_L + 25 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.16 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
$\overline{\text{Enable}}$ to Output		5.0	—	160	320	
		10	—	125	250	
		15	—	100	200	
Strobe to Output		5.0	—	200	400	
		10	—	100	200	
		15	—	80	160	
Strobe to $\overline{\text{Full}}$ (MC14597B only)		5.0	—	200	400	
		10	—	100	200	
		15	—	80	160	
$\overline{\text{Reset}}$ to Output		5.0	—	175	350	
		10	—	90	180	
		15	—	70	140	
Pulse Width	t_{WH}, t_{WL}					ns
$\overline{\text{Enable}}$		5.0	320	160	—	
		10	240	120	—	
		15	160	80	—	
Strobe		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
Increment (MC14597B only)		5.0	200	100	—	
		10	100	50	—	
		15	80	40	—	
$\overline{\text{Reset}}$		5.0	300	150	—	
		10	160	80	—	
		15	100	50	—	
Setup Time	t_{su}					ns
Data		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Address (MC14598B only)		5.0	200	100	—	
		10	100	50	—	
		15	70	35	—	
Increment (MC14597B only)		5.0	400	200	—	
		10	200	100	—	
		15	170	85	—	
Hold Time	t_h					ns
Data		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
Address (MC14598B only)		5.0	100	50	—	
		10	50	25	—	
		15	35	20	—	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	20	– 25	—	ns
		10	20	– 15	—	
		15	20	– 10	—	

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

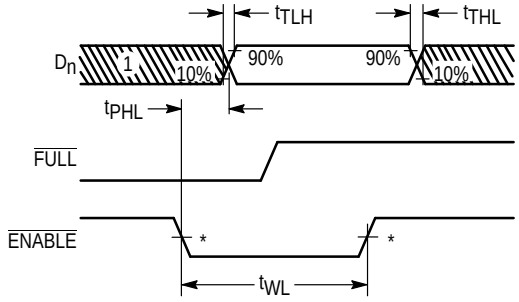
MC14597B FUNCTION DIAGRAM



MC14597B TIMING DIAGRAMS



NOTE: $\overline{\text{Enable}}$ in High state.

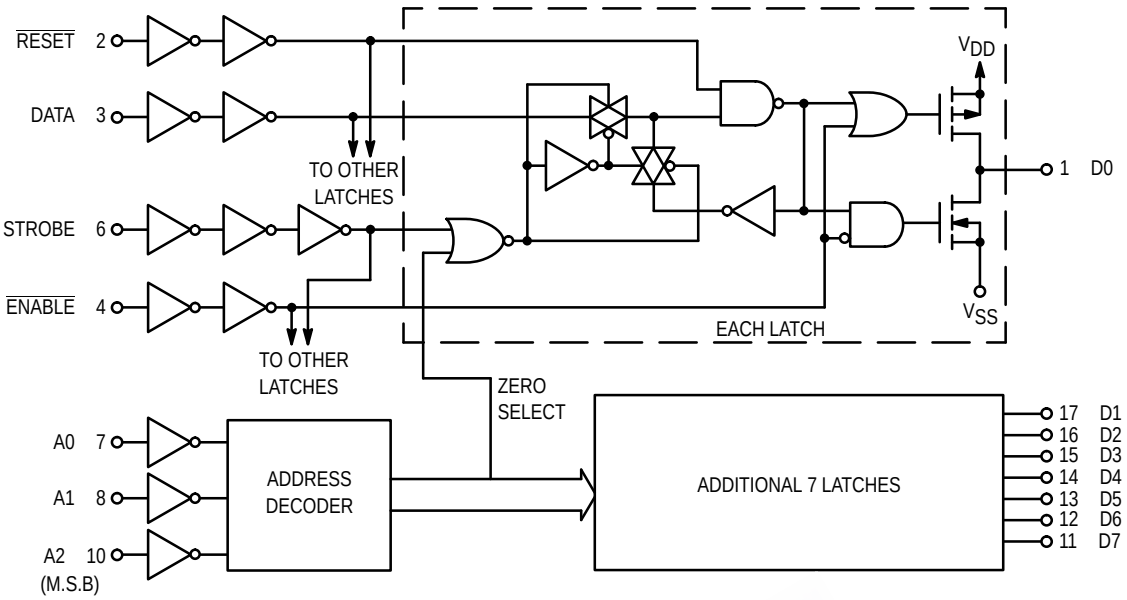


* 1.4 V with V_{DD} = 5.0 V

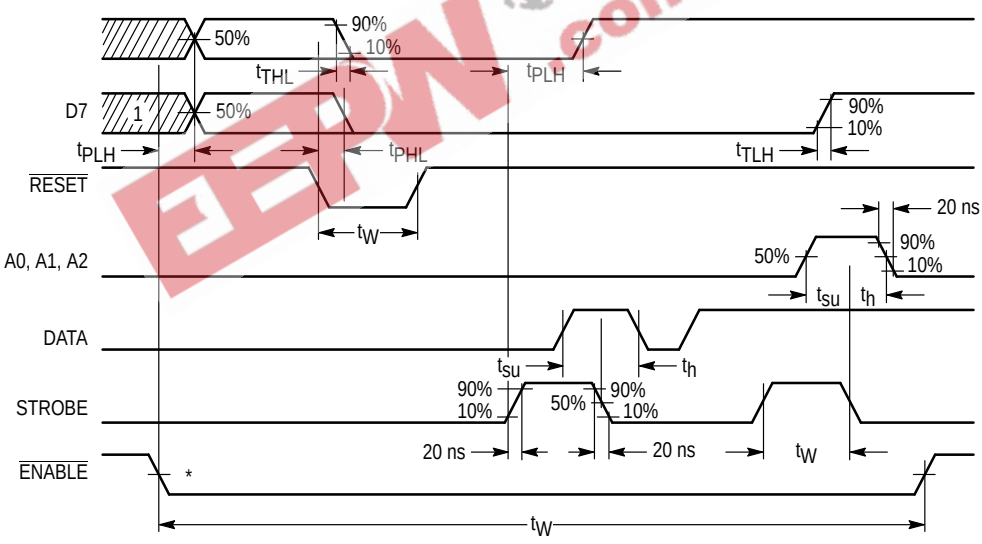
NOTES:

1. High–impedance output state (another device controls bus).
2. $\overline{\text{Reset}}$ in High state.

MC14598B FUNCTION DIAGRAM



MC14598B TIMING DIAGRAM



* 1.4 V with V_{DD} = 5.0 V

NOTES:

1. High–impedance output state (another device controls bus).
2. Output Load as for MC14597B.

LATCH TRUTH TABLE

Strobe	$\overline{\text{Reset}}$	Address Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

* = No change in state of latch

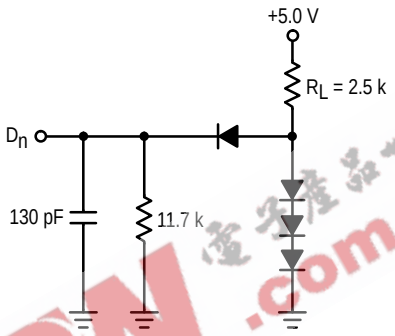
X = Don't care

TRUTH TABLE FOR MC14597B

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
⌥	X	1	Count Up	—
⌤	X	1	No Change	—
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

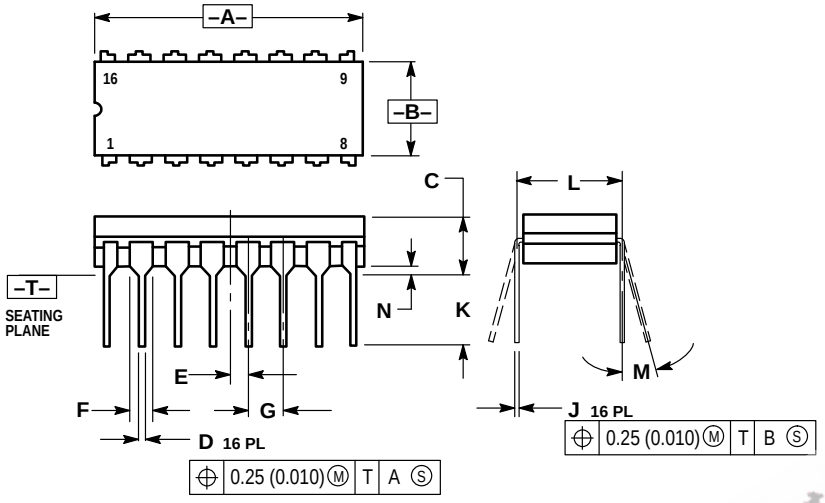
X = Don't care

TEST LOAD
ALL OUTPUTS



OUTLINE DIMENSIONS

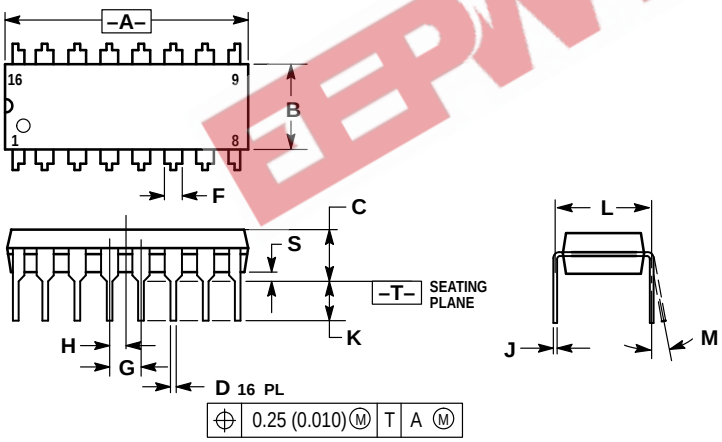
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

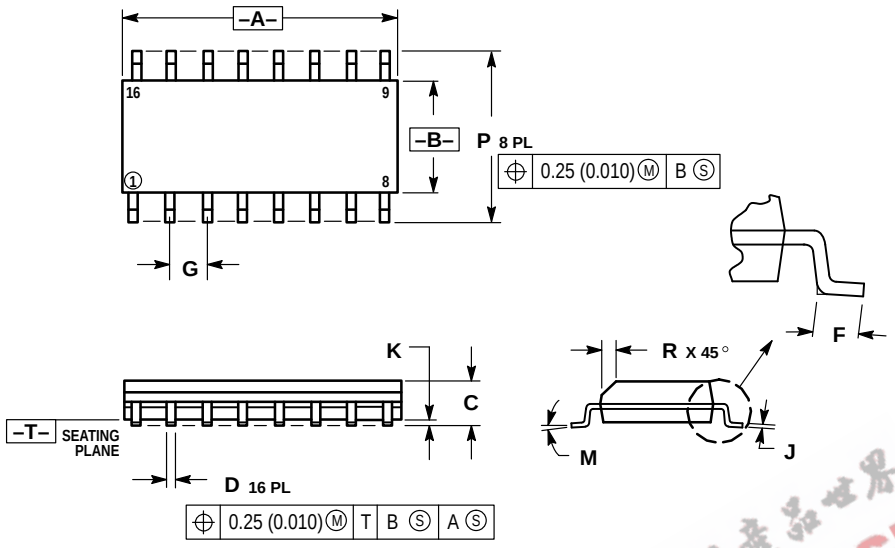


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

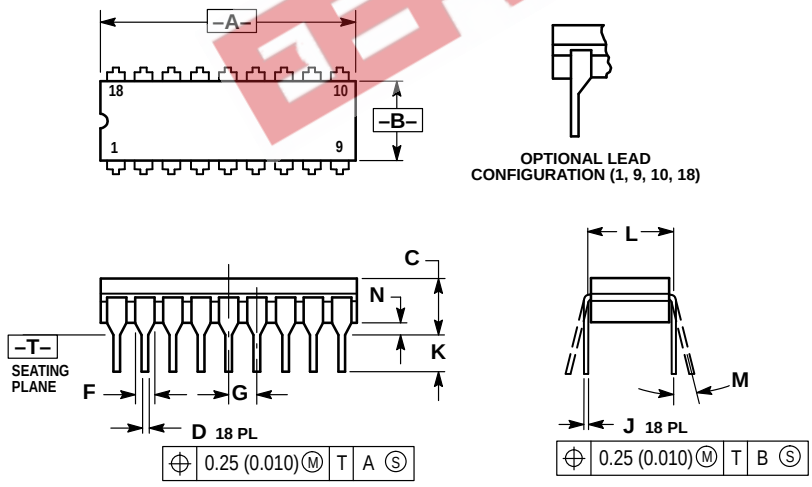
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

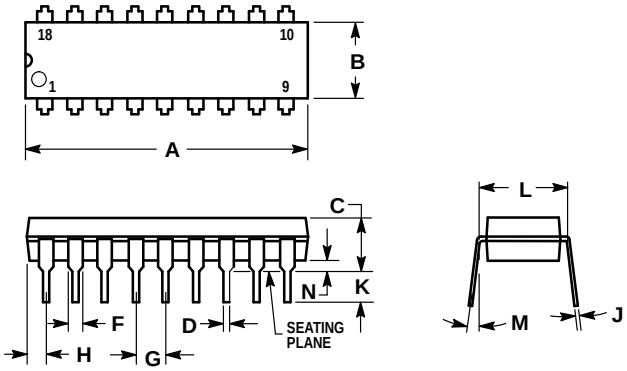
L SUFFIX
CERAMIC DIP PACKAGE
CASE 726–04
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.880	0.910	22.35	23.11
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.021	0.38	0.53
F	0.055	0.070	1.40	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.170	3.18	4.32
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

P SUFFIX
PLASTIC DIP PACKAGE
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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