



MOTOROLA

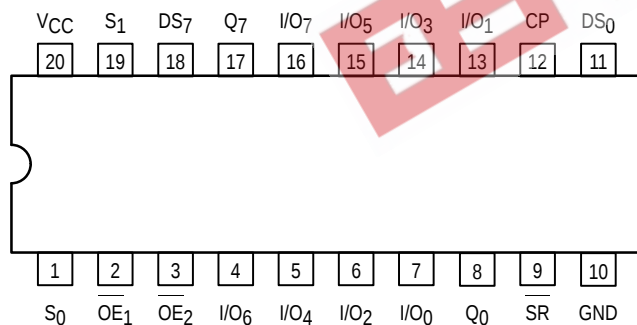
MC74AC323 MC74ACT323

Advance Information

8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

The MC74AC323/74ACT323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the MC74AC299/74ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q₀ and Q₇ to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

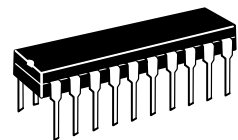
- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- ACT323 Has TTL Compatible Inputs



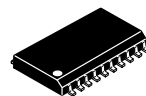
PIN NAMES

CP	Clock Pulse Input
DS ₀	Serial Data Input for Right Shift
DS ₇	Serial Data Input for Left Shift
S ₀ , S ₁	Mode Select Inputs
SR	Synchronous Master Reset
OE ₁ , OE ₂	3-State Output Enable Inputs
I/O ₀ –I/O ₇	Multiplexed Parallel Data Inputs or 3-State Parallel Data Outputs
Q ₀ , Q ₇	Serial Outputs

8-INPUT UNIVERSAL SHIFT/
STORAGE REGISTER WITH
SYNCHRONOUS RESET
AND COMMON I/O PINS

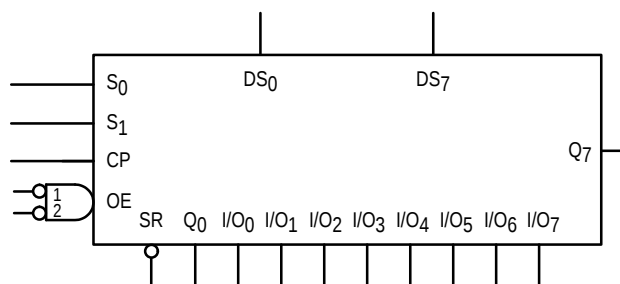


N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-04
PLASTIC

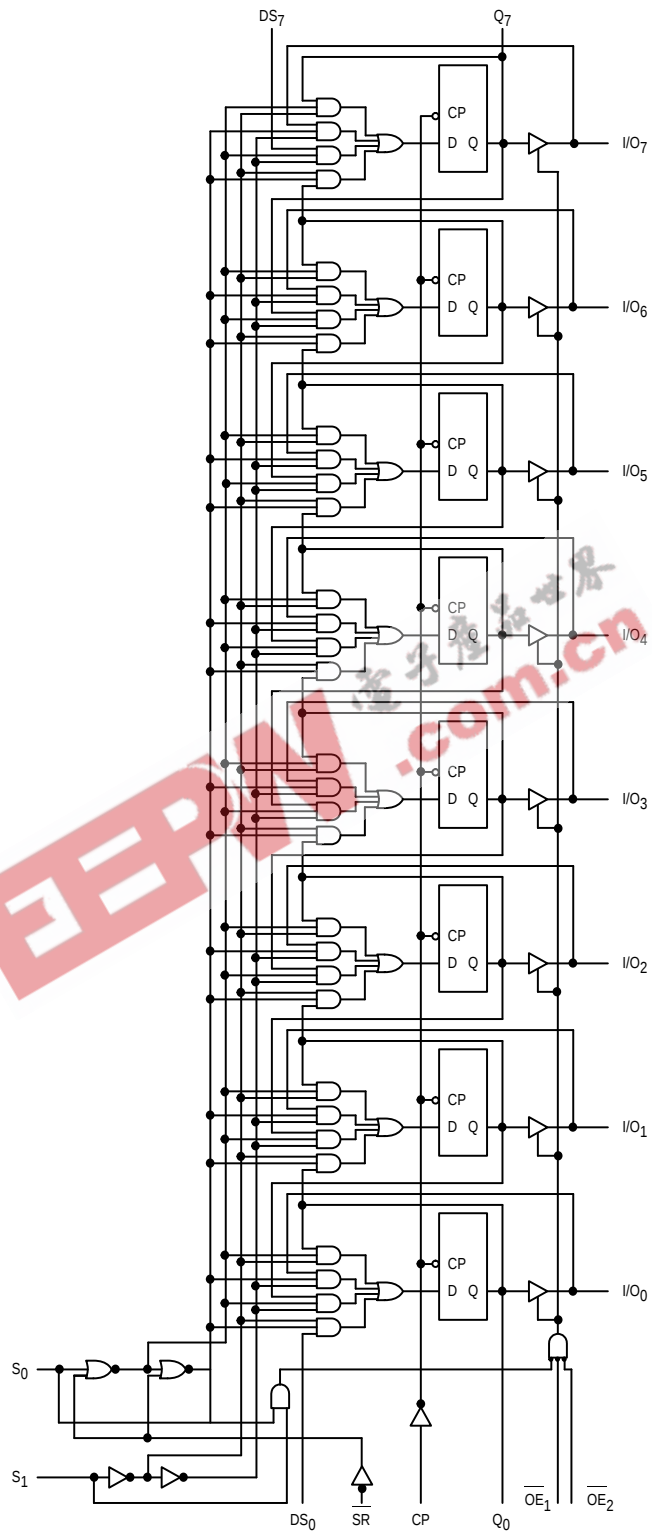
LOGIC SYMBOL



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC74AC323 MC74ACT323

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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FUNCTIONAL DESCRIPTION

The MC74AC323/74ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3 state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on SR overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other

state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either OE_1 or OE_2 disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

TRUTH TABLE

Inputs				Response
SR	S_1	S_0	CP	
L	X	X	$\downarrow$	Synchronous Reset; $Q_0 - Q_7 = \text{LOW}$
H	H	H	$\downarrow$	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	$\downarrow$	Shift Right; $DS_0 \rightarrow Q_0, Q_0 \rightarrow Q_1$, etc.
H	H	L	$\downarrow$	Shift Left; $DS_7 \rightarrow Q_7, Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level $\downarrow$ = LOW-to-HIGH Clock Transition

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 \text{ V}$		150		ns/V
		$V_{CC} @ 4.5 \text{ V}$		40		
		$V_{CC} @ 5.5 \text{ V}$		25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 \text{ V}$		10		ns/V
		$V_{CC} @ 5.5 \text{ V}$		8.0		
T_J	Junction Temperature (PDIP)				140	°C
T_A	Operating Ambient Temperature Range		-40	25	85	°C
I_{OH}	Output Current — High				-24	mA
I_{OL}	Output Current — Low				24	mA

1. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Unit	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OZT}	Maximum 3-State Current	5.5		±0.6	±6.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.

† Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Max	Min	Max		
f _{max}	Maximum Input Frequency	3.3 5.0					MHz	3-3
t _{PLH}	Propagation Delay CP to Q0 or Q7	3.3 5.0					ns	3-6
t _{PHL}	Propagation Delay CP to Q0 or Q7	3.3 5.0					ns	3-6
t _{PLH}	Propagation Delay CP to I/O _n	3.3 5.0					ns	3-6
t _{PHL}	Propagation Delay CP to I/O _n	3.3 5.0					ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0					ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0					ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0					ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0					ns	3-8

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0				ns	3-9
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	3.3 5.0				ns	3-9
t _s	Setup Time, HIGH or LOW/ I/O _n , DS ₀ , DS ₇ to CP	3.3 5.0				ns	3-9
t _h	Hold Time, HIGH or LOW/ I/O _n , DS ₀ , DS ₇ to CP	3.3 5.0				ns	3-9
t _s	Setup Time, HIGH or LOW SR to CP	3.3 5.0				ns	3-9
t _h	Hold Time, HIGH or LOW SR to CP	3.3 5.0				ns	3-9
t _w	CP Pulse Width HIGH or LOW	3.3 5.0				ns	3-6

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} − 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA	
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZT}	Maximum 3-State Current	5.5		±0.6	±6.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

* All outputs loaded; thresholds on input associated with output under test.

† Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Input Frequency	5.0	120	125		110		MHz	3-3
t _{PLH}	Propagation Delay CP to Q ₀ or Q ₇	5.0	5.0	9.0	12.5	4.0	14	ns	3-6
t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	5.0	5.0	9.0	13.5	4.5	15	ns	3-6
t _{PLH}	Propagation Delay CP to I/O _n	5.0	5.0	8.5	12.5	4.5	14.5	ns	3-6
t _{PHL}	Propagation Delay CP to I/O _n	5.0	6.0	10	14.5	5.0	16	ns	3-6
t _{PZH}	Output Enable Time	5.0	3.5	7.5	11	3.0	12.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	3.5	7.5	11.5	3.0	13	ns	3-8
t _{PHZ}	Output Disable Time	5.0	4.0	8.5	12.5	3.0	13.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	3.0	8.0	11.5	2.5	12.5	ns	3-8

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	2.0	5.0	5.0	ns	3-9
t _h	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	0	1.5	1.5	ns	3-9
t _s	Setup Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0	1.0	4.0	4.5	ns	3-9
t _h	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0	0	1.0	1.0	ns	3-9
t _s	Setup Time, HIGH or LOW SR to CP	5.0	1.0	2.5	2.5	ns	3-9
t _h	Setup Time, HIGH or LOW SR to CP	5.0	0	1.0	1.0	ns	3-9
t _w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns	3-6

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

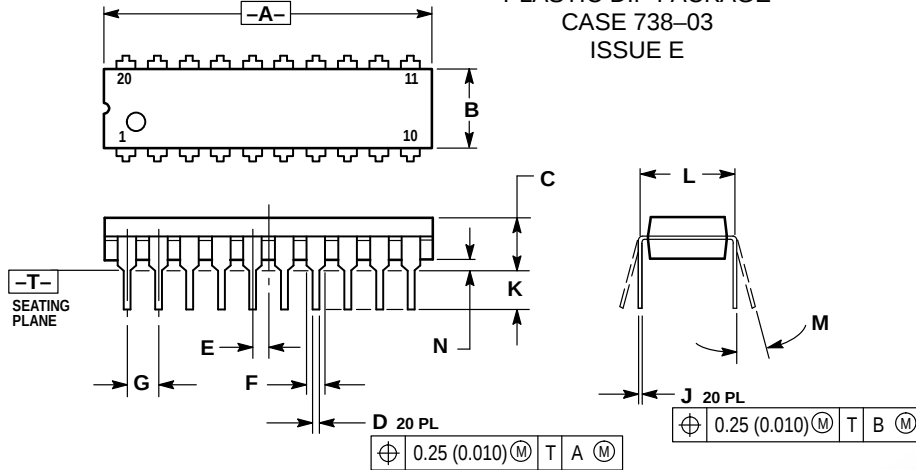
CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	170	pF	V _{CC} = 5.0 V

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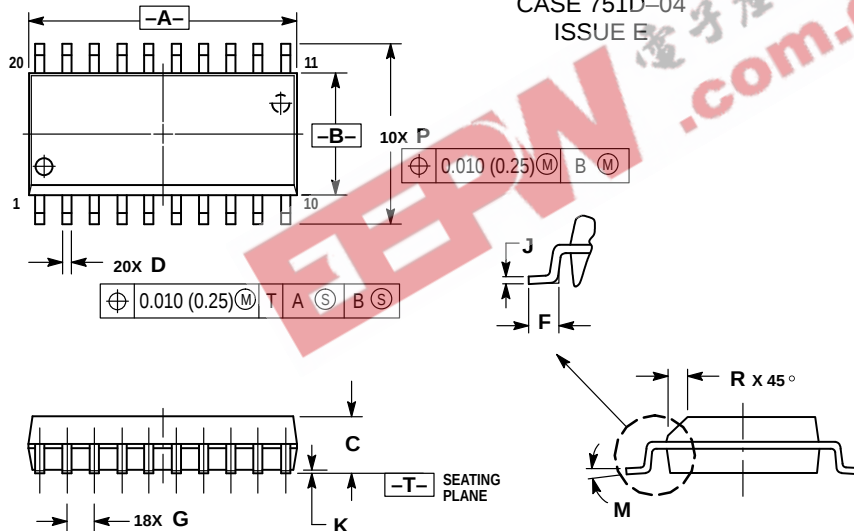
OUTLINE DIMENSIONS

N SUFFIX PLASTIC DIP PACKAGE CASE 738-03 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DW SUFFIX PLASTIC SOIC PACKAGE CASE 751D-04 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

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MC74AC323/D

