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MC68HC05D9

Technical Summary
8-bit microcomputer with PWM outputs and LED drive

The MC68HC05D9 is a member of the MC68HC05 family derived from the MC68HC05C8, and ultimately from the MC68HC05C4 microcomputer. The MC68HC05D9 is a member of the MC68HC05 family derived from the MC68HC05C8, and ultimately from the MC68HC05C4 microcomputer. Its special features include a high current output port capable of driving LEDs and 5 PWM (Pulse Width Modulator) channels, of 6-bits each, suitable for use in applications such as TV. The pinout and instruction set are compatible with the MC68HC05C9 except in the case of Port D which supports the PWM output and timer I/O functions and the SCI. For more detailed information, contact your local Motorola sales office.

The main features of the MC68HC05D9 are listed below:

- 68HC05 core
- 16K bytes of ROM
- 352 bytes of RAM
- Five 6-bit PWM channels operating at 30KHz
- High current LED output port
- Software configurable memory configurations
- COP watchdog timer + clock monitor
- Serial Communications Interface (SCI)
- Pin compatible with MC68HC05C9
- Self-check mode
- 40-pin DIL or 44-pin PLCC
- 16-bit timer with Input Capture and Output Compare functions

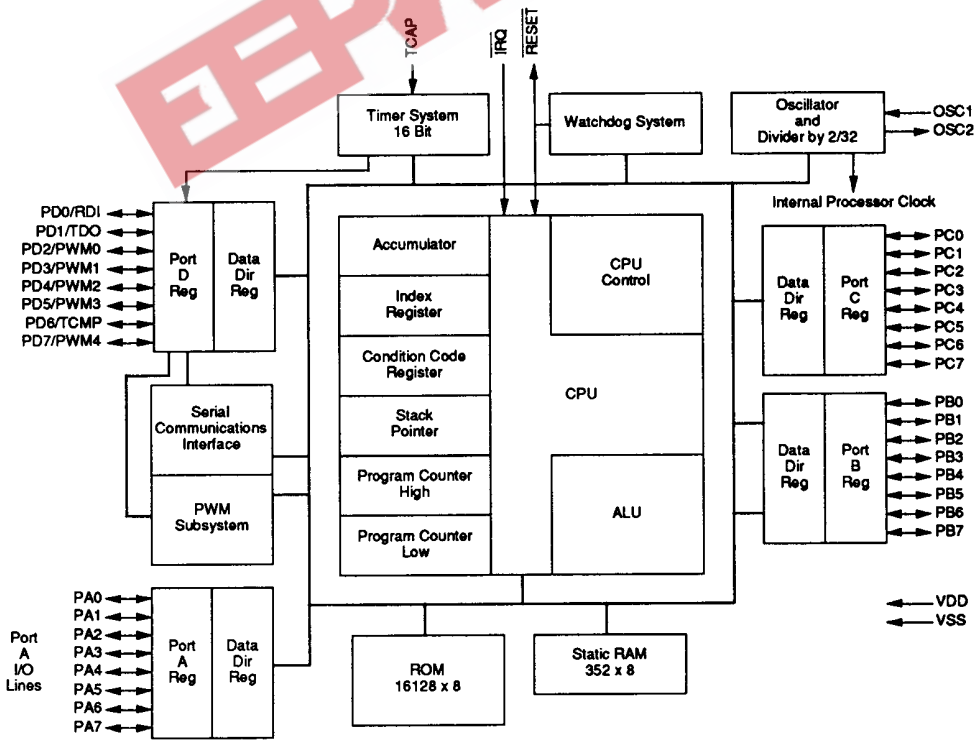

Figure 1. MC68HC05D9 Block Diagram

This document contains information on a new product. Specifications and other information herein are therefore subject to change without notice.

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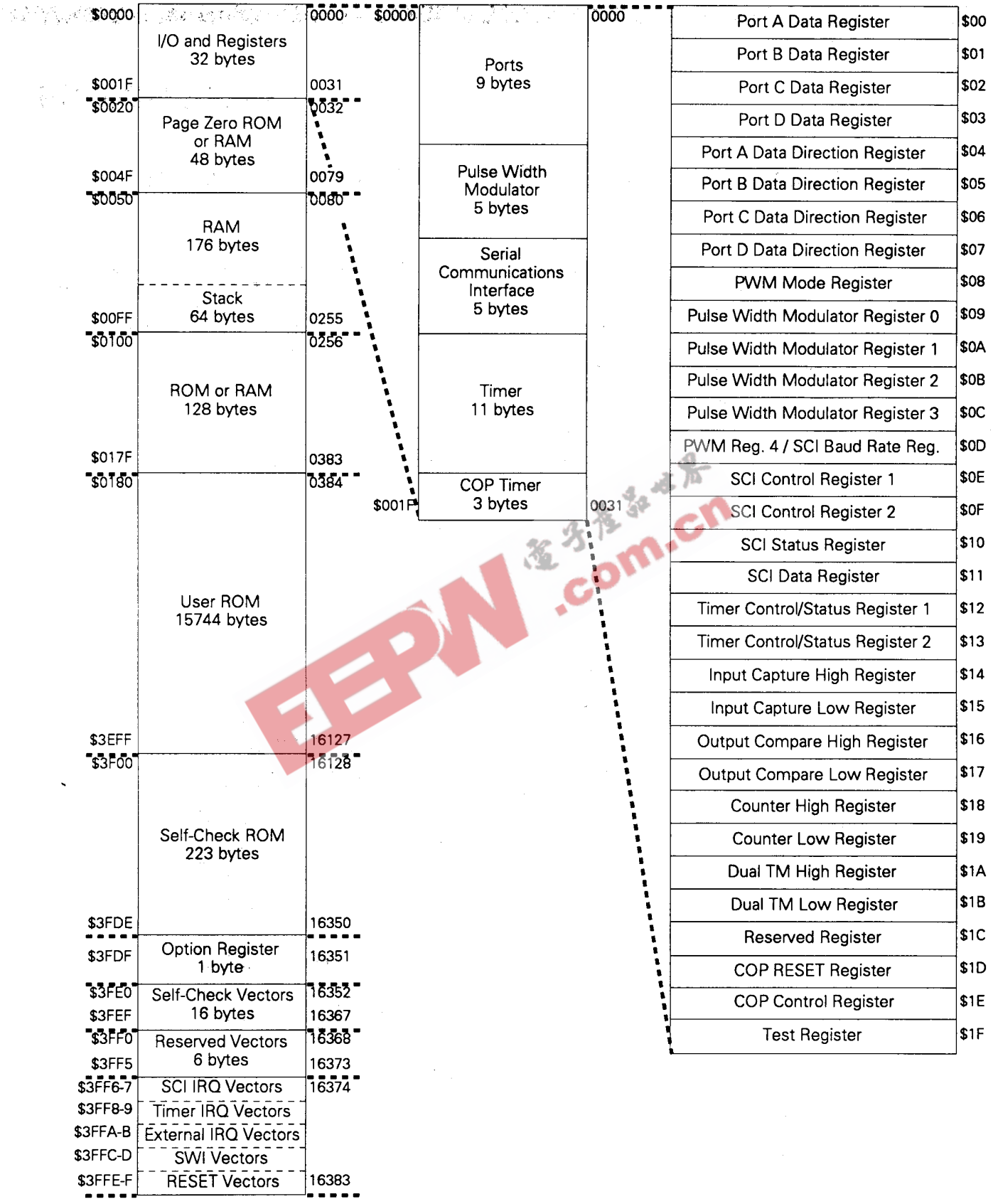

Figure 2. MC68HC05D9 Memory Map

RESETS

The MC68HC05D9 can be reset in four ways: a power-on reset function, an active-low external reset pin, an internal watchdog timer and an internal clock monitor.

RESET pin

The RESET pin is used to provide an orderly software and hardware startup. It also contains an internal Schmitt trigger to improve noise immunity.

Power-on reset (POR)

The Power-on reset occurs when a positive transition is detected on VDD. Power-on reset is strictly for power turn-on and should not be used to detect a drop in the power supply voltage.

Note: There is no internal provision for a power-off reset.

MODES OF OPERATION

The MC68HC05D9 has two modes of operation available to the user: Normal (single chip) mode and Self-check mode.

Single chip mode

The normal operating mode of the device is the single chip mode.

Self check mode

The MC68HC05D9 contains, in mask ROM location $3F00 to $3FDE, a program which checks the integrity of the device with a minimum of support hardware.

This program is executed in the self-check mode, entered when the MCU comes out of reset if the IRQ pin is at 9 volts. Under these circumstances, the self-check vector will be fetched and the self-check firmware will start to execute.

INTERRUPTS

The MC68HC05D9 has 4 different interrupt sources, each with its own vector (three hardware and one software).

If an interrupt enable bit is set to zero it prevents the interrupt from occurring but does not inhibit the associated status flags from being set. RESET clears all interrupt enable bits. When the I-bit in the condition code register (CCR) is set, it blocks all interrupts except the software interrupt (SWI).

Software interrupt

The software interrupt is generated by executing an SWI instuction.

Hardware interrupts

A hardware interrupt can be generated from 3 sources; the external IRQ pin, the SCI interface, or the Timer.

External interrupts are caused by transitions or levels on the IRQ pin.

The SCI can generate an interrupt when various conditions are met thus allowing the serial interface to be interrupt driven.

The Timer can generate an interrupt when one of three conditions is met; overflow, input capture, and output compare. Each of the 3 interrupt sources can be individually enabled.

OPTION REGISTER

The option register contains 3 bits which control the configuration of the memory map and the I-bit which controls the operation of the external interrupt IRQ. The three option bits operate in the following way:

$3FDF	OPTION	RAM0	RAM1	—	—	—	—	IRQEL	—

- IRQEL When set, this bit selects the EDGE and LEVEL interrupt option.

  When clear, the EDGE only option is selected. This bit is not readable and can only be written once after RESET.

  RESET sets this bit.

- RAM1 When set, this bits maps 128 bytes of RAM into the memory map starting at address $100. This makes inaccessible the 128 bytes of ROM that were formerly at these addressess. This bit is readable and writable at all times, allowing the user to switch back and forth between memory types during the course of execution.

  RESET clears this bit.

- RAM0 When set, this bit maps 48 bytes of RAM into page zero starting at address $20. This makes the 48 bytes of page zero ROM inaccessible. This bit is readable and writable at all times, allowing the user to switch back and forth between memory types during the course of execution.

  RESET clears this bit.

SERIAL COMMUNICATIONS INTERFACE

A full-duplex asynchronous Serial Communications Interface (SCI) is provided with a standard NRZ format and a variety of baud rates. The SCI transmitter and receiver are functionally independent, but use the same data format and bit rate. The serial data format is standard mark/space (NRZ) with one start bit, eight or nine data bits and one stop bit. The SCI can be interrupt driven.

COMPUTER OPERATING PROPERLY(COP)

The MC68HC05D9 includes a COP watchdog system to help protect against software failures.

In order to use the COP watchdog timer, the application must be able to execute the special watchdog reset sequence on a regular periodic basis so that the watchdog timer never times out. Although most software disciplines permit the watchdog system concept there is no widely accepted time out period. To keep the MC68HC05D9 compatible with as many different applications as possible, the COP function includes special control bits which allow one of four time out periods to be specified. These control bits also allow the function to be disabled completely.

Clock Monitor

In addition to the COP watchdog system described above, the MC68HC05D9 includes a clock monitor. The clock monitor is enabled/disabled by a software control bit and will generate a reset when the internal clock of the processor is absent for more than a certain period.

TIMER

The 16-bit programmable timer can be used for measuring the pulse width of an input signal while simultaneously generating an output signal. Pulse widths of the input and output signals can vary from several microseconds to many seconds. The timer is also capable of generating periodic interrupts or indicating the passage of an arbitrary number of process cycles.

Because the timer has a 16-bit architecture, each specific functional segment is represented by two registers. These registers contain the 'High' and 'Low' bytes of this functional segment. Generally, accessing the Low byte of a specific timer function allows full control of that function; accessing the High byte will inhibit that capability until the Low byte is accessed.

Note: The I-bit in the condition code register should be set, while manipulating both the High and Low byte register of a specific timer function, to ensure that an interrupt does not occur. A problem could arise if an interrupt were to occur in the time interval between accessing the Low byte and accessing the High byte.

PORTS

Parallel ports

In the single chip mode, there are a total of four I/O ports available. One of the ports, port D, shares its pins with the timer, the PWM and SCI subsystems.

I/O ports

Ports A, B and C are dedicated 8-bit I/O ports. Their I/O pins are individually programmable (under software control) to be either input or output. The direction of the pins of these ports is determined by the associated data direction register (DDR).

When a data direction register bit is set to one, the corresponding I/O pin becomes an output. A read of the pin, configured as an output, returns the last logic level written to that pin. This is necessary for the proper operation of read/modify/write instructions in the presence of heavy electrical loads on the port's output drivers.

At power-on or external reset all DDRs are set to zero which forces all I/O pins to appear as inputs. The DDRs can be written to and read by the processor.

Special port

Port D is an 8-bit I/O port which shares pins with the special subsystem. After Power-on or RESET all bits of port D are configured as standard input, except bit 6 which is a permanent output pin.

When a port D data direction register bit is set to zero, the corresponding bit in the data register port D reflects the level on its associated pin at all times. This means that a port D bit whose pin is shared with the timer, SCI or PWM subsystem can be used to read the state of the pin even when the associated subsystem is enabled.

Note: The operation of the timer or PWM subsystems can cause transitions on the port D pins which are asynchronous with respect to the read cycles on the port D data register. Care should be taken, when writing software, to avoid dependency on the value of any bit of the port D that was read while the operation of one of the associated subsystems may have been causing transitions on that pin.

When a subsystem is enabled, certain pins associated with that subsystem are capable of becoming outputs. These pins then get their drive signal directly from the subsystem rather than from the port D data register. However, these pins remain under the control of the data direction register and can be configured as input pins and read even when driven directly from the subsystem.

The pins of port D are assigned as follows:

- Bit 0 is shared with Receiver Data Input (RDI).

  When the SCI is enabled this pin is the high impedance RDI and the SCI receiver is active.

  When the SCI is disabled the pin acts as a normal port I/O pin.

- Bit 1 is shared with Transmit Data Output (TDO).

  When the SCI is enabled this pin is the TDO.

  When the SCI is disabled the pin acts as a normal port I/O pin.

- Bits 2, 3, 4, 5 and 7 are shared with the PWM0 to PWM4 output signals from the PWM subsystem.

  When the associated bits in the mode register are set to one the pins of port D are outputs driven directly from the PWM subsystem.

  Conversely each one of the five pins can be configured as an I/O pin when the associated bit is set to zero.

- Bit 6 is dedicated to the Timer Output Compare function (TCMP).

  No means is provided for disabling the TCMP function therefore the port D data direction register bit, bit 6, is not provided and writes to this bit have no effect.

  Reads of the port D data register bit, bit 6, return the instantaneous value on the TCMP pin.

PULSE WIDTH MODULATOR (PWM) SUBSYSTEM

The PWM subsystem is a self contained system within the MC68HC05D9 which contains 5 PWM channels of 6 bits which can be used as independent D/A converters.

Each channel has a 6-bit data register which contains the value to be translated into a corresponding pulse width.

The operation of PWM4 has to be selected after RESET by setting the SCIE bit, in the PWM mode register ($08), to zero. This will set the SCI baud rate register, at address $0D, to the data register for PWM4.

ADDRESS		DATA							
		7	6	5	4	3	2	1	0
$08	PWM MODE	0	0	SCIE	PWM4	PWM3	PWM2	PWM1	PWM0
$09	PWM0	0	0						
$0A	PWM1	0	0						
$0B	PWM2	0	0						
$0C	PWM3	0	0						
$0D	PWM4	0	0						

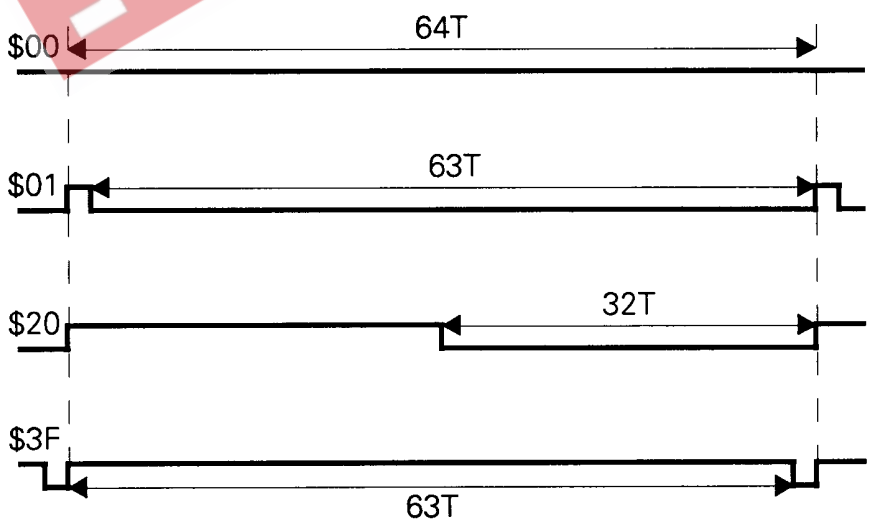

Figure 3. PWM Data Register table and PWM Output Waveform

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	-65 to +150	°C

DC Electrical Characteristics

(V_{DD} = 5Vdc + 10%, V_{SS} = 0Vdc, T_A = 0^0 to 70^0 C)

Characteristic	Symbol	Min	Max	Unit
Output Voltage, $I_{LOAD} \leq 25\ \mu A$	V_{OL}	—	0.1	V
	V_{OH}	V_{DD} – 0.1	—	V
Output High Voltage, I_{LOAD} = 0.8 mA PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{OH}	V_{DD} – 0.8	—	V
Output Low Voltage, I_{LOAD} = 1.6 mA PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	V_{OL}	—	0.4	V
Output Low Voltage, I_{LOAD} = 25 mA PB0-PB7	V_{OL}	—	1.0	V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, TCAP, IRQ, RESET, OSC1	V_{IH}	V_{DD} x 0.7	V_{DD}	V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, TCAP, IRQ, RESET, OSC1	V_{IL}	Vss	V_{DD} x 0.2	V
Maximum total Port B sink current to Vss	I_{SS}	—	200	mA
Data retention mode (0^o - 70^o C)	V_{RM}	2.0	—	V

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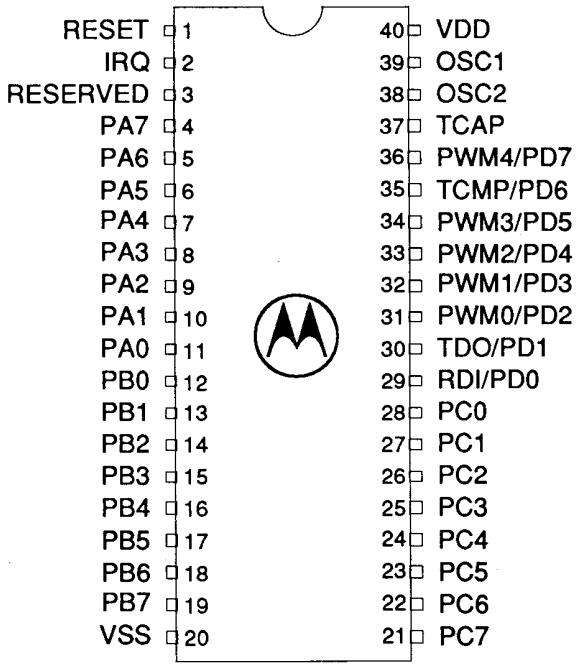
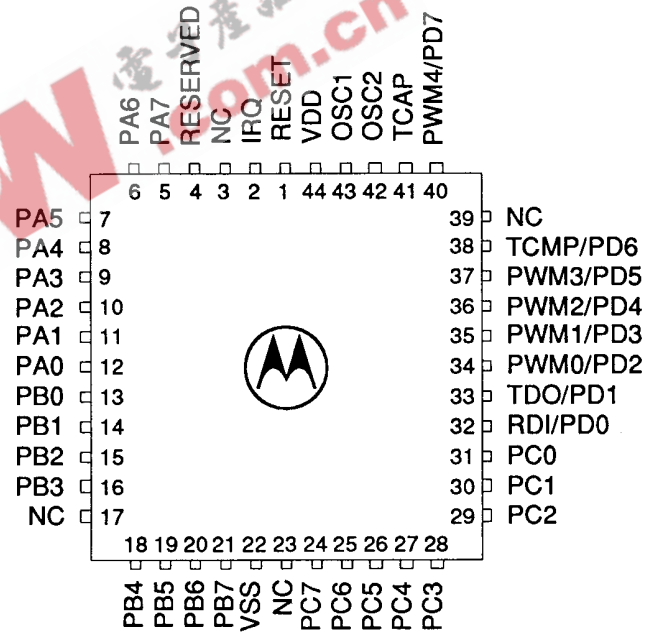


40 pin DIL



44 pin PLCC

Figure 4. Pinouts

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