P4C1256
HIGH SPEED 32K x 8
STATIC CMOS RAM

FEATURES

- **High Speed (Equal Access and Cycle Times)**
  - **— 12/15/20/25/35 ns (Commercial)**
  - **— 15/20/25/35/45 ns (Industrial)**
  - **— 20/25/35/45/55/70 ns (Military)**
- **Low Power**
  - **— 880 mW Active (Commercial)**
- **Single 5V±10% Power Supply**
- **Easy Memory Expansion Using $\overline{CE}$ and $\overline{OE}$ Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Fast t_{OE}**
- **Automatic Power Down**
- **Packages**
  - **—28-Pin 300 mil DIP and SOJ**
  - **—28-Pin 600 mil Ceramic DIP**
  - **—28-Pin LCC(350 mil x 550 mil)**
  - **—32-Pin LCC (450 mil x 550 mil)**

DESCRIPTION

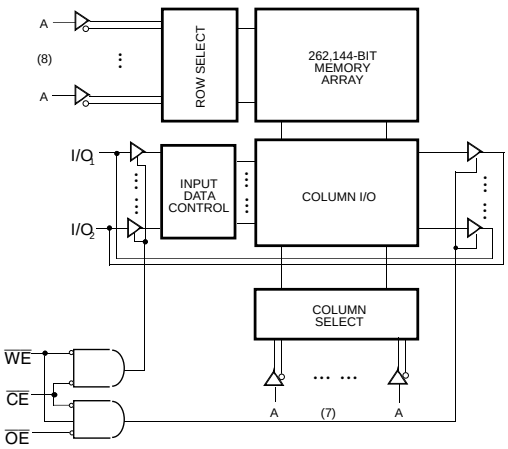
The P4C1256 is a 262,144-bit high-speed CMOS static RAM organized as 32Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

Access times as fast as 12 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1256 is a member of a family of PACE RAM™ products offering fast access times.

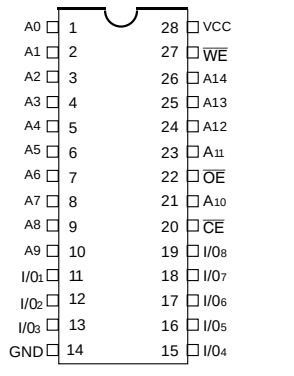
The P4C1256 device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{14}. Reading is accomplished by device selection ($\overline{CE}$ and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or $\overline{WE}$ is LOW.

Package options for the P4C1256 include 28-pin 300 mil DIP and SOJ packages. For military temperature range, Ceramic DIP and LCC packages are available.

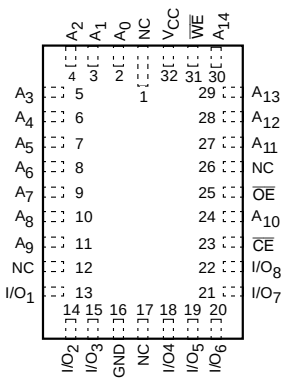
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P5, C5, D5-1), SOJ (J5)
TOP VIEW



32 LCC (L6)
TOP VIEW

See Selection Guide page for 28-pin LCC

MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade(2)	Ambient Temperature	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0V ± 10%
Industrial	–40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

CAPACITANCES[4]

V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions	P4C1256 Min	P4C1256 Max	Unit
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC} –0.2	V_{CC} +0.5	V
V_{LC}	CMOS Input Low Voltage		–0.5[3]	0.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min.		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.	2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max. Mil. V_{IN} = GND to V_{CC} Ind./Com'l.	–10 –5	+10 +5	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, Mil. V_{OUT} = GND to V_{CC} Ind./Com'l.	–10 –5	+10 +5	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$ or Mil. $CE_2 \leq V_{IL}$, V_{CC}= Max Ind./Com'l. f = Max., Outputs Open	—— ——	45 30	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$ or Mil. $CE_2 \leq V_{LC}$, V_{CC}= Max Ind./Com'l. f = 0, Outputs Open $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	—— ——	20 10	mA

n/a = Not Applicable

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	–12	–15	–20	–25	–35	–45	–55	–70	Unit
I_{CC}	Dynamic Operating Current*	Commercial	170	160	155	150	145	N/A	N/A	N/A	mA
		Industrial	N/A	170	165	160	155	150	N/A	N/A	mA
		Military	N/A	N/A	170	165	160	155	150	150	mA

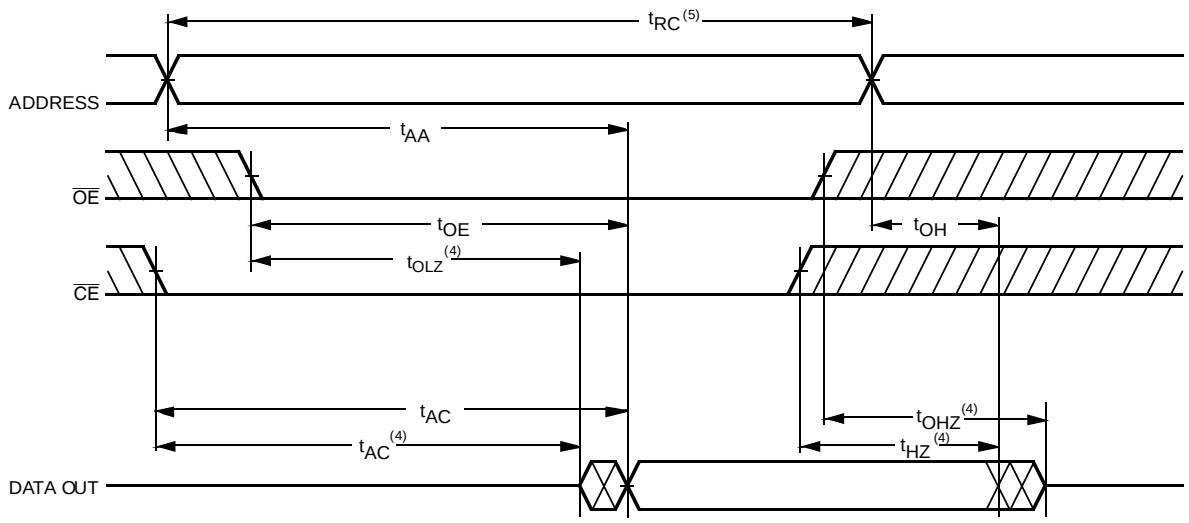
*V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

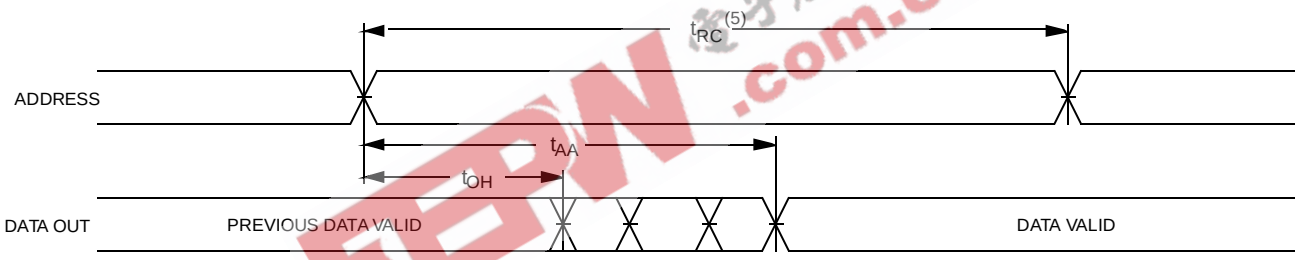
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		35		45		55		70		ns
t_{AA}	Address Access Time		12		15		20		25		35		45		55		70	ns
t_{AC}	Chip Enable Access Time		12		15		20		25		35		45		55		70	ns
t_{OH}	Output Hold from Address Change	2		2		2		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		3		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		5		8		9		11		15		20		25		30	ns
t_{OE}	Output Enable Low to Data Valid		5		7		9		10		15		20		25		30	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		5		7		9		11		15		20		25		30	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		15		20		20		20		25		30		35	ns

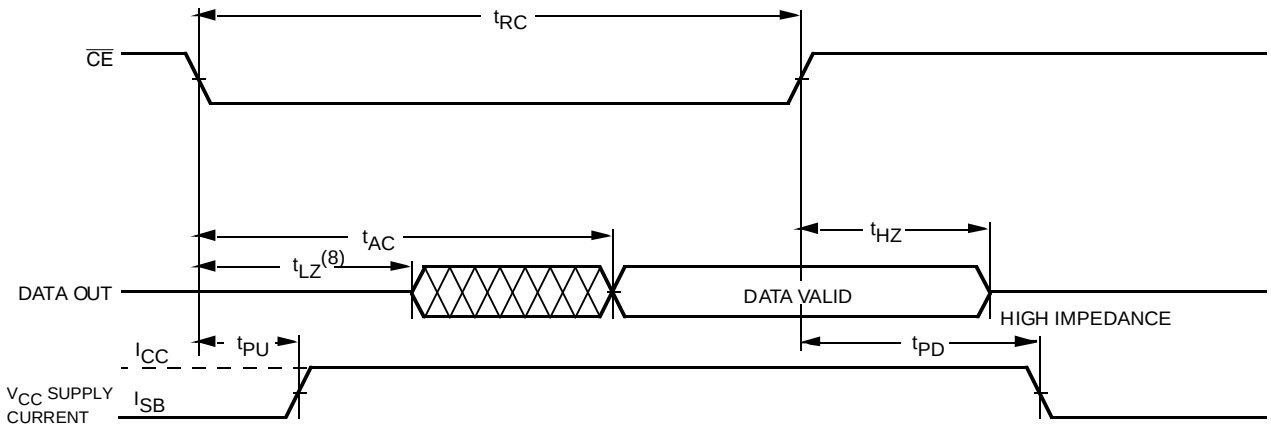
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[1]



READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)



Notes:

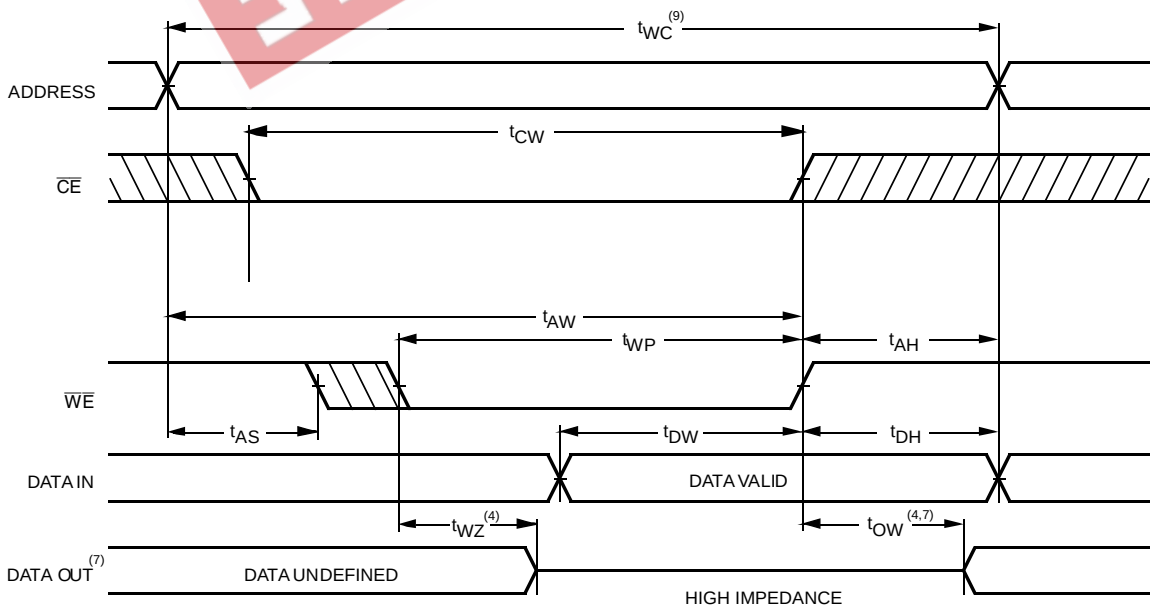
1. $\overline{WE}$ is HIGH for READ cycle.
2. $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
3. ADDRESS must be valid prior to, or coincident with $\overline{CE}_1$ transition LOW .
4. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		15		20		25		35		45		55		70		ns
t_{CW}	Chip Enable Time to End of Write	9		10		15		18		22		30		35		40		ns
t_{AW}	Address Valid to End of Write	9		10		15		20		25		35		40		45		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	9		11		15		18		22		25		30		35		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	8		9		11		13		15		20		25		30		ns
t_{DH}	Date Hold Time	0		0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		7		8		10		11		15		18		25		30	ns
t_{OW}	Output Active from End of Write	3		3		3		3		5		5		0		0		ns

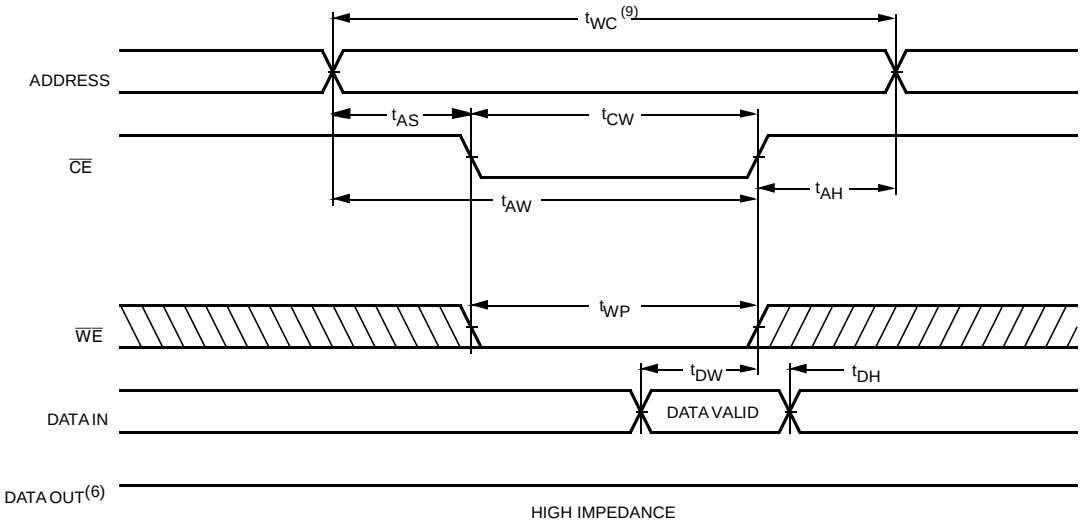
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[6]



Notes:

6. $\overline{CE}_1$ and $\overline{WE}$ must be LOW for WRITE cycle.
7. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
8. If $\overline{CE}_1$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
9. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[6]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

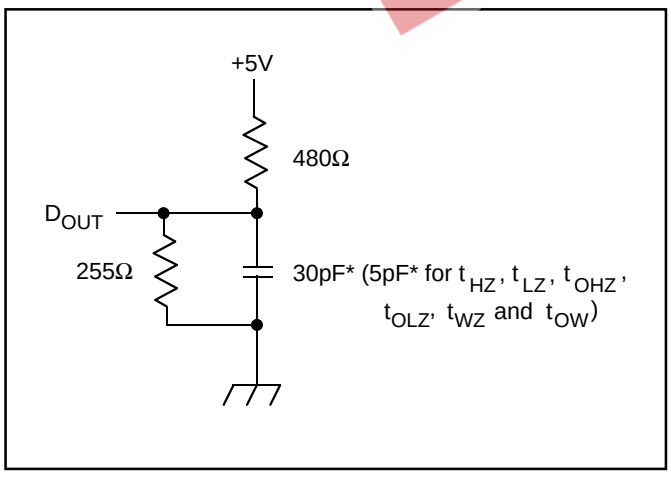


Figure 1. Output Load

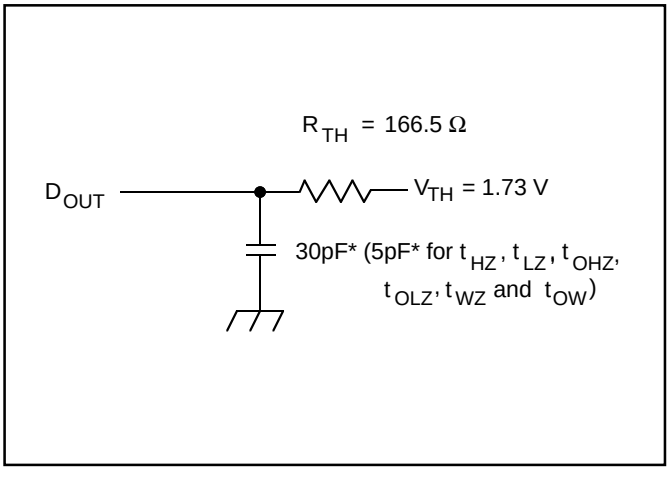


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C1256, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

PACKAGE SUFFIX

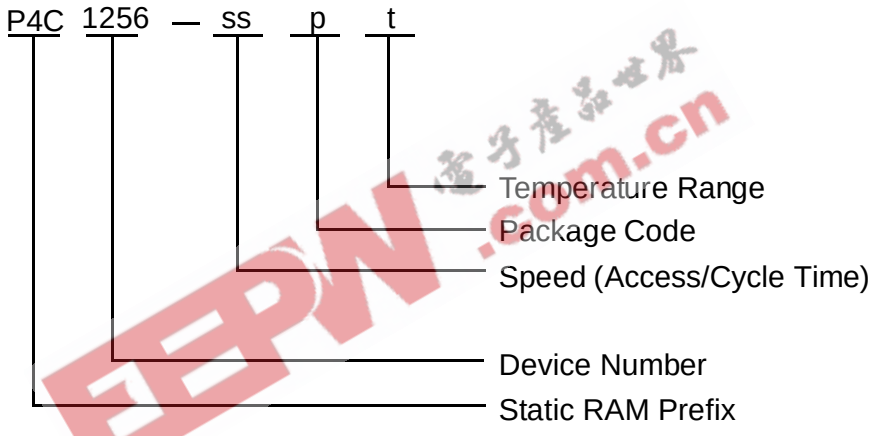
Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide
D	CERDIP, 300 mil wide
DW	CERDIP, 600 mil wide
L28	Leadless Chip Carrier, 350 x 550 mils
L32	Leadless Chip Carrier, 450 x 550 mils

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
I	Industrial Temperature Range, –40˚C to +85˚C.
M	Military Temperature Range, –55°C to +125°C.
MB	Mil. Temp. with MIL-STD-883 Class B compliance.

ORDERING INFORMATION

Performance Semiconductor's part numbering scheme is as follows:



I = Ultra-low standby power designator L, if available.
ss = Speed (access/cycle time in ns). e.g. 25, 35.
p = Package code, i.e., P, J, C, D, DW, L28, L32.
t = Temperature range, i.e., C, M. MB.

The P4C1256 is also available per SMD 5962-88662

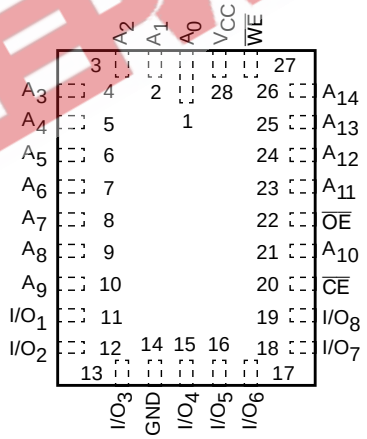
SELECTION GUIDE

The P4C1256 is available in the following temperature, speed and package options. The P4C1256L is available only over the military temperature range.

Temp. Range	Package \ Speed	12	15	20	25	35	45	55	70
Com'l	Plastic DIP	-12PC	-15PC	-20PC	-25PC	-35PC	N/A	N/A	N/A
	Plastic SOJ	-12JC	-15JC	-20JC	-25JC	-35JC	N/A	N/A	N/A
Ind.	Plastic DIP	N/A	-15PI	-20PI	-25PI	-35PI	-45PI	N/A	N/A
	Plastic SOJ	N/A	-15JI	-20JI	-25JI	-35JI	-425JI	N/A	N/A
Mil. Temp.	Sidebrazed (300 mil)	N/A	N/A	-20CM	-25CM	-35CM	-45CM	-55CM	-70CM
	CERDIP (300 mil)	N/A	N/A	-20DM	-25DM	-35DM	-45DM	-55DM	-70DM
	CERDIP (600 mil)	N/A	N/A	-20DWM	-25DWM	-35DWM	-45DWM	-55DWM	-70DWM
	L28	N/A	N/A	-20L28M	-25L28M	-35L28M	-45L28M	-55L28M	-70L28M
	L32	N/A	N/A	-20L32M	-25L32M	-35L32M	-45L32M	-55L32M	-70L32M
Military Proc'd*	Sidebrazed (300 mil)	N/A	N/A	-20CMB	-25CMB	-35CMB	-45CMB	-55CMB	-70CMB
	CERDIP (300 mil)	N/A	N/A	-20DMB	-25DMB	-35DMB	-45DMB	-55DMB	-70DMB
	CERDIP (600 mil)	N/A	N/A	-20DWMB	-25DWMB	-35DWMB	-45DWMB	-55DWMB	-70DWMB
	L28	N/A	N/A	-20L28MB	-25L28MB	-35L28MB	-45L28MB	-55L28MB	-70L28MB
	L32	N/A	N/A	-20L32MB	-25L32MB	-35L32MB	-45L32MB	-55L32MB	-70L32MB

* Military temperature range with MIL-STD-883, Class B processing.
N/A = Not Available

28 LCC PIN CONFIGURATION



28 LCC (L5)
TOP VIEW