

P4C164

ULTRA HIGH SPEED 8K x 8

STATIC CMOS RAMS



FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 8/10/12/15/20/25/35/70/100 ns (Commercial)
 - 10/12/15/20/25/35/70/100 ns (Industrial)
 - 12/15/20/25/35/45/70/100 ns (Military)
- Low Power Operation
- Output Enable and Dual Chip Enable Control Functions
- Single 5V±10% Power Supply
- Data Retention with 2.0V Supply, 10 µA Typical Current (P4C164L Military)
- Common Data I/O
- Fully TTL Compatible Inputs and Outputs
- Standard Pinout (JEDEC Approved)
 - 28-Pin 300 mil Plastic DIP, SOJ
 - 28-Pin 600 mil Plastic DIP (70 & 100ns)
 - 28-Pin 300 mil SOP (70 & 100ns)
 - 28-Pin 300 mil Ceramic DIP
 - 28-Pin 600 mil Ceramic DIP
 - 28-Pin 350 x 550 mil LCC
 - 32-Pin 450 x 550 mil LCC
 - 28-Pin CERPACK



DESCRIPTION

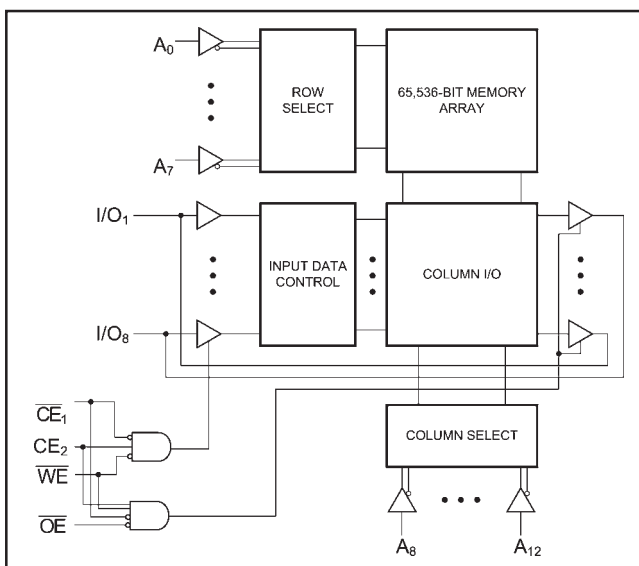
The P4C164 is a 65,536-bit ultra high-speed static RAM organized as 8K x 8. The CMOS memory requires no clocks or refreshing and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply. With battery backup, data integrity is maintained with supply voltages down to 2.0V. Current drain is typically 10 µA from a 2.0V supply.

Access times as fast as 8 nanoseconds are available, permitting greatly enhanced system operating speeds.

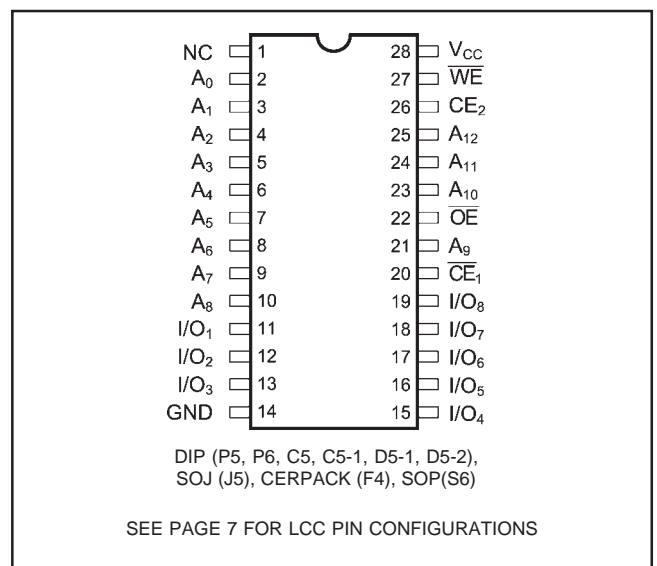
The P4C164 is available in 28-pin 300 mil DIP and SOJ, 28-pin 600 mil plastic and ceramic DIP, 28-pin 350 x 550 mil LCC, 32-pin 450 x 550 mil LCC, and 28-pin CERPACK. The 70ns and 100ns P4C164s are available in the 600 mil plastic DIP.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------------|------|
| V _{CC} | Power Supply Pin with Respect to GND | -0.5 to +7 | V |
| V _{TERM} | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 to V _{CC} +0.5 | V |
| T _A | Operating Temperature | -55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|-------------------|------------------------|-------------|------|
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | mA |

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade ⁽²⁾ | Ambient Temperature | GND | V _{CC} |
|----------------------|---------------------|-----|-----------------|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

CAPACITANCES⁽⁴⁾

V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz

| Symbol | Parameter | Conditions | Typ. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | pF |

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

| Symbol | Parameter | Test Conditions | P4C164 | | P4C164L | | Unit |
|------------------|--|---|----------------------|----------------------|----------------------|----------------------|------|
| | | | Min | Max | Min | Max | |
| V _{IH} | Input High Voltage | | 2.2 | V _{CC} +0.5 | 2.2 | V _{CC} +0.5 | V |
| V _{IL} | Input Low Voltage | | -0.5 ⁽³⁾ | 0.8 | -0.5 ⁽³⁾ | 0.8 | V |
| V _{HC} | CMOS Input High Voltage | | V _{CC} -0.2 | V _{CC} +0.5 | V _{CC} -0.2 | V _{CC} +0.5 | V |
| V _{LC} | CMOS Input Low Voltage | | -0.5 ⁽³⁾ | 0.2 | -0.5 ⁽³⁾ | 0.2 | V |
| V _{CD} | Input Clamp Diode Voltage | V _{CC} = Min., I _{IN} = -18 mA | | -1.2 | | -1.2 | V |
| V _{OL} | Output Low Voltage (TTL Load) | I _{OL} = +8 mA, V _{CC} = Min. | | 0.4 | | 0.4 | V |
| V _{OH} | Output High Voltage (TTL Load) | I _{OH} = -4 mA, V _{CC} = Min. | 2.4 | | 2.4 | | V |
| I _{IU} | Input Leakage Current | V _{CC} = Max. Mil. V _{IN} = GND to V _{CC} Ind./Com'l. | -10 -5 | +10 +5 | -5 n/a | +5 n/a | µA |
| I _{LO} | Output Leakage Current | V _{CC} = Max., $\overline{CE} = V_{IH}$, Mil. V _{OUT} = GND to V _{CC} Ind./Com'l. | -10 -5 | +10 +5 | -5 n/a | +5 n/a | µA |
| I _{SB} | Standby Power Supply Current (TTL Input Levels) | $\overline{CE}_1 \geq V_{IH}$ or Mil. $\overline{CE}_2 \leq V_{IL}$, Ind./Com'l. V _{CC} = Max, f = Max., Outputs Open | — — | 40 30 | — — | 40 n/a | mA |
| I _{SB1} | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE}_1 \geq V_{HC}$ or Mil. $\overline{CE}_2 \leq V_{LC}$, Ind./Com'l. V _{CC} = Max, f = 0, Outputs Open V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC} | — — | 25 15 | — — | 1 n/a | mA |

Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | -8 | -10 | -12 | -15 | -20 | -25 | -35 | 45 | -70 | -100 | Unit |
|-----------------|----------------------------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|
| I _{CC} | Dynamic Operating Current* | Commercial | 200 | 180 | 170 | 160 | 155 | 150 | 145 | N/A | 130 | 125 | mA |
| | | Industrial | N/A | 190 | 180 | 170 | 160 | 155 | 150 | N/A | 145 | 140 | mA |
| | | Military | N/A | N/A | 180 | 170 | 160 | 155 | 150 | 145 | 145 | 145 | mA |

*V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}_1 = V_{IL}$, CE₂ = V_{IH}, $\overline{OE} = V_{IH}$

DATA RETENTION CHARACTERISTICS (P4C164L, Military Temperature Only)

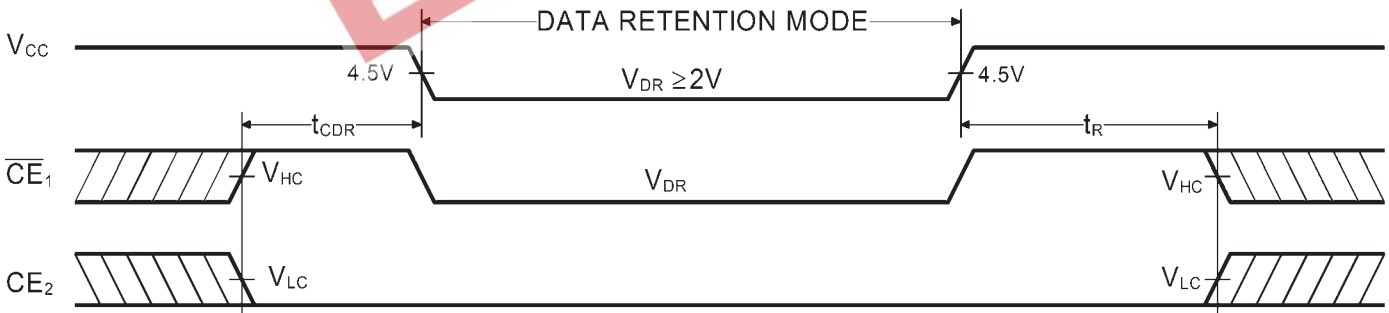
| Symbol | Parameter | Test Condition | Min | Typ.* | | Max | | Unit |
|-----------------------------|--------------------------------------|--|------------------------------|------------------------|------------------------|------------------------|------------------------|------|
| | | | | V _{CC} = 2.0V | V _{CC} = 3.0V | V _{CC} = 2.0V | V _{CC} = 3.0V | |
| V _{DR} | V _{CC} for Data Retention | | 2.0 | | | | | V |
| I _{CCDR} | Data Retention Current | $\overline{CE}_1 \geq V_{CC} - 0.2V$ or | | 10 | 15 | 200 | 300 | μA |
| t _{CDR} | Chip Deselect to Data Retention Time | CE ₂ ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V | 0 | | | | | ns |
| t _R [†] | Operation Recovery Time | or V _{IN} ≤ 0.2V | t _{RC} [§] | | | | | ns |

*T_A = +25°C

§t_{RC} = Read Cycle Time

†This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM

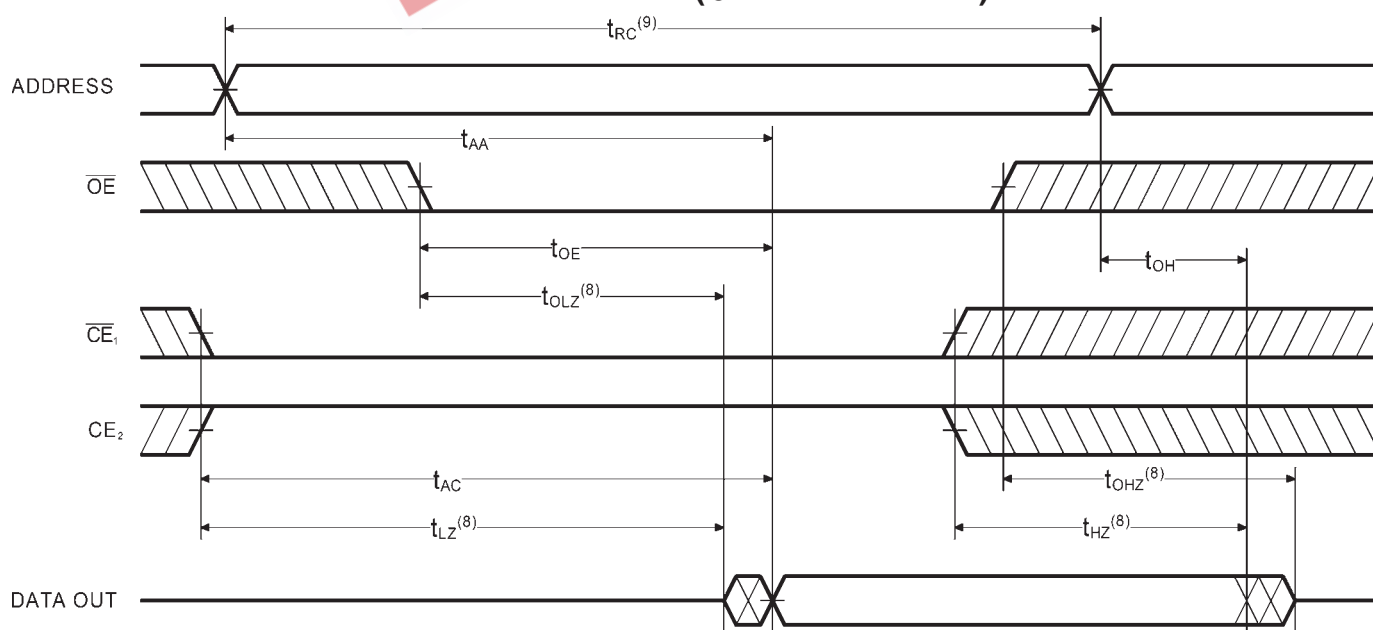


AC ELECTRICAL CHARACTERISTICS—READ CYCLE

($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

| Symbol | Parameter | -8 | | -10 | | -12 | | -15 | | -20 | | -25 | | -35 | | -45 | | -70 | | -100 | | Unit |
|-----------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{RC} | Read Cycle Time | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 70 | | 100 | | ns |
| t_{AA} | Address Access Time | | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 70 | | 100 | ns |
| t_{AC} | Chip Enable Access Time | | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 70 | | 100 | ns |
| t_{OH} | Output Hold from Address Change | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t_{LZ} | Chip Enable to Output in Low Z | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| t_{HZ} | Chip Disable to Output in High Z | | 5 | | 6 | | 7 | | 8 | | 8 | | 10 | | 15 | | 20 | | 35 | | 45 | ns |
| t_{OE} | Output Enable Low to Data Valid | | 5 | | 6 | | 7 | | 9 | | 10 | | 13 | | 18 | | 20 | | 35 | | 45 | ns |
| t_{OLZ} | Output Enable Low to Low Z | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| t_{OHZ} | Output Enable High to High Z | | 5 | | 6 | | 7 | | 9 | | 9 | | 12 | | 15 | | 20 | | 35 | | 45 | ns |
| t_{PU} | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{PD} | Chip Disable to Power Down Time | | 8 | | 10 | | 12 | | 15 | | 20 | | 20 | | 20 | | 25 | | 35 | | 45 | ns |

TIMING WAVEFORM OF READ CYCLE NO. 1 (\overline{OE} CONTROLLED)⁽⁵⁾

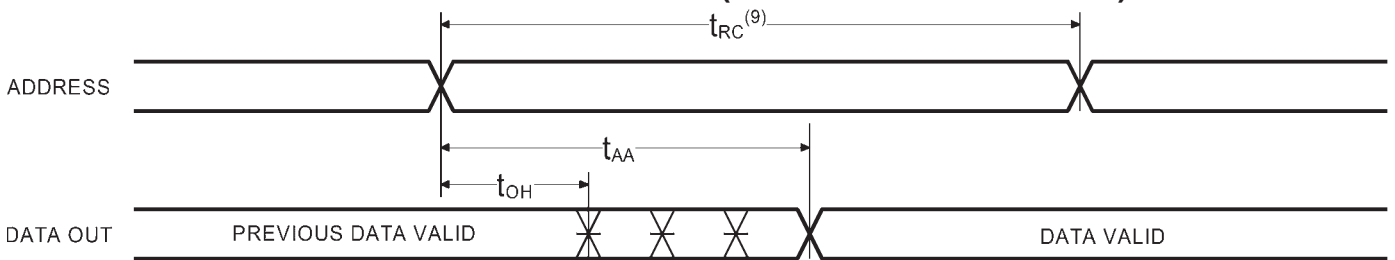


Notes:

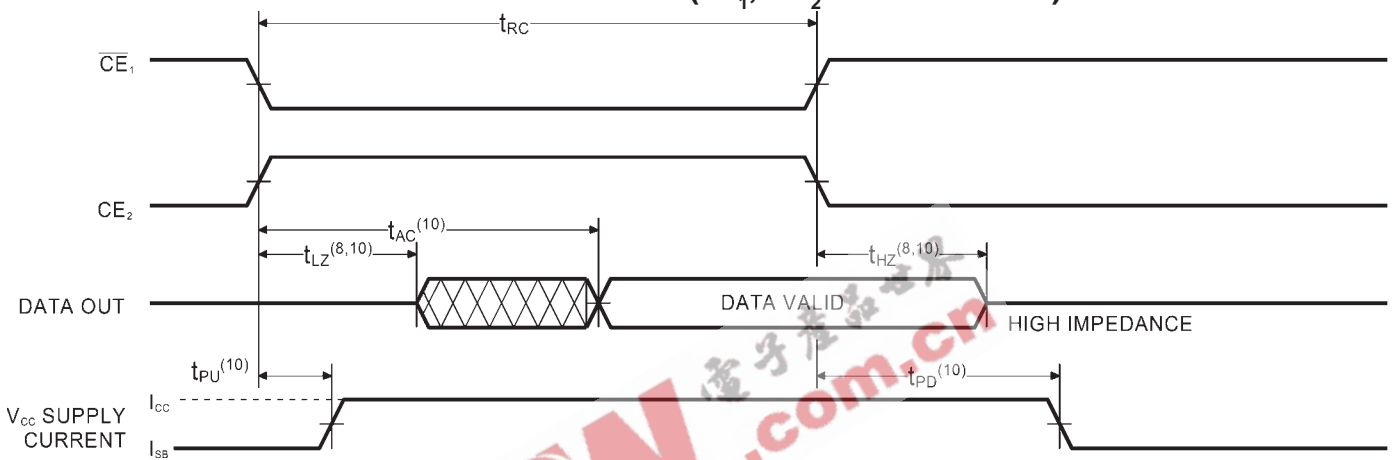
- 5. \overline{WE} is HIGH for READ cycle.
- 6. \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{OE} is LOW for READ cycle.
- 7. ADDRESS must be valid prior to, or coincident with \overline{CE}_1 transition LOW and \overline{CE}_2 transition HIGH.

- 8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)^(5,6)



TIMING WAVEFORM OF READ CYCLE NO. 3 (\overline{CE}_1 , CE_2 CONTROLLED)^(5,7,10)



Notes:

9. READ Cycle Time is measured from the last valid address to the first transitioning address.

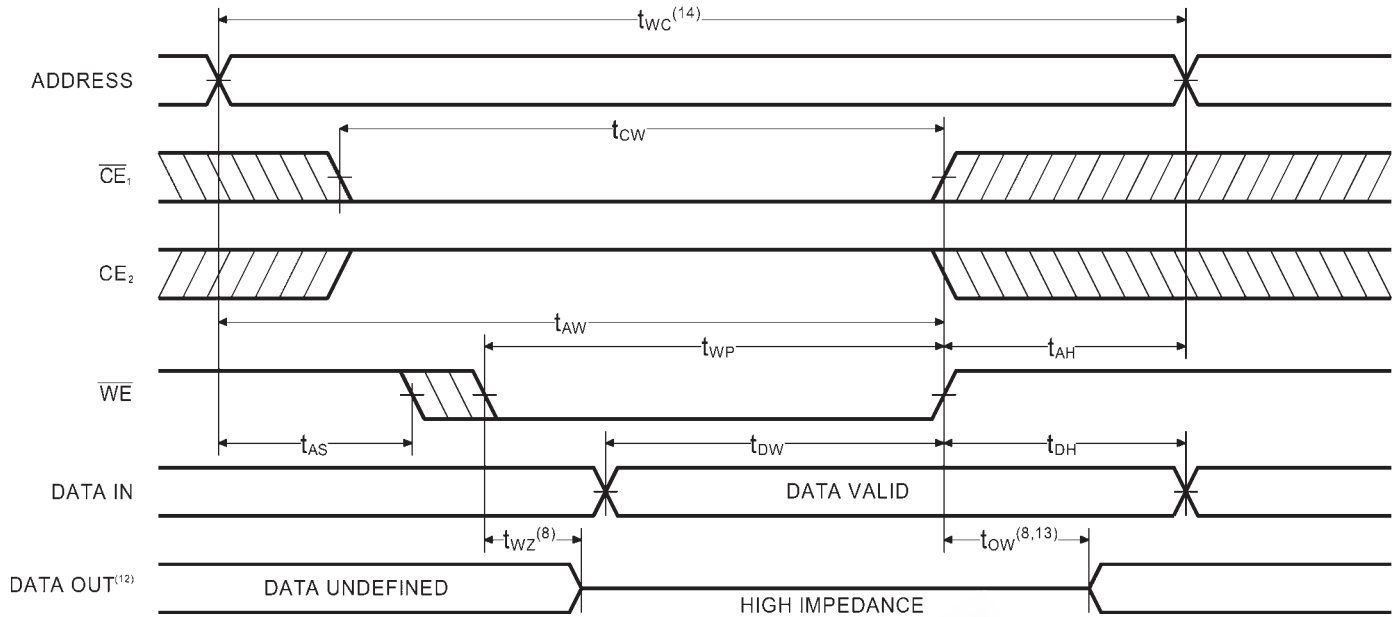
10. Transitions caused by a chip enable control have similar delays irrespective of whether \overline{CE}_1 or CE_2 causes them.

AC CHARACTERISTICS—WRITE CYCLE

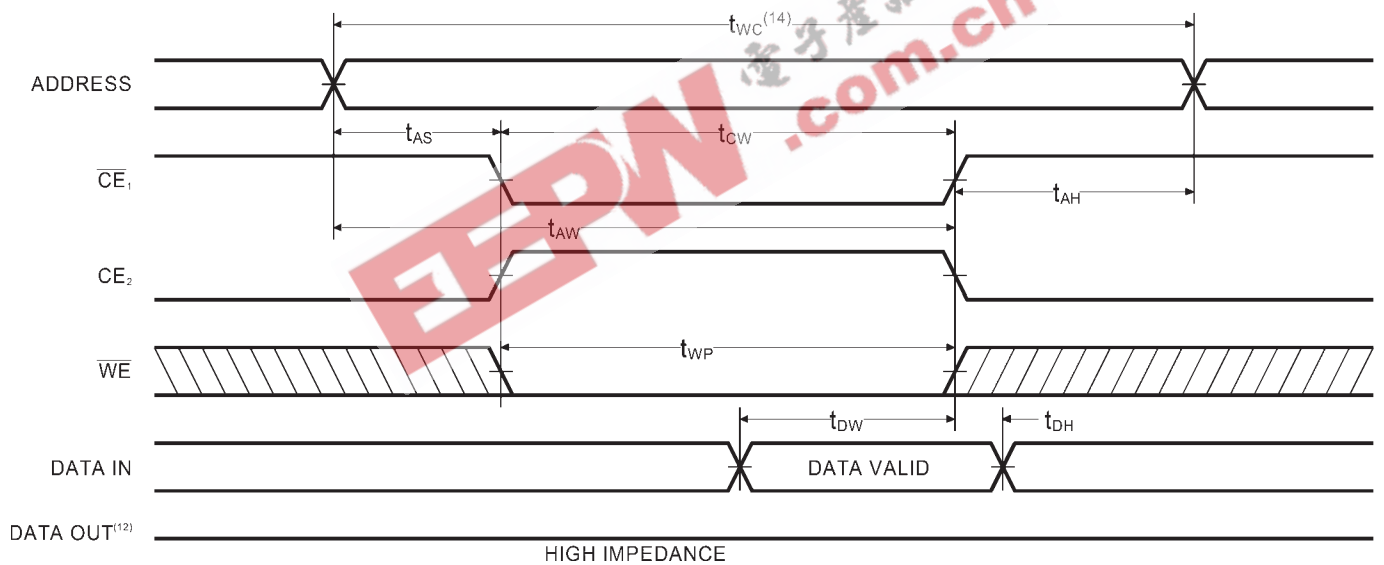
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

| Symbol | Parameter | -8 | | -10 | | -12 | | -15 | | -20 | | -25 | | -35 | | -45 | | -70 | | -100 | | Unit |
|----------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{WC} | Write Cycle Time | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 70 | | 100 | | ns |
| t_{CW} | Chip Enable Time to End of Write | 6 | | 7 | | 8 | | 12 | | 15 | | 18 | | 25 | | 33 | | 50 | | 70 | | ns |
| t_{AW} | Address Valid to End of Write | 7 | | 8 | | 10 | | 12 | | 15 | | 18 | | 25 | | 33 | | 50 | | 70 | | ns |
| t_{AS} | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WP} | Write Pulse Width | 7 | | 8 | | 9 | | 12 | | 15 | | 18 | | 20 | | 25 | | 40 | | 50 | | ns |
| t_{AH} | Address Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{DW} | Data Valid to End of Write | 6 | | 7 | | 8 | | 9 | | 11 | | 13 | | 15 | | 20 | | 30 | | 40 | | ns |
| t_{DH} | Date Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WZ} | Write Enable to Output in High Z | | 6 | | 7 | | 7 | | 7 | | 8 | | 10 | | 14 | | 18 | | 30 | | 40 | ns |
| t_{OW} | Output Active from End of Write | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)⁽¹¹⁾



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED)⁽¹¹⁾



Notes:

- 11. \overline{CE}_1 and \overline{WE} must be LOW, and CE_2 HIGH for WRITE cycle.
- 12. \overline{OE} is LOW for this WRITE cycle to show t_{WZ} and t_{OW} .
- 13. If \overline{CE}_1 goes HIGH, or CE_2 goes LOW, simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.

- 14. Write Cycle Time is measured from the last valid address to the first transitioning address.

AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

TRUTH TABLE

| Mode | \overline{CE}_1 | CE_2 | \overline{OE} | \overline{WE} | I/O | Power |
|--------------------|-------------------|--------|-----------------|-----------------|-----------|---------|
| Standby | H | X | X | X | High Z | Standby |
| Standby | X | L | X | X | High Z | Standby |
| D_{OUT} Disabled | L | H | H | H | High Z | Active |
| Read | L | H | L | H | D_{OUT} | Active |
| Write | L | H | X | L | High Z | Active |

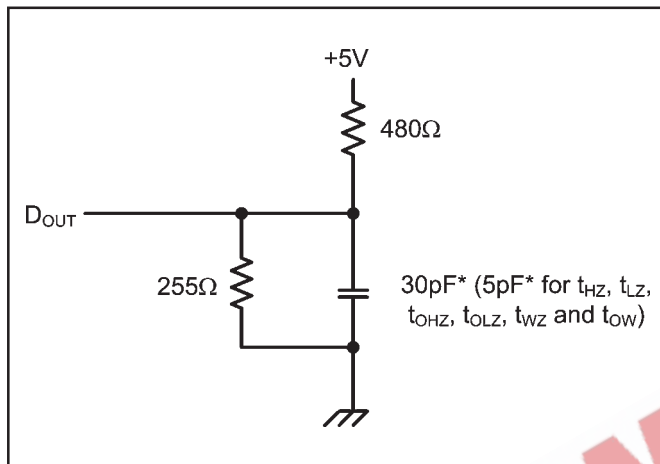


Figure 1. Output Load

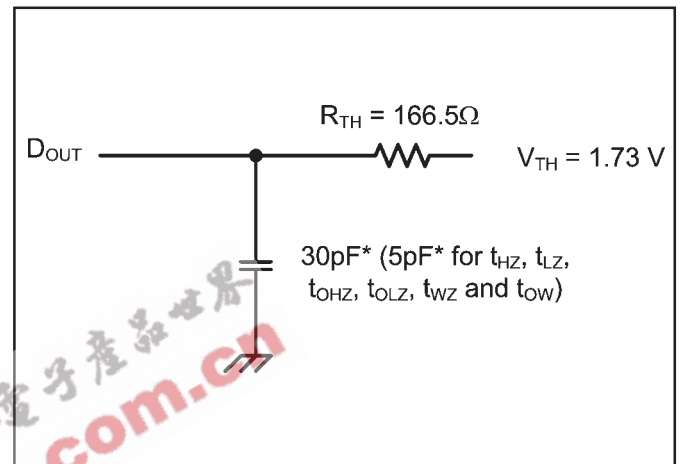


Figure 2. Thevenin Equivalent

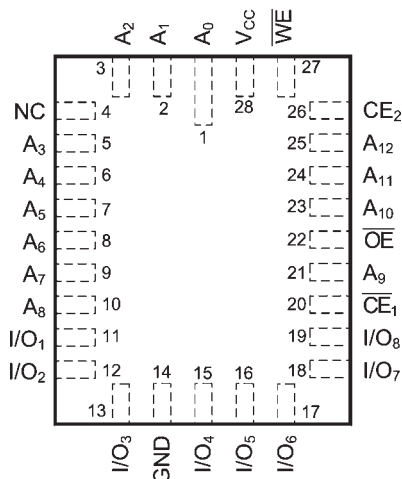
* including scope and test fixture.

Note:

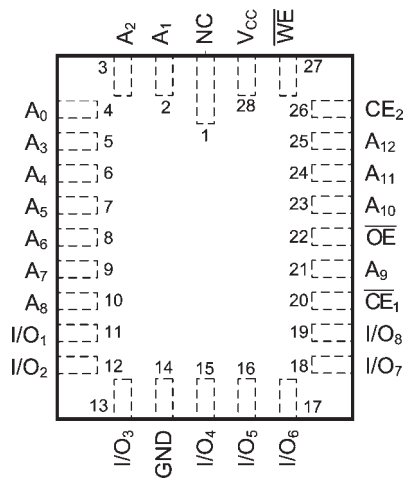
Because of the high speed of the P4C164/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections,

proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116 Ω resistor must be used in series with D_{OUT} to match 166 Ω (Thevenin Resistance).

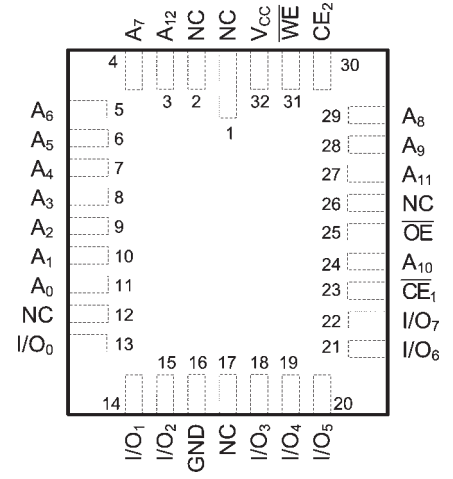
LCC PIN CONFIGURATIONS



LCC (L5)
"L" - STANDARD PIN-OUT

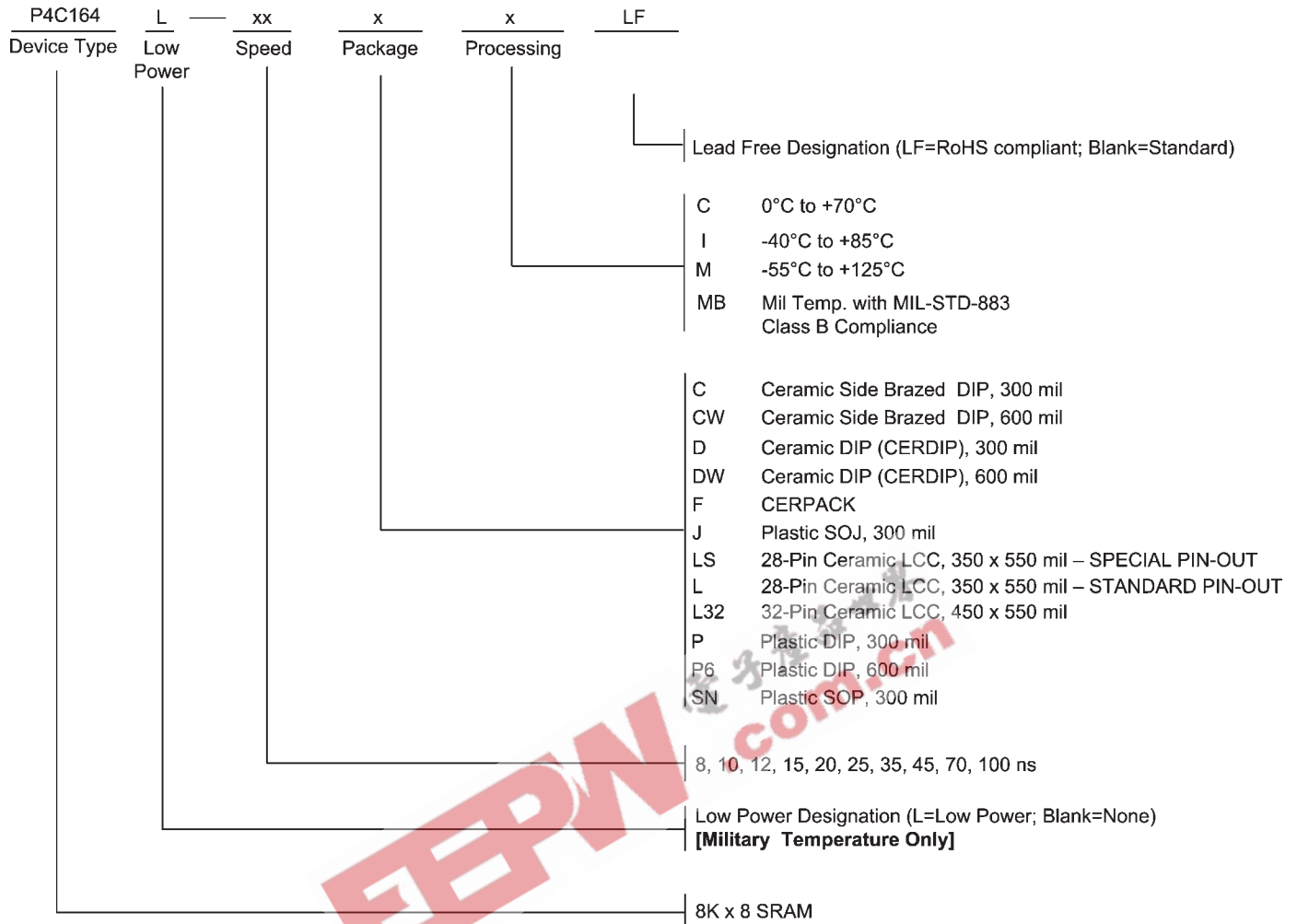


LCC (L5)
"LS" - SPECIAL PIN-OUT



LCC (L6)

ORDERING INFORMATION



SELECTION GUIDE

The P4C164 is available in the following temperature, speed and package options. The P4C164L is available only over the military temperature range.

| Temperature Range | Package | Speed (ns) | | | | | | | | | |
|-------------------|-----------------------|------------|-------|-------|-------|-------|-------|-------|-----|--------|---------|
| | | 8 | 10 | 12 | 15 | 20 | 25 | 35 | 45 | 70 | 100 |
| Commercial | Plastic DIP (300 mil) | -8PC | -10PC | -12PC | -15PC | -20PC | -25PC | -35PC | N/A | N/A | N/A |
| | Plastic DIP (600 mil) | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | -70P6C | -100P6C |
| | Plastic SOJ | -8JC | -10JC | -12JC | -15JC | -20JC | -25JC | -35JC | N/A | N/A | N/A |
| | Plastic SOP | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | -70SNC | -100SNC |
| Industrial | Plastic DIP (300 mil) | N/A | -10PI | -12PI | -15PI | -20PI | -25PI | -35PI | N/A | N/A | N/A |
| | Plastic DIP (600 mil) | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | -70P6I | -100P6I |
| | Plastic SOJ | N/A | -10JI | -12JI | -15JI | -20JI | -25JI | -35JI | N/A | N/A | N/A |
| | Plastic SOP | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | -70SNI | -100SNI |

N/A = Not available

SELECTION GUIDE (continued)

| Temperature Range | Package | Speed (ns) | | | | | | | | | |
|----------------------|------------------|------------|-----|----------|----------|----------|----------|----------|----------|----------|-----------|
| | | 8 | 10 | 12 | 15 | 20 | 25 | 35 | 45 | 70 | 100 |
| Military Temperature | Side Brazed DIP | N/A | N/A | -12CM | -15CM | -20CM | -25CM | -35CM | -45CM | -70CM | -100CM |
| | CERDIP (300 mil) | N/A | N/A | -12DM | -15DM | -20DM | -25DM | -35DM | -45DM | -70DM | -100DM |
| | CERDIP (600 mil) | N/A | N/A | -12DWM | -15DWM | -20DWM | -25DWM | -35DWM | -45DWM | -70DWM | -100DWM |
| | CERPACK | N/A | N/A | -12FM | -15FM | -20FM | -25FM | -35FM | -45FM | -70FM | -100FM |
| | 28-Pin LCC | N/A | N/A | -12LM | -15LM | -20LM | -25LM | -35LM | -45LM | -70LM | -100LM |
| | 28-Pin LCC ** | N/A | N/A | -12LSM | -15LSM | -20LSM | -25LSM | -35LSM | -45LSM | -70LSM | -100LSM |
| | 32-Pin LCC | N/A | N/A | -12L32M | -15L32M | -20L32M | -25L32M | -35L32M | -45L32M | -70L32M | -100L32M |
| Military Processed * | Side Brazed DIP | N/A | N/A | -12CMB | -15CMB | -20CMB | -25CMB | -35CMB | -45CMB | -70CMB | -100CMB |
| | CERDIP (300 mil) | N/A | N/A | -12DMB | -15DMB | -20DMB | -25DMB | -35DMB | -45DMB | -70DMB | -100DMB |
| | CERDIP (600 mil) | N/A | N/A | -12DWMB | -15DWMB | -20DWMB | -25DWMB | -35DWMB | -45DWMB | -70DWMB | -100DWMB |
| | CERPACK | N/A | N/A | -12FMB | -15FMB | -20FMB | -25FMB | -35FMB | -45FMB | -70FMB | -100FMB |
| | 28-Pin LCC | N/A | N/A | -12LMB | -15LMB | -20LMB | -25LMB | -35LMB | -45LMB | -70LMB | -100LMB |
| | 28-Pin LCC ** | N/A | N/A | -12LSMB | -15LSMB | -20LSMB | -25LSMB | -35LSMB | -45LSMB | -70LSMB | -100LSMB |
| | 32-Pin LCC | N/A | N/A | -12L32MB | -15L32MB | -20L32MB | -25L32MB | -35L32MB | -45L32MB | -70L32MB | -100L32MB |

* Military temperature range with MIL-STD-883, Class B processing.

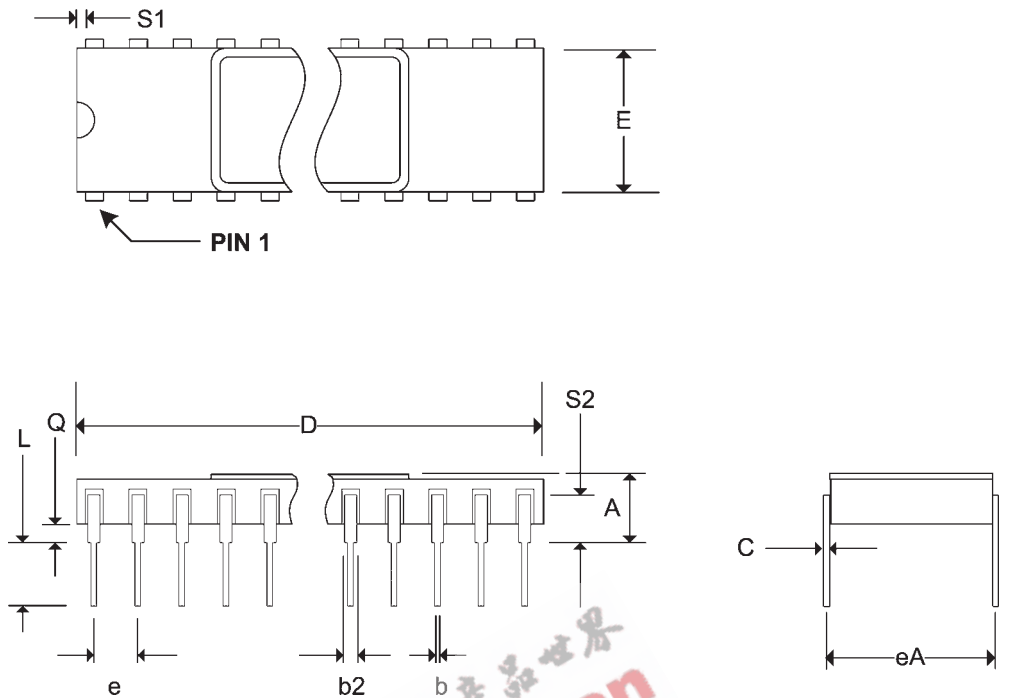
**SPECIAL PINOUT

N/A = Not available

EEPW.com.cn 电子产品世界

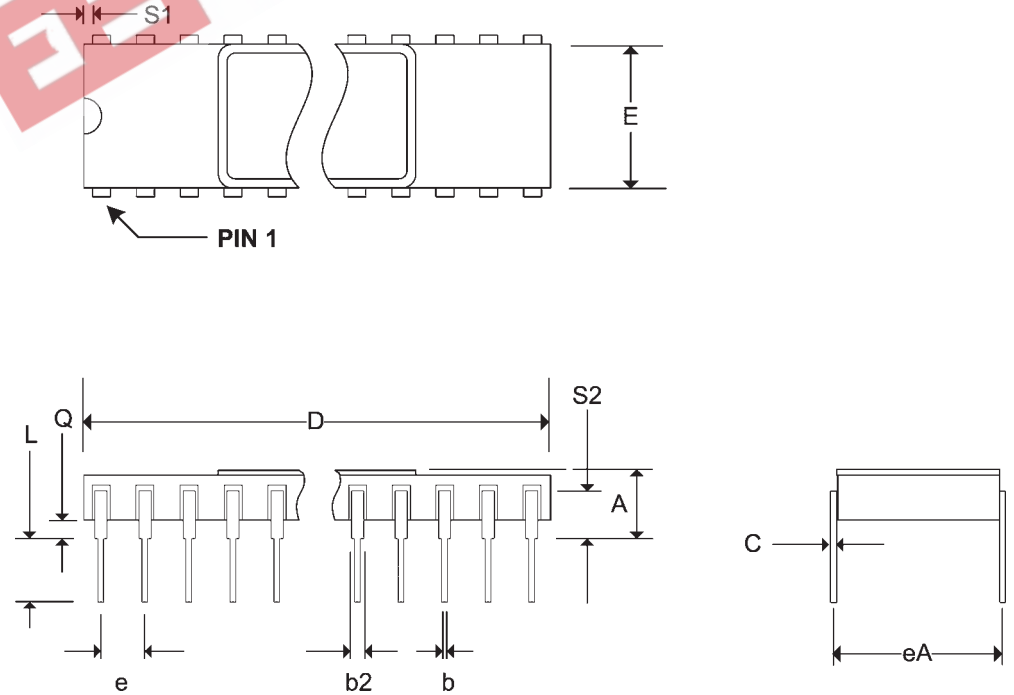
| | | |
|--------|--------------|------------|
| Pkg # | C5 | |
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.225 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.485 |
| E | 0.240 | 0.310 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.070 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

SIDE BRAZED DUAL IN-LINE PACKAGE (300 mils)



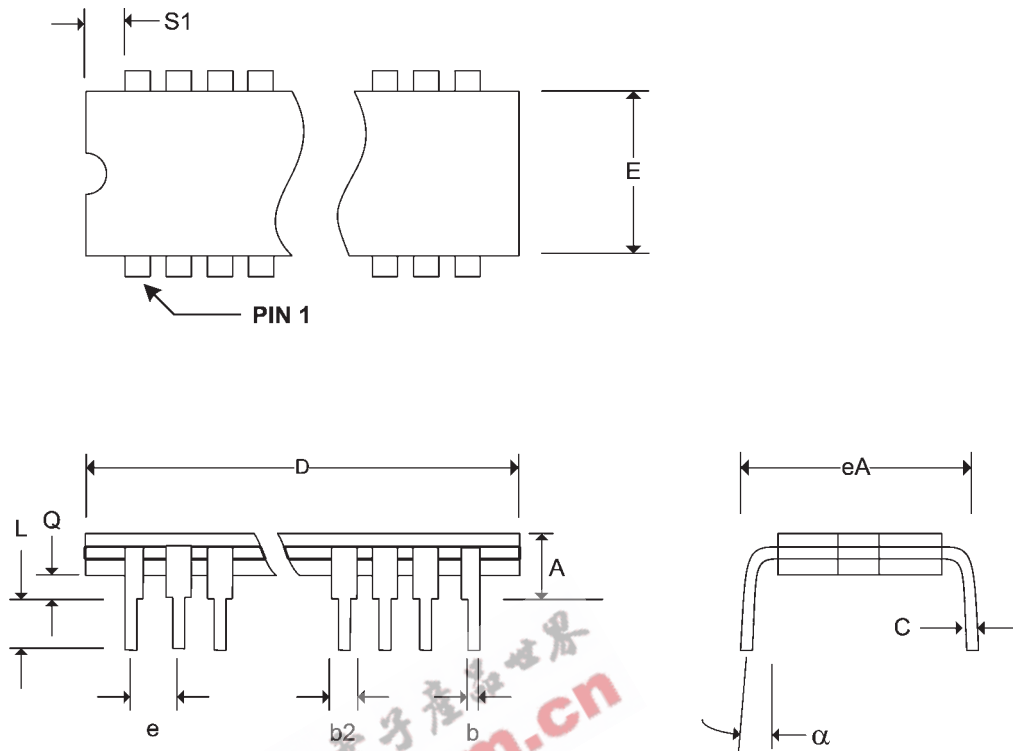
| | | |
|--------|--------------|------------|
| Pkg # | C5-1 | |
| # Pins | 28 (600 mil) | |
| Symbol | Min | Max |
| A | - | 0.232 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.490 |
| E | 0.500 | 0.610 |
| eA | 0.600 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.060 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

SIDE BRAZED DUAL IN-LINE PACKAGE (600 mils)



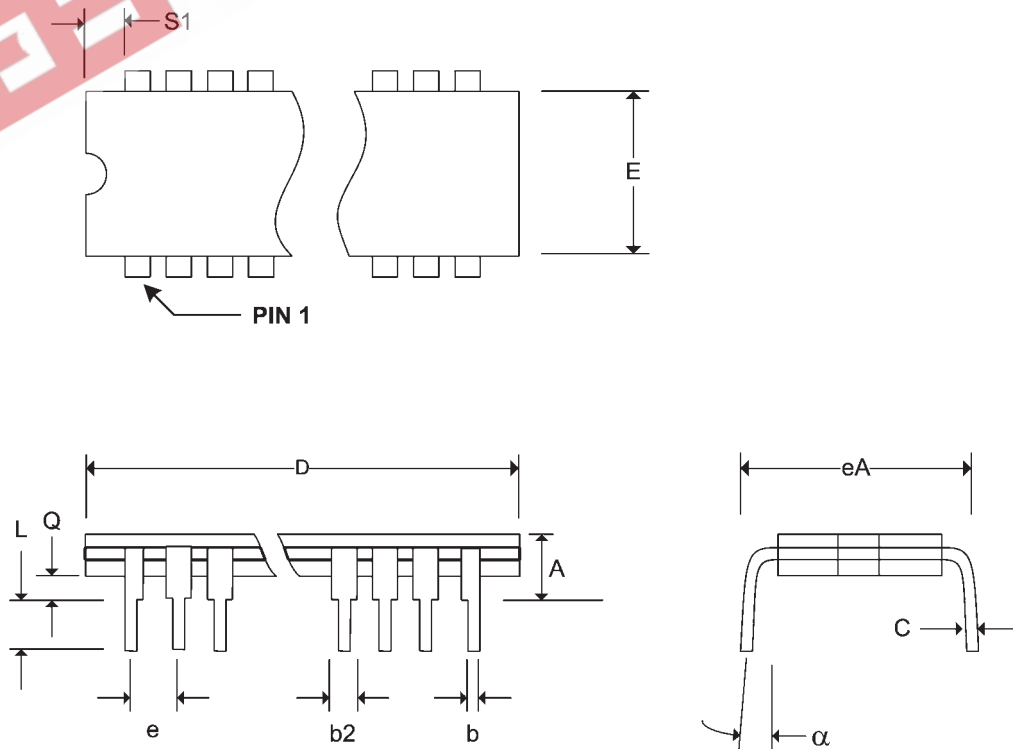
| Pkg # | D5-1 | |
|----------|--------------|-------|
| # Pins | 28 (600 mil) | |
| Symbol | Min | Max |
| A | - | 0.232 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.490 |
| E | 0.500 | 0.610 |
| eA | 0.600 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.060 |
| S1 | 0.005 | - |
| α | 0° | 15° |

CERDIP DUAL IN-LINE PACKAGE



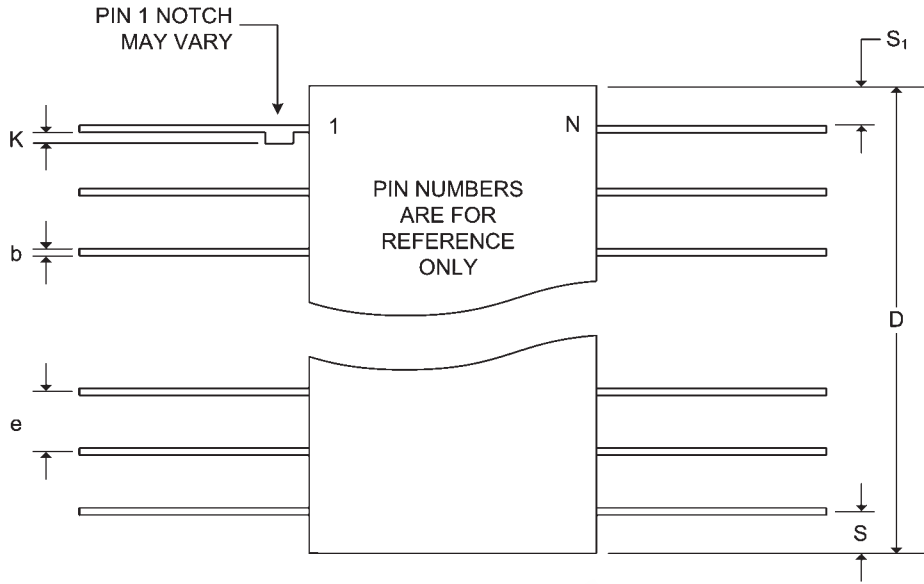
| Pkg # | D5-2 | |
|----------|--------------|-------|
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.225 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.485 |
| E | 0.240 | 0.310 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.060 |
| S1 | 0.005 | - |
| α | 0° | 15° |

CERDIP DUAL IN-LINE PACKAGE



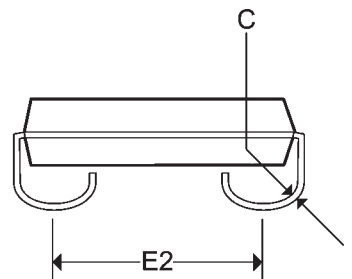
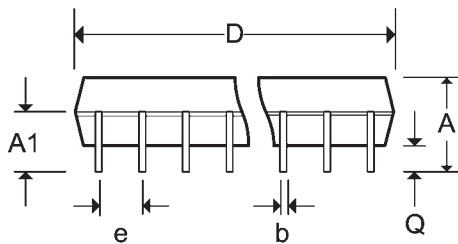
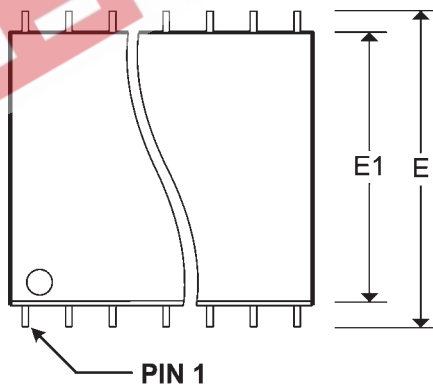
| Pkg # | F4 | |
|--------|-----------|-------|
| # Pins | 28 | |
| Symbol | Min | Max |
| A | 0.060 | 0.090 |
| b | 0.015 | 0.022 |
| c | 0.004 | 0.009 |
| D | - | 0.730 |
| E | 0.330 | 0.380 |
| e | 0.050 BSC | |
| k | 0.005 | 0.018 |
| L | 0.250 | 0.370 |
| Q | 0.026 | 0.045 |
| S | - | 0.085 |
| S1 | 0.005 | - |

CERPACK CERAMIC FLAT PACKAGE



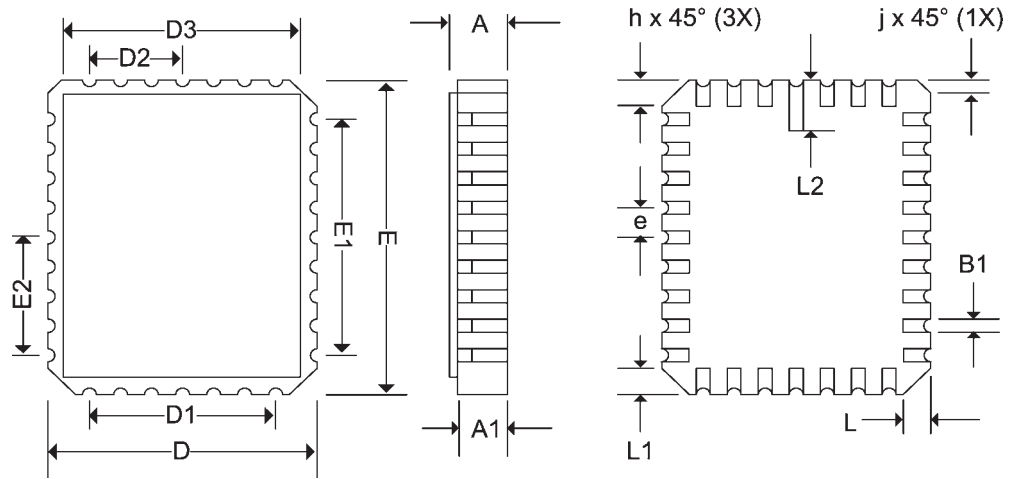
| Pkg # | J5 | |
|--------|--------------|-------|
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | 0.120 | 0.148 |
| A1 | 0.078 | - |
| b | 0.014 | 0.020 |
| C | 0.007 | 0.011 |
| D | 0.700 | 0.730 |
| e | 0.050 BSC | |
| E | 0.335 BSC | |
| E1 | 0.292 | 0.300 |
| E2 | 0.267 BSC | |
| Q | 0.025 | - |

SOJ SMALL OUTLINE IC PACKAGE



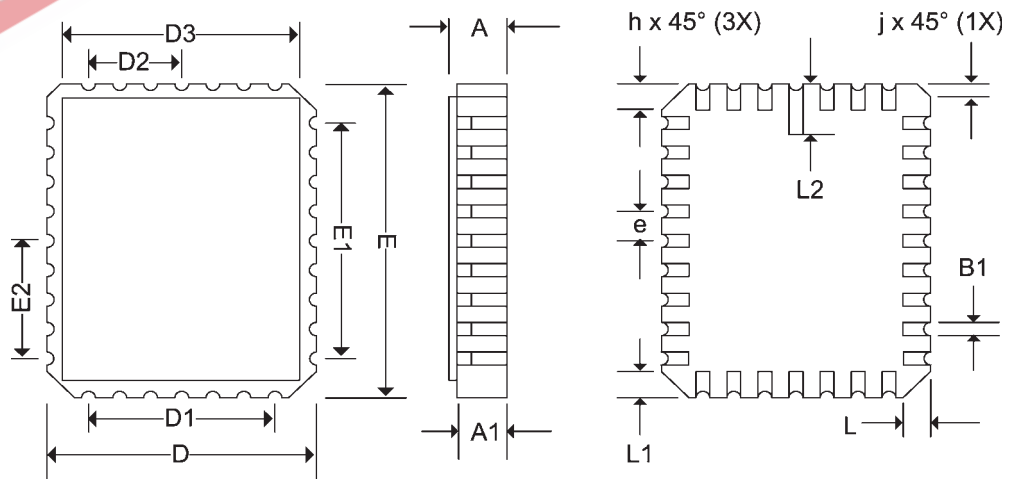
| | | |
|--------|------------|------------|
| Pkg # | L5 | |
| # Pins | 28 | |
| Symbol | Min | Max |
| A | 0.060 | 0.075 |
| A1 | 0.050 | 0.065 |
| B1 | 0.022 | 0.028 |
| D | 0.342 | 0.358 |
| D1 | 0.200 BSC | |
| D2 | 0.100 BSC | |
| D3 | - | 0.358 |
| E | 0.540 | 0.560 |
| E1 | 0.400 BSC | |
| E2 | 0.200 BSC | |
| E3 | - | 0.558 |
| e | 0.050 BSC | |
| h | 0.040 REF | |
| j | 0.020 REF | |
| L | 0.045 | 0.055 |
| L1 | 0.045 | 0.055 |
| L2 | 0.075 | 0.095 |
| ND | 5 | |
| NE | 9 | |

RECTANGULAR LEADLESS CHIP CARRIER



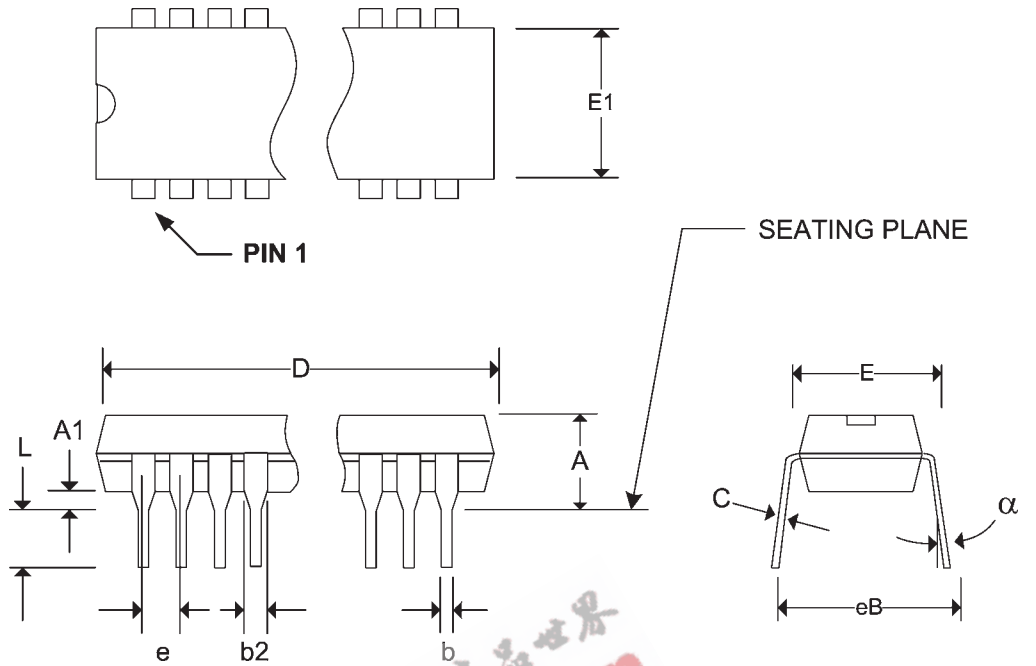
| | | |
|--------|------------|------------|
| Pkg # | L6 | |
| # Pins | 32 | |
| Symbol | Min | Max |
| A | 0.060 | 0.075 |
| A1 | 0.050 | 0.065 |
| B1 | 0.022 | 0.028 |
| D | 0.442 | 0.458 |
| D1 | 0.300 BSC | |
| D2 | 0.150 BSC | |
| D3 | - | 0.458 |
| E | 0.540 | 0.560 |
| E1 | 0.400 BSC | |
| E2 | 0.200 BSC | |
| E3 | - | 0.558 |
| e | 0.050 BSC | |
| h | 0.040 REF | |
| j | 0.020 REF | |
| L | 0.045 | 0.055 |
| L1 | 0.045 | 0.055 |
| L2 | 0.075 | 0.095 |
| ND | 7 | |
| NE | 9 | |

RECTANGULAR LEADLESS CHIP CARRIER



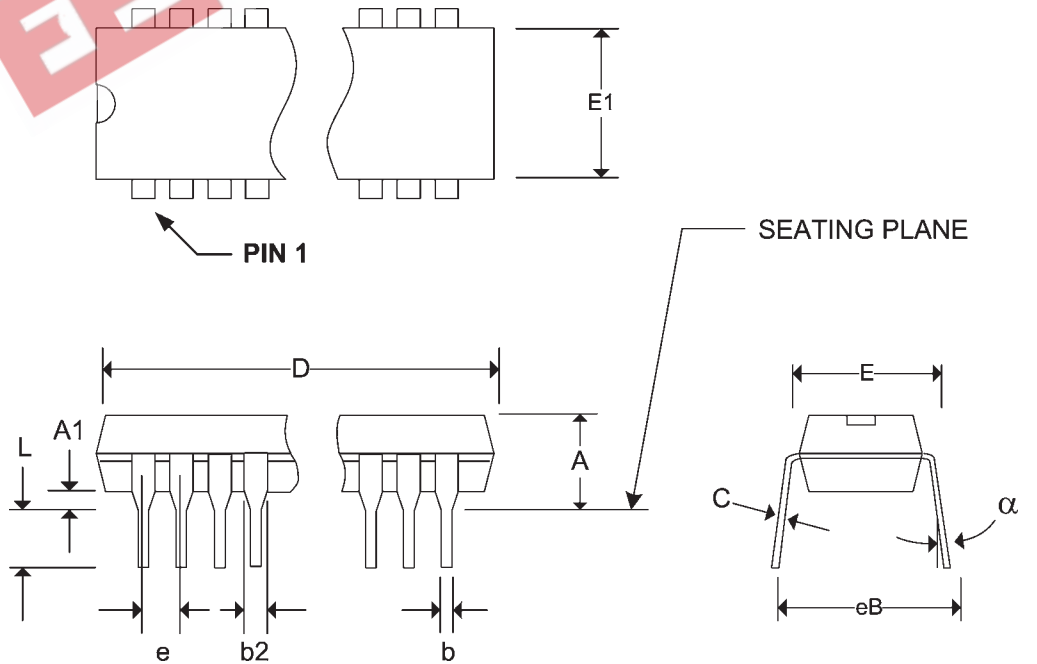
| Pkg # | P5 | |
|----------|--------------|-------|
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.210 |
| A1 | - | - |
| b | 0.014 | 0.023 |
| b2 | 0.045 | 0.070 |
| C | 0.008 | 0.014 |
| D | 1.345 | 1.400 |
| E1 | 0.270 | 0.300 |
| E | 0.300 | 0.380 |
| e | 0.100 BSC | |
| eB | - | 0.430 |
| L | 0.115 | 0.150 |
| α | 0° | 15° |

PLASTIC DUAL IN-LINE PACKAGE (300 mils)



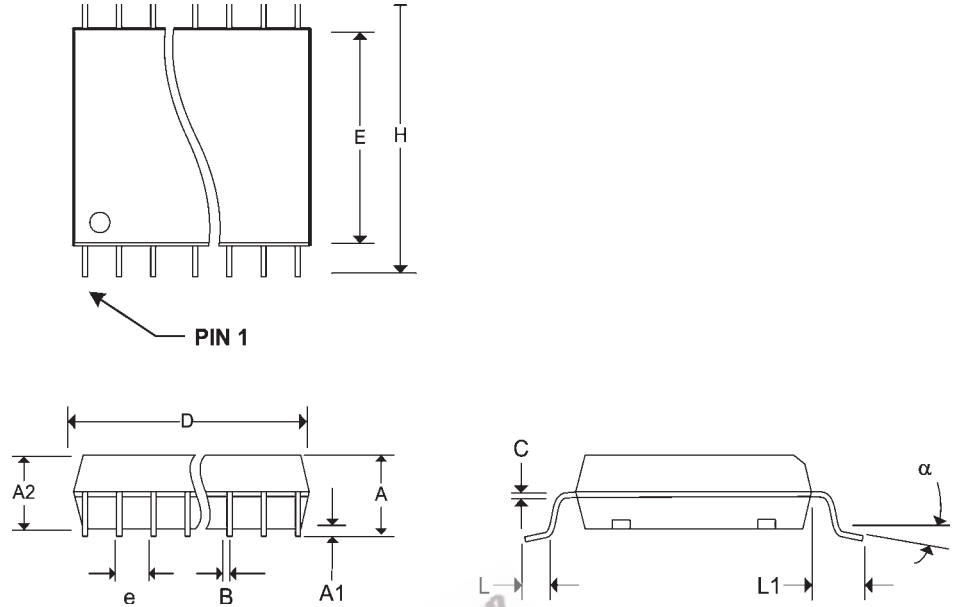
| Pkg # | P6 | |
|----------|--------------|-------|
| # Pins | 28 (600 mil) | |
| Symbol | Min | Max |
| A | 0.090 | 0.200 |
| A1 | 0.000 | 0.070 |
| b | 0.014 | 0.020 |
| b2 | 0.015 | 0.065 |
| C | 0.008 | 0.012 |
| D | 1.380 | 1.480 |
| E1 | 0.485 | 0.550 |
| E | 0.600 | 0.625 |
| e | 0.100 BSC | |
| eB | 0.600 TYP | |
| L | 0.100 | 0.200 |
| α | 0° | 15° |

PLASTIC DUAL IN-LINE PACKAGE (600 mils)



| | | |
|----------|--------------|------------|
| Pkg # | S6 | |
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | 0.090 | 0.110 |
| A1 | 0.003 | 0.010 |
| B | 0.012 | 0.020 |
| C | 0.004 | 0.012 |
| D | 0.700 | 0.716 |
| e | 0.050 BSC | |
| E | 0.290 | 0.300 |
| H | 0.465 | 0.485 |
| L | 0.016 | 0.050 |
| α | 0° | 9° |

SOIC/SOP SMALL OUTLINE IC PACKAGE (SN)



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REVISIONS

| DOCUMENT NUMBER: | | SRAM115 | |
|-------------------------|------------|---|---------------------------------|
| DOCUMENT TITLE: | | P4C164 ULTRA HIGH SPEED 8K x 8 STATIC CMOS RAMS | |
| REV. | ISSUE DATE | ORIG. OF CHANGE | DESCRIPTION OF CHANGE |
| OR | 1997 | DAB | New Data Sheet |
| A | Oct-05 | JDB | Change logo to Pyramid |
| B | Jun-06 | JDB | Added 28-pin ceramic DIP |
| C | Aug-06 | JDB | Added Lead Free Designation |
| D | Aug-06 | JDB | Added "LS" - SPECIAL PIN-OUT |
| E | Aug-06 | JDB | Updated SOJ package information |
| F | Jun-07 | JDB | Corrected SOP package details |
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