

P4C1256

HIGH SPEED 32K x 8

STATIC CMOS RAM

FEATURES

- High Speed (Equal Access and Cycle Times)
 - 12/15/20/25/35 ns (Commercial)
 - 15/20/25/35/45 ns (Industrial)
 - 20/25/35/45/55/70 ns (Military)
- Low Power
- Single 5V±10% Power Supply
- Easy Memory Expansion Using CE and OE Inputs
- Common Data I/O
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Fast t_{OE}
- Automatic Power Down
- Packages
 - 28-Pin 300 mil DIP, SOJ, TSOP
 - 28-Pin 300 mil Ceramic DIP
 - 28-Pin 600 mil Ceramic DIP
 - 28-Pin CERPACK
 - 28-Pin SOP
 - 28-Pin LCC (350 mil x 550 mil)
 - 32-Pin LCC (450 mil x 550 mil)

DESCRIPTION

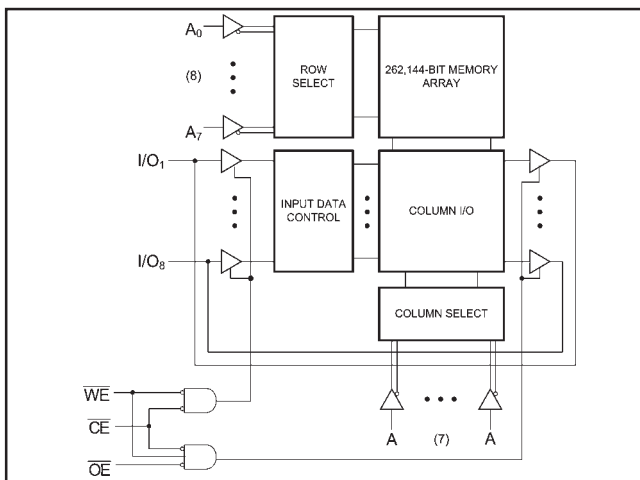
The P4C1256 is a 262,144-bit high-speed CMOS static RAM organized as 32Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

Access times as fast as 12 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1256 is a member of a family of PACE RAM™ products offering fast access times.

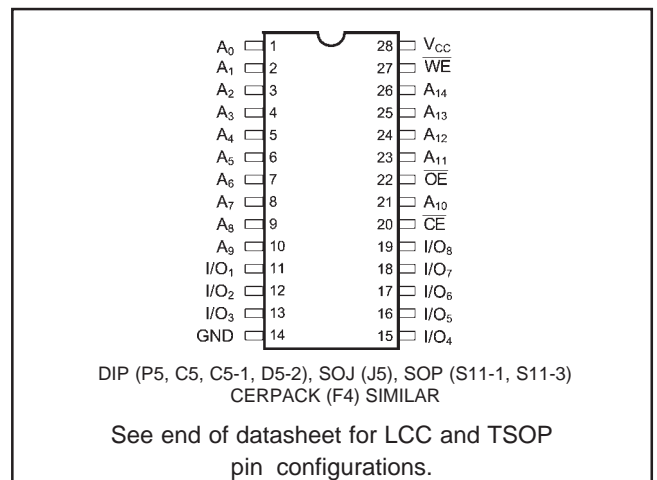
The P4C1256 device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{14} . Reading is accomplished by device selection (CE and output enabling (OE) while write enable (WE) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either CE or OE is HIGH or WE is LOW.

Package options for the P4C1256 include 28-pin 300 mil DIP, SOJ and TSOP packages. For military temperature range, Ceramic DIP and LCC packages are available.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------------|------|
| V _{CC} | Power Supply Pin with Respect to GND | -0.5 to +7 | V |
| V _{TERM} | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 to V _{CC} +0.5 | V |
| T _A | Operating Temperature | -55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|-------------------|------------------------|-------------|------|
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | mA |

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade(2) | Ambient Temperature | GND | V _{CC} |
|------------|---------------------|-----|-----------------|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

CAPACITANCES⁽⁴⁾

V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz

| Symbol | Parameter | Conditions | Typ. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 8 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 10 | pF |

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage⁽²⁾

| Symbol | Parameter | Test Conditions | P4C1256 | | P4C1256L | | Unit |
|------------------|--|---|----------------------|----------------------|----------------------|----------------------|------|
| | | | Min | Max | Min | Max | |
| V _{IH} | Input High Voltage | | 2.2 | V _{CC} +0.5 | 2.2 | V _{CC} +0.5 | V |
| V _{IL} | Input Low Voltage | | -0.5 ⁽³⁾ | 0.8 | -0.5 ⁽³⁾ | 0.8 | V |
| V _{HC} | CMOS Input High Voltage | | V _{CC} -0.2 | V _{CC} +0.5 | V _{CC} -0.2 | V _{CC} +0.5 | V |
| V _{LC} | CMOS Input Low Voltage | | -0.5 ⁽³⁾ | 0.2 | -0.5 ⁽³⁾ | 0.2 | V |
| V _{OL} | Output Low Voltage (TTL Load) | I _{OL} = +8 mA, V _{CC} = Min. | | 0.4 | | 0.4 | V |
| V _{OH} | Output High Voltage (TTL Load) | I _{OH} = -4 mA, V _{CC} = Min. | 2.4 | | 2.4 | | V |
| I _{LI} | Input Leakage Current | V _{CC} = Max. Mil. | -10 | +10 | -5 | +5 | µA |
| | | V _{IN} = GND to V _{CC} Ind./Com'l. | -5 | +5 | n/a | n/a | |
| I _{LO} | Output Leakage Current | V _{CC} = Max., Mil. | -10 | +10 | -5 | +5 | µA |
| | | CE = V _{IH} , Ind./Com'l. V _{OUT} = GND to V _{CC} | -5 | +5 | n/a | n/a | |
| I _{SB} | Standby Power Supply Current (TTL Input Levels) | CE ≥ V _{IH} Mil. | — | 45 | — | 30 | mA |
| | | V _{CC} = Max, Ind./Com'l. f = Max., Outputs Open | — | 30 | — | n/a | |
| I _{SB1} | Standby Power Supply Current (CMOS Input Levels) | CE ≥ V _{HC} Mil. | — | 20 | — | 10 | mA |
| | | V _{CC} = Max, Ind./Com'l. f = 0, Outputs Open V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC} | — | 10 | — | n/a | |

N/A = Not Applicable

DATA RETENTION CHARACTERISTICS (P4C1256L Military Temperature Only)

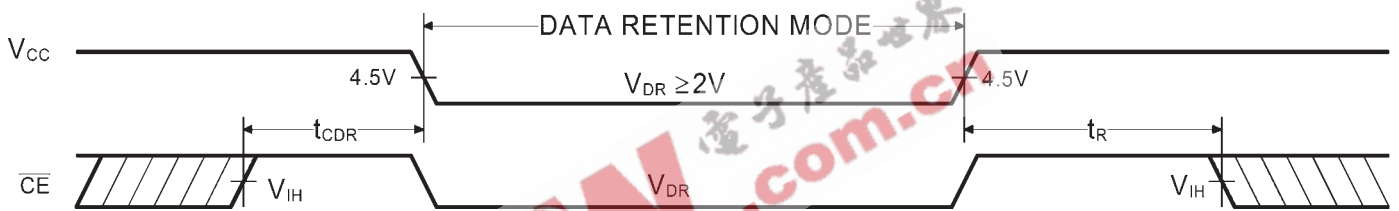
| Symbol | Parameter | Test Conditions | Min | Typ.* | | Max | | Unit |
|---------------|--------------------------------------|---|-------------|-----------------|-----------------|-----------------|-----------------|---------|
| | | | | $V_{CC} = 2.0V$ | $V_{CC} = 3.0V$ | $V_{CC} = 2.0V$ | $V_{CC} = 3.0V$ | |
| V_{DR} | V_{CC} for Data Retention | | 2.0 | | | | | V |
| I_{CCDR} | Data Retention Current | $CE \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 10 | 15 | 100 | 200 | μA |
| t_{CDR} | Chip Deselect to Data Retention Time | | 0 | | | | | ns |
| t_R^\dagger | Operation Recovery Time | | t_{RC}^\S | | | | | ns |

* $T_A = +25^\circ C$

t_{RC}^\S = Read Cycle Time

† This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | -12 | -15 | -20 | -25 | -35 | -45 | -55 | -70 | Unit |
|----------|----------------------------|-------------------|------------|------------|----------|-----|-----|-----|-----|-----|------|
| | | | Commercial | Industrial | Military | | | | | | |
| I_{CC} | Dynamic Operating Current* | Commercial | 170 | 160 | 155 | 150 | 145 | N/A | N/A | N/A | mA |
| | | Industrial | N/A | 170 | 165 | 160 | 155 | 150 | N/A | N/A | mA |
| | | Military | N/A | N/A | 170 | 165 | 160 | 155 | 150 | 150 | mA |

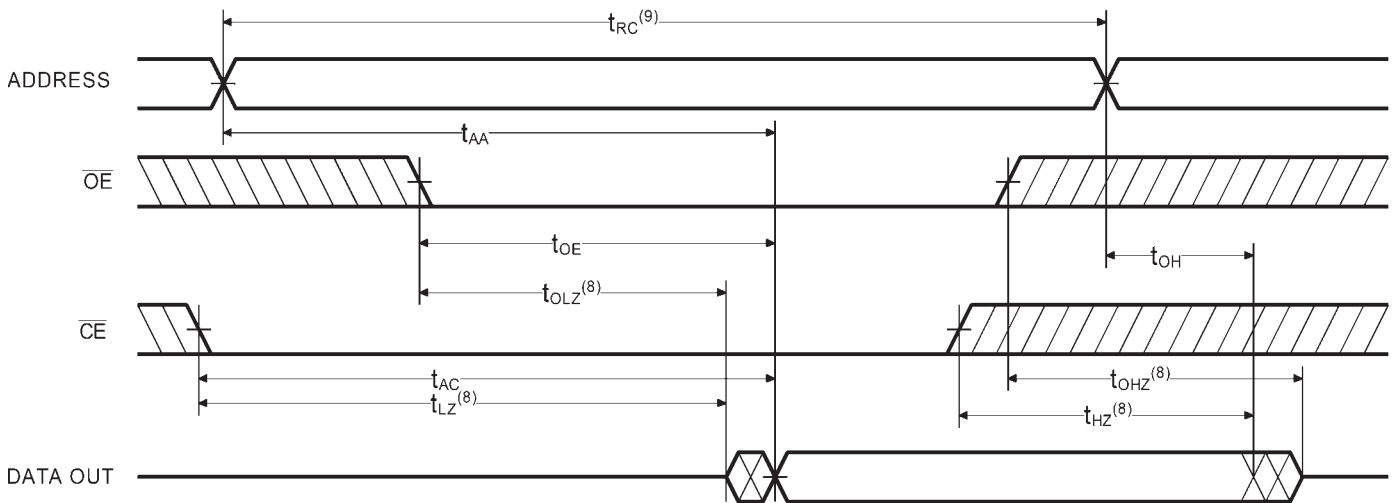
* $V_{CC} = 5.5V$. Tested with outputs open. $f = \text{Max}$. Switching inputs are 0V and 3V. $CE = V_{IL}$, $OE = V_{IH}$.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

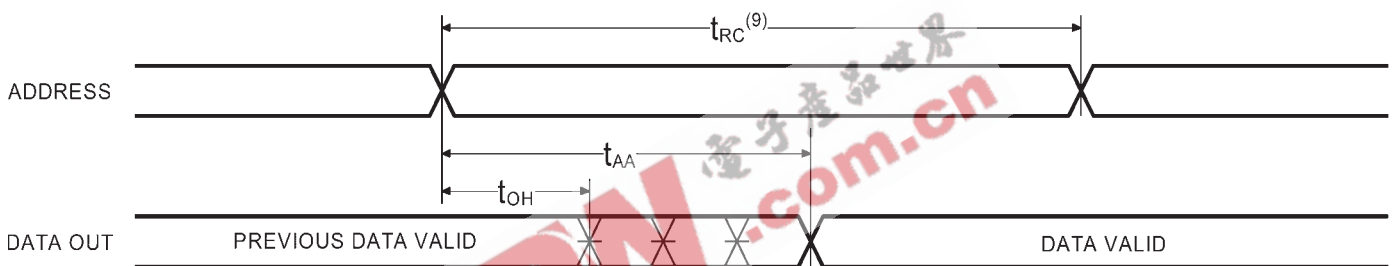
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

| Sym. | Parameter | -12 | | -15 | | -20 | | -25 | | -35 | | -45 | | -55 | | -70 | | Unit |
|-----------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{RC} | Read Cycle Time | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 55 | | 70 | | ns |
| t_{AA} | Address Access Time | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 55 | | 70 | ns |
| t_{AC} | Chip Enable Access Time | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 55 | | 70 | ns |
| t_{OH} | Output Hold from Address Change | 2 | | 2 | | 2 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t_{LZ} | Chip Enable to Output in Low Z | 2 | | 2 | | 2 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| t_{HZ} | Chip Disable to Output in High Z | | 5 | | 8 | | 9 | | 11 | | 15 | | 20 | | 25 | | 30 | ns |
| t_{OE} | Output Enable Low to Data Valid | | 5 | | 7 | | 9 | | 10 | | 15 | | 20 | | 25 | | 30 | ns |
| t_{OLZ} | Output Enable Low to Low Z | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{OHZ} | Output Enable High to High Z | | 5 | | 7 | | 9 | | 11 | | 15 | | 20 | | 25 | | 30 | ns |
| t_{PU} | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{PD} | Chip Disable to Power Down Time | | 12 | | 15 | | 20 | | 20 | | 20 | | 25 | | 30 | | 35 | ns |

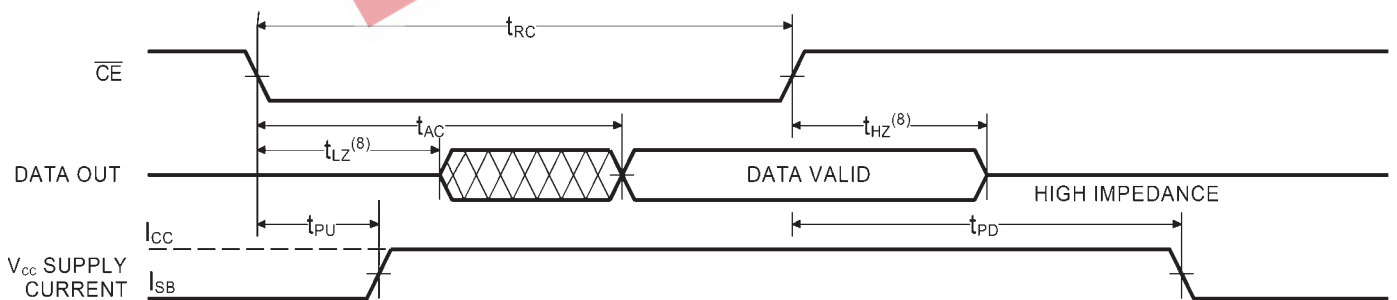
TIMING WAVEFORM OF READ CYCLE NO. 1 (OE CONTROLLED)⁽⁵⁾



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)^(5,6)



TIMING WAVEFORM OF READ CYCLE NO. 3 (CE CONTROLLED)^(5,7)



Notes:

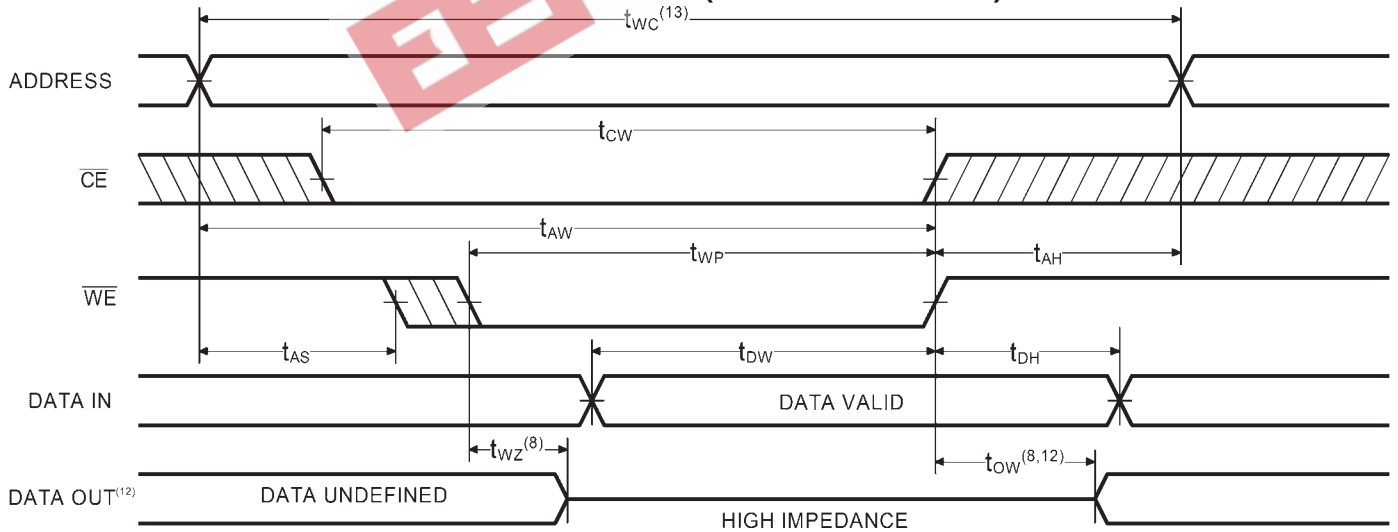
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than $-3.0V$ and $-100mA$, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.
5. WE is HIGH for READ cycle.
6. CE is LOW and OE is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with CE transition LOW.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

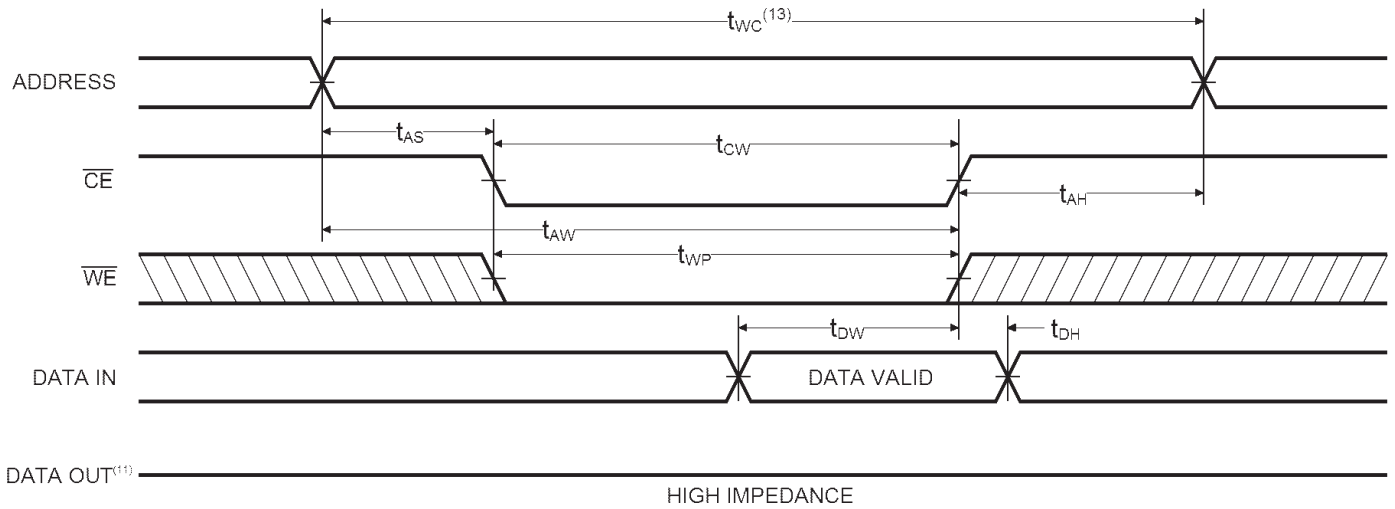
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

| Sym. | Parameter | -12 | | -15 | | -20 | | -25 | | -35 | | -45 | | -55 | | -70 | | Unit |
|----------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{WC} | Write Cycle Time | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | 55 | | 70 | | ns |
| t_{CW} | Chip Enable Time to End of Write | 9 | | 10 | | 15 | | 18 | | 22 | | 30 | | 35 | | 40 | | ns |
| t_{AW} | Address Valid to End of Write | 9 | | 10 | | 15 | | 20 | | 25 | | 35 | | 40 | | 45 | | ns |
| t_{AS} | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WP} | Write Pulse Width | 9 | | 11 | | 15 | | 18 | | 22 | | 25 | | 30 | | 35 | | ns |
| t_{AH} | Address Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{DW} | Data Valid to End of Write | 8 | | 9 | | 11 | | 13 | | 15 | | 20 | | 25 | | 30 | | ns |
| t_{DH} | Date Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WZ} | Write Enable to Output in High Z | | 7 | | 8 | | 10 | | 11 | | 15 | | 18 | | 25 | | 30 | ns |
| t_{OW} | Output Active from End of Write | 3 | | 3 | | 3 | | 3 | | 5 | | 5 | | 0 | | 0 | | ns |

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED)^(10,11)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CE CONTROLLED)⁽¹⁰⁾



Notes:

- 10. \overline{CE} and \overline{WE} must be LOW for WRITE cycle.
- 11. \overline{OE} is LOW for this WRITE cycle to show t_{wz} and t_{ow} .
- 12. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains

- in a high impedance state
- 13. Write Cycle Time is measured from the last valid address to the first transitioning address.



AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

TRUTH TABLE

| Mode | CE | OE | WE | I/O | Power |
|---------------------------|----|----|----|------------------|---------|
| Standby | H | X | X | High Z | Standby |
| Standby | X | X | X | High Z | Standby |
| D _{OUT} Disabled | L | H | H | High Z | Active |
| Read | L | L | H | D _{OUT} | Active |
| Write | L | X | L | High Z | Active |

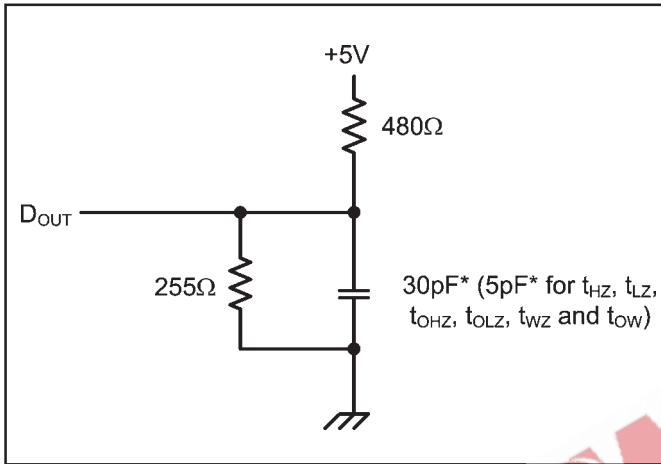


Figure 1. Output Load

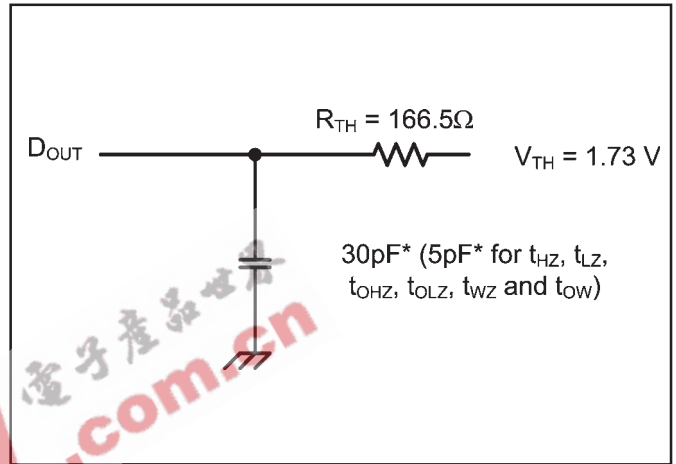


Figure 2. Thevenin Equivalent

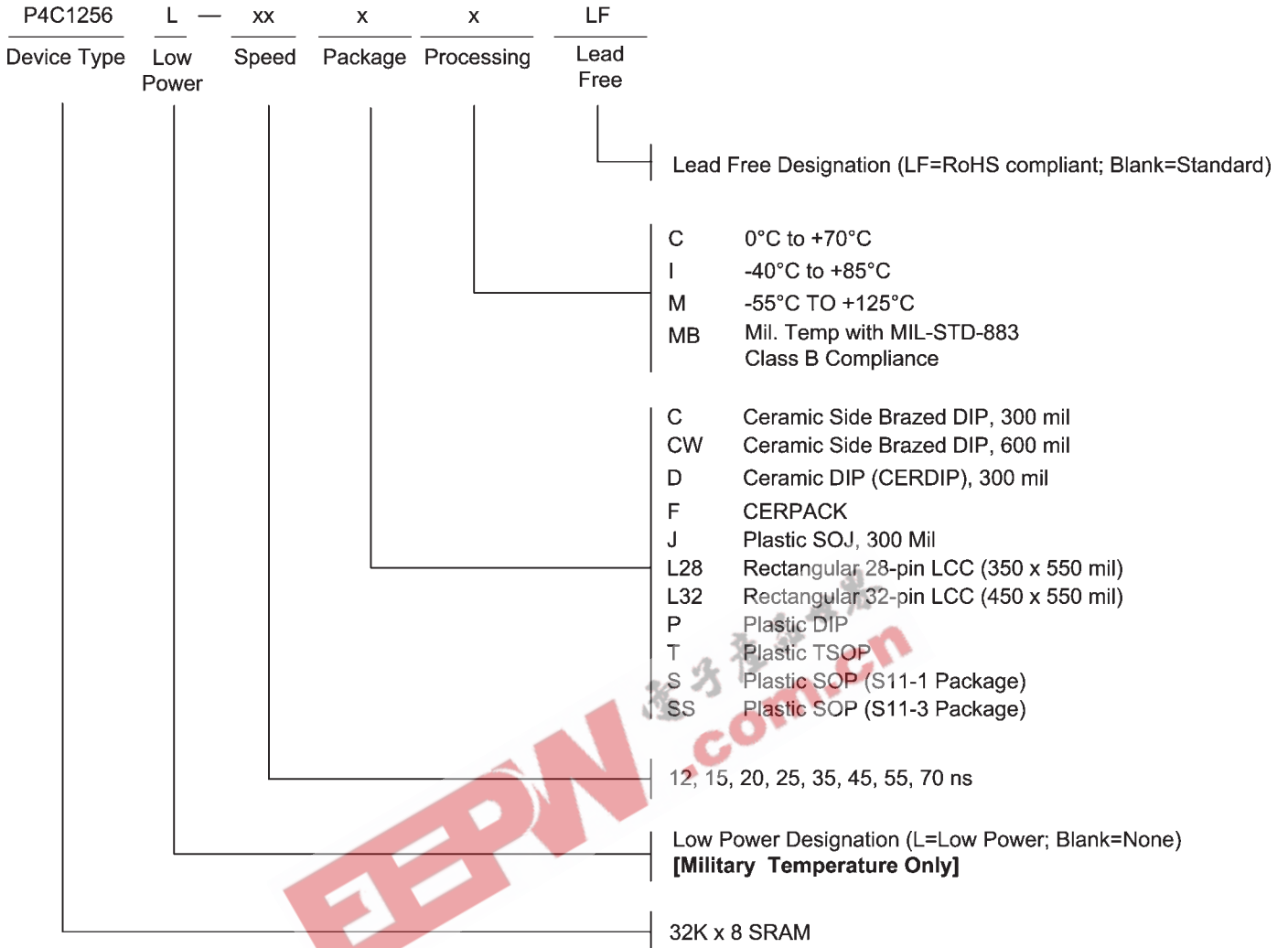
* including scope and test fixture.

Note:

Because of the ultra-high speed of the P4C1256, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination

must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



SELECTION GUIDE

The P4C1256 is available in the following temperature, speed and package options. The P4C1256L is available only over the military temperature range. **

| Temperature Range | Package | Speed | | | | | | | |
|-------------------|---------------------|--------|--------|--------|--------|--------|--------|-----|-----|
| | | 12 | 15 | 20 | 25 | 35 | 45 | 55 | 70 |
| Commercial | Plastic DIP | -12PC | -15PC | -20PC | -25PC | -35PC | N/A | N/A | N/A |
| | Plastic SOJ | -12JC | -15JC | -20JC | -25JC | -35JC | N/A | N/A | N/A |
| | Plastic TSOP | -12TC | -15TC | -20TC | -25TC | -35TC | N/A | N/A | N/A |
| | Plastic SOP (S11-1) | -12SC | -15SC | -20SC | -25SC | -35SC | N/A | N/A | N/A |
| | Plastic SOP (S11-3) | -12SSC | -15SSC | -20SSC | -25SSC | -35SSC | N/A | N/A | N/A |
| Industrial | Plastic DIP | N/A | -15PI | -20PI | -25PI | -35PI | -45PI | N/A | N/A |
| | Plastic SOJ | N/A | -15JI | -20JI | -25JI | -35JI | -45JI | N/A | N/A |
| | Plastic TSOP | N/A | -15TI | -20TI | -25TI | -35TI | -45TI | N/A | N/A |
| | Plastic SOP (S11-1) | N/A | -15SI | -20SI | -25SI | -35SI | -45SI | N/A | N/A |
| | Plastic SOP (S11-3) | N/A | -15SSI | -20SSI | -25SSI | -35SSI | -45SSI | N/A | N/A |

* Military temperature range with MIL-STD-883, Class B processing.

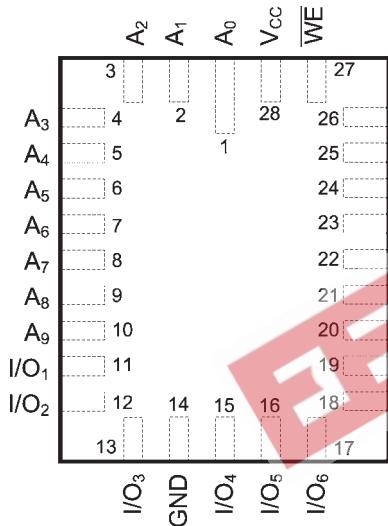
** For RoHS compliant plastic products, the suffix "LF" (Lead Free) should be added to the part number.

N/A = Not Available

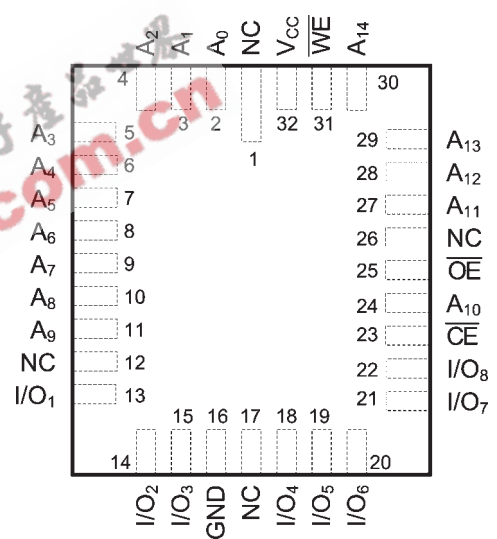
SELECTION GUIDE (CONTINUED)

| Temperature Range | Package | Speed | | | | | | | |
|----------------------|---------------------------|-------|-----|----------|----------|----------|----------|----------|----------|
| | | 12 | 15 | 20 | 25 | 35 | 45 | 55 | 70 |
| Military Temperature | Side Brazed DIP (300 mil) | N/A | N/A | -20CM | -25CM | -35CM | -45CM | -55CM | -70CM |
| | Side Brazed DIP (600 mil) | N/A | N/A | -20CWM | -25CWM | -35CWM | -45CWM | -55CWM | -70CWM |
| | Ceramic DIP | N/A | N/A | -20DM | -25DM | -35DM | -45DM | -55DM | -70DM |
| | CERPACK | N/A | N/A | -20FM | -25FM | -35FM | -45FM | -55FM | -70FM |
| | LCC (28-Pin) | N/A | N/A | -20L28M | -25L28M | -35L28M | -45L28M | -55L28M | -70L28M |
| | LCC (32-Pin) | N/A | N/A | -20L32M | -25L32M | -35L32M | -45L32M | -55L32M | -70L32M |
| Military Processed* | Side Brazed DIP (300 mil) | N/A | N/A | -20CMB | -25CMB | -35CMB | -45CMB | -55CMB | -70CMB |
| | Side Brazed DIP (600 mil) | N/A | N/A | -20CWMB | -25CWMB | -35CWMB | -45CWMB | -55CWMB | -70CWMB |
| | Ceramic DIP | N/A | N/A | -20DMB | -25DMB | -35DMB | -45DMB | -55DMB | -70DMB |
| | CERPACK | N/A | N/A | -20FMB | -25FMB | -35FMB | -45FMB | -55FMB | -70FMB |
| | LCC (28-Pin) | N/A | N/A | -20L28MB | -25L28MB | -35L28MB | -45L28MB | -55L28MB | -70L28MB |
| | LCC (32-Pin) | N/A | N/A | -20L32MB | -25L32MB | -35L32MB | -45L32MB | -55L32MB | -70L32MB |

LCC PIN CONFIGURATIONS



28 LCC (L5)



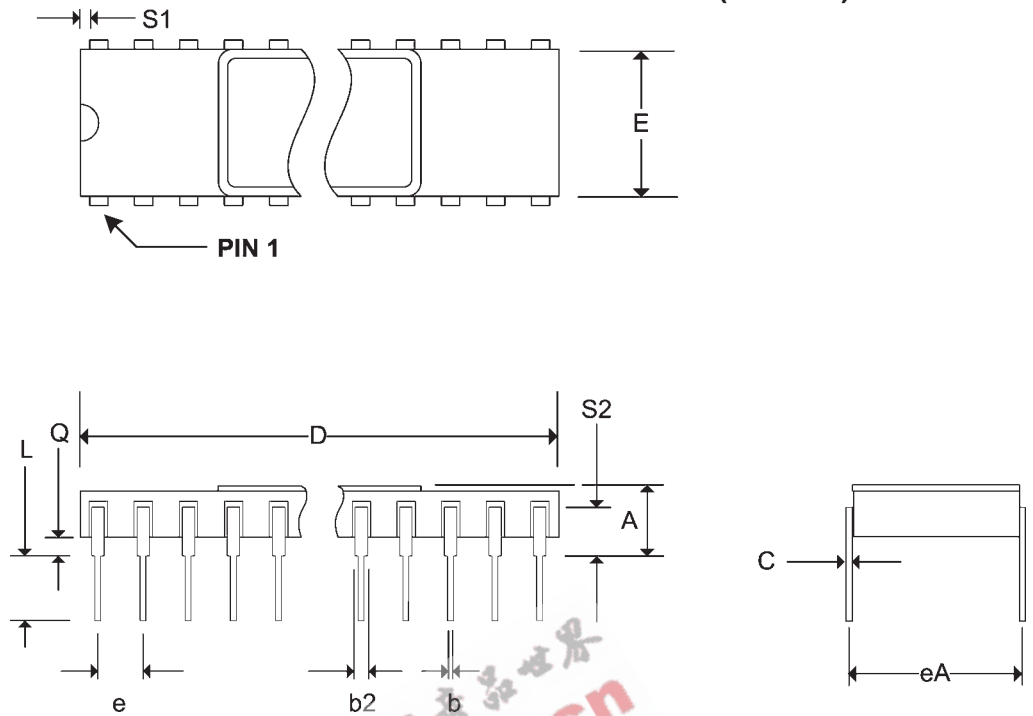
32 LCC (L6)



TSOP (T1)

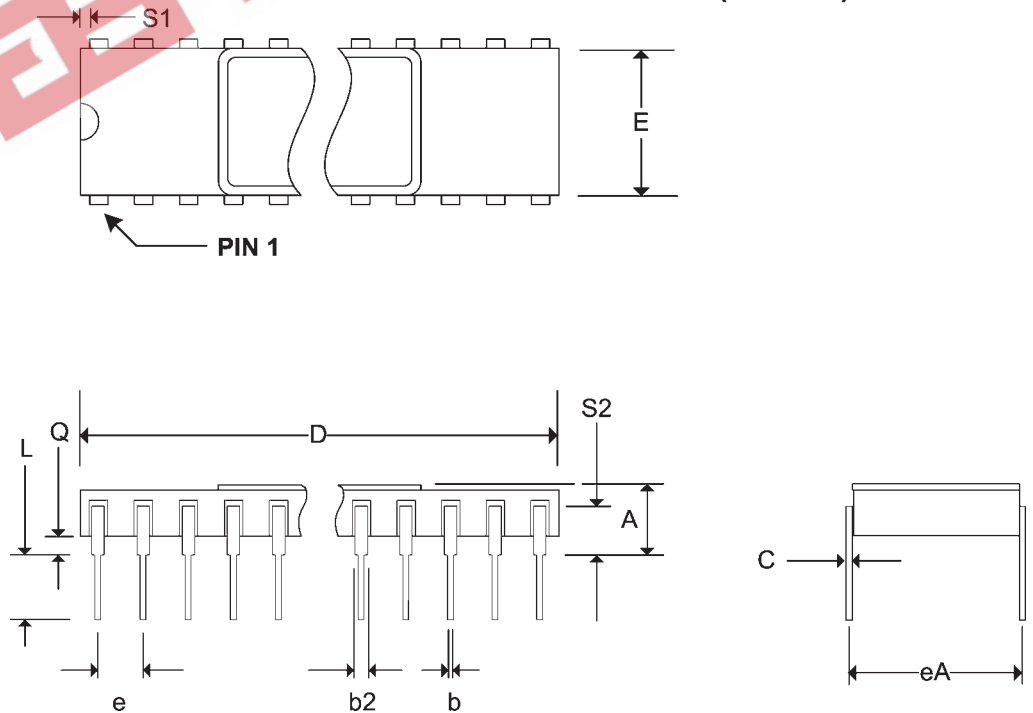
| | | |
|--------|--------------|------------|
| Pkg # | C5 | |
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.225 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.485 |
| E | 0.240 | 0.310 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.070 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

SIDE BRAZED CERAMIC DUAL IN-LINE PACKAGE (300 Mils)



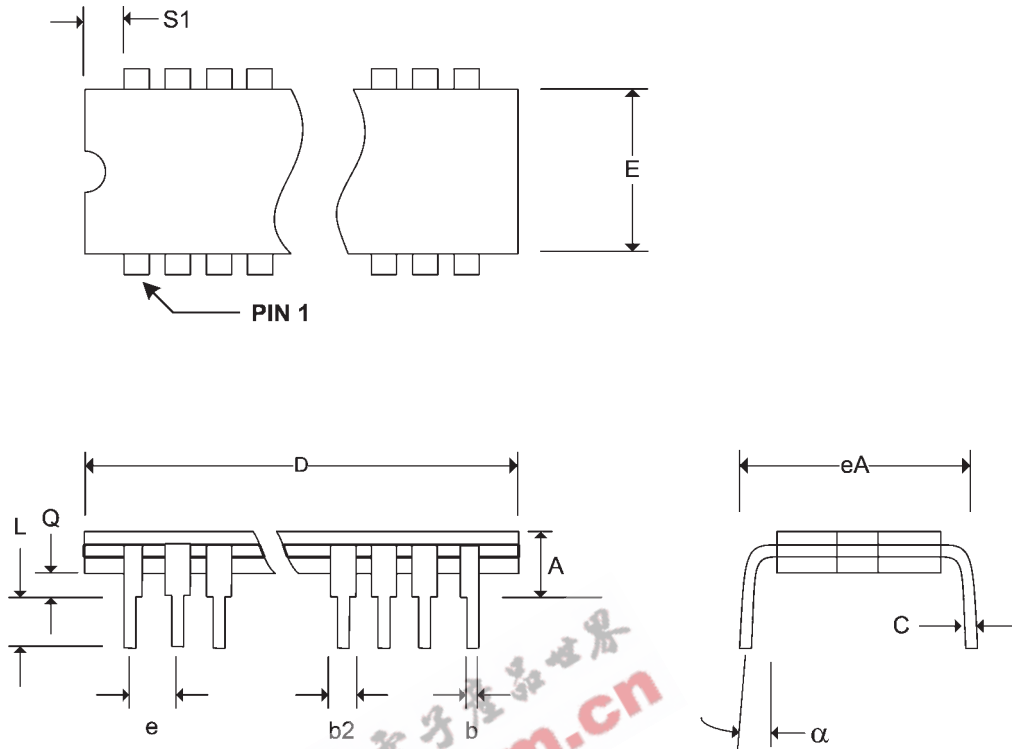
| | | |
|--------|--------------|------------|
| Pkg # | C5-1 | |
| # Pins | 28 (600 mil) | |
| Symbol | Min | Max |
| A | - | 0.232 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.490 |
| E | 0.500 | 0.610 |
| eA | 0.600 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.060 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

SIDE BRAZED CERAMIC DUAL IN-LINE PACKAGE (600 Mils)



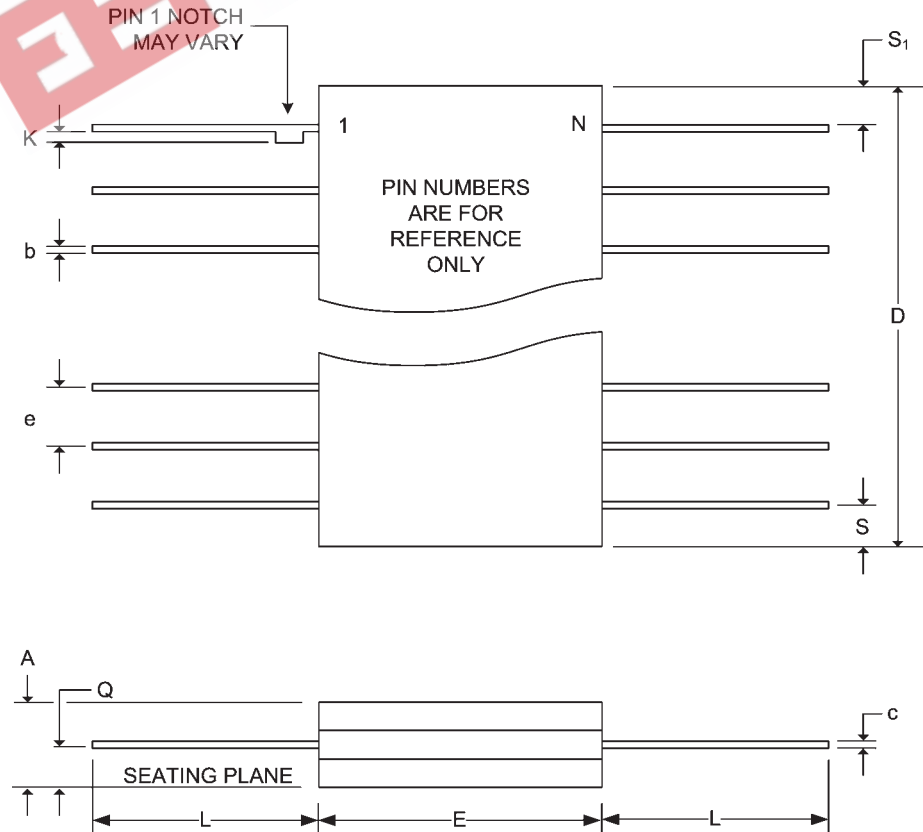
| Pkg # | D5-2 | |
|----------|--------------|-------|
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.225 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.485 |
| E | 0.240 | 0.310 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.060 |
| S1 | 0.005 | - |
| α | 0° | 15° |

CERDIP DUAL IN-LINE PACKAGE



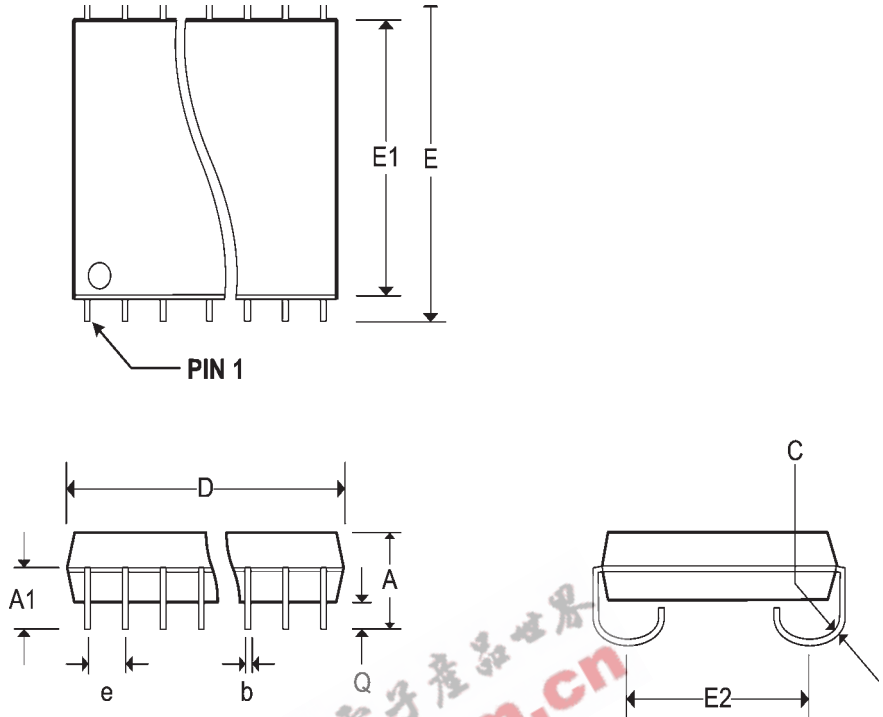
| Pkg # | F4 | |
|--------|-----------|-------|
| # Pins | 28 | |
| Symbol | Min | Max |
| A | 0.060 | 0.090 |
| b | 0.015 | 0.022 |
| c | 0.004 | 0.009 |
| D | - | 0.730 |
| E | 0.330 | 0.380 |
| e | 0.050 BSC | |
| k | 0.005 | 0.018 |
| L | 0.250 | 0.370 |
| Q | 0.026 | 0.045 |
| S | - | 0.085 |
| S1 | 0.005 | - |

CERPACK CERAMIC FLAT PACKAGE



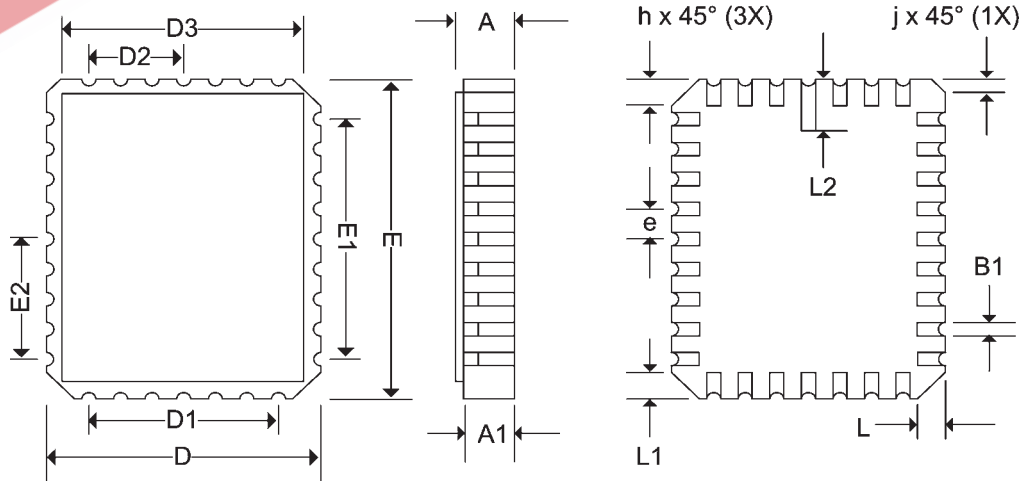
| | | |
|--------|--------------|------------|
| Pkg # | J5 | |
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | 0.120 | 0.148 |
| A1 | 0.078 | - |
| b | 0.014 | 0.020 |
| C | 0.007 | 0.011 |
| D | 0.700 | 0.730 |
| e | 0.050 BSC | |
| E | 0.335 BSC | |
| E1 | 0.292 | 0.300 |
| E2 | 0.267 BSC | |
| Q | 0.025 | - |

SOJ SMALL OUTLINE IC PACKAGE



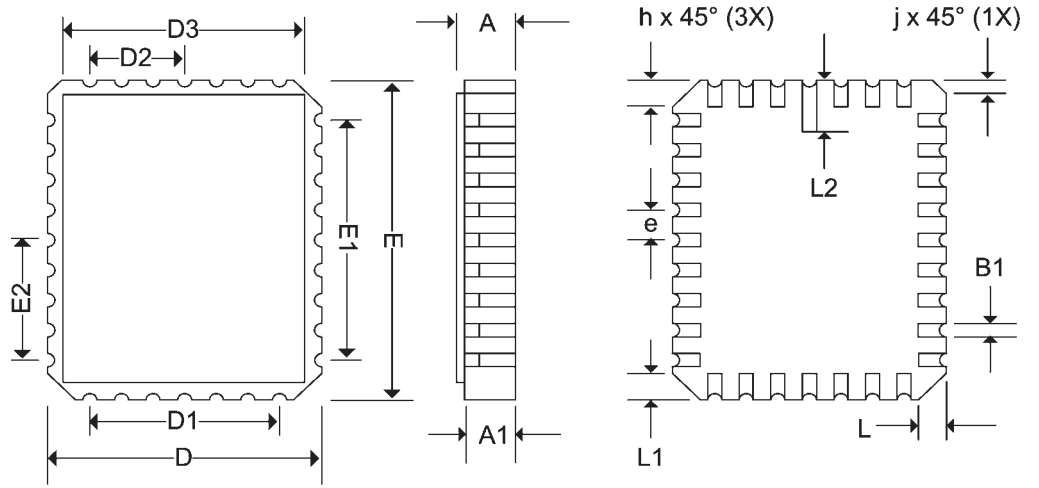
| | | |
|--------|------------|------------|
| Pkg # | L5 | |
| # Pins | 28 | |
| Symbol | Min | Max |
| A | 0.060 | 0.075 |
| A1 | 0.050 | 0.065 |
| B1 | 0.022 | 0.028 |
| D | 0.342 | 0.358 |
| D1 | 0.200 BSC | |
| D2 | 0.100 BSC | |
| D3 | - | 0.358 |
| E | 0.540 | 0.560 |
| E1 | 0.400 BSC | |
| E2 | 0.200 BSC | |
| E3 | - | 0.558 |
| e | 0.050 BSC | |
| h | 0.040 REF | |
| j | 0.020 REF | |
| L | 0.045 | 0.055 |
| L1 | 0.045 | 0.055 |
| L2 | 0.075 | 0.095 |
| ND | 5 | |
| NE | 9 | |

RECTANGULAR LEADLESS CHIP CARRIER (28 Pins)



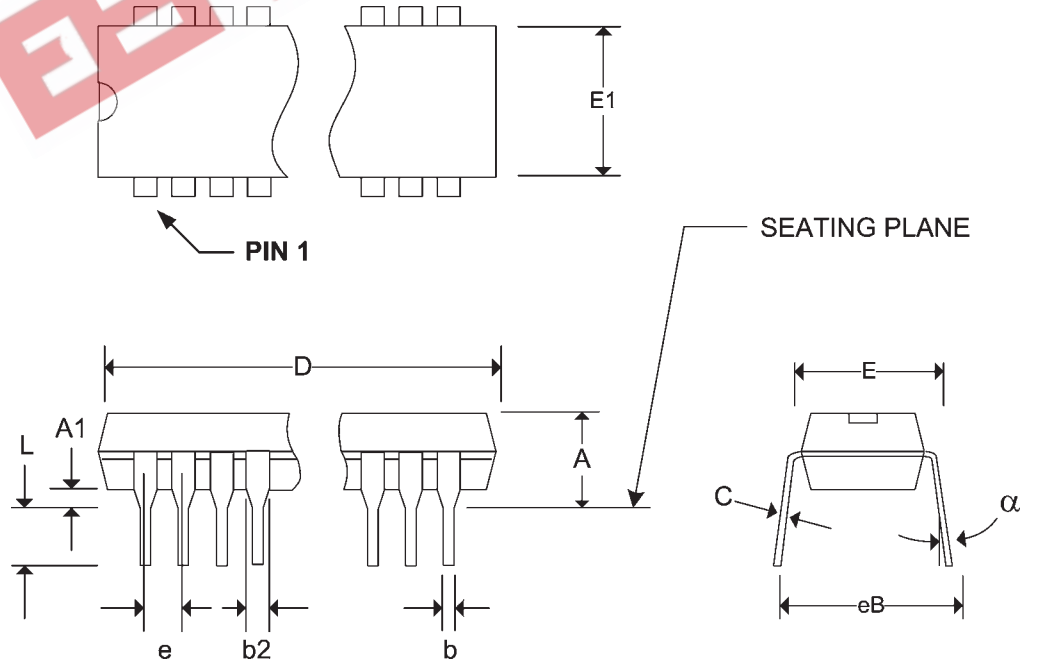
| Pkg # | L6 | |
|--------|-----------|-------|
| # Pins | 32 | |
| Symbol | Min | Max |
| A | 0.060 | 0.075 |
| A1 | 0.050 | 0.065 |
| B1 | 0.022 | 0.028 |
| D | 0.442 | 0.458 |
| D1 | 0.300 BSC | |
| D2 | 0.150 BSC | |
| D3 | - | 0.458 |
| E | 0.540 | 0.560 |
| E1 | 0.400 BSC | |
| E2 | 0.200 BSC | |
| E3 | - | 0.558 |
| e | 0.050 BSC | |
| h | 0.040 REF | |
| j | 0.020 REF | |
| L | 0.045 | 0.055 |
| L1 | 0.045 | 0.055 |
| L2 | 0.075 | 0.095 |
| ND | 7 | |
| NE | 9 | |

RECTANGULAR LEADLESS CHIP CARRIER (32 Pins)



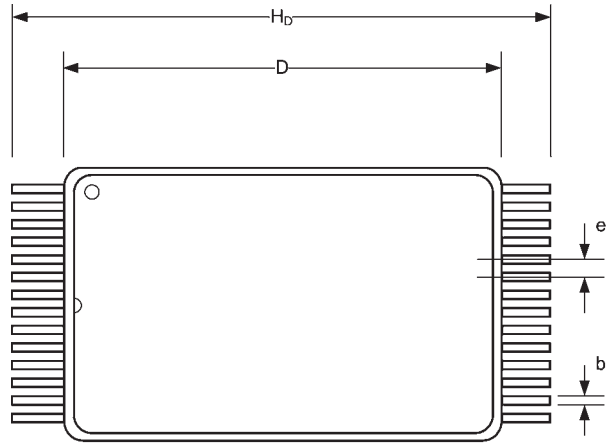
| Pkg # | P5 | |
|----------|--------------|-------|
| # Pins | 28 (300 mil) | |
| Symbol | Min | Max |
| A | - | 0.210 |
| A1 | - | - |
| b | 0.014 | 0.023 |
| b2 | 0.045 | 0.070 |
| C | 0.008 | 0.014 |
| D | 1.345 | 1.400 |
| E1 | 0.270 | 0.300 |
| E | 0.300 | 0.380 |
| e | 0.100 BSC | |
| eB | - | 0.430 |
| L | 0.115 | 0.150 |
| α | 0° | 15° |

PLASTIC DUAL IN-LINE PACKAGE

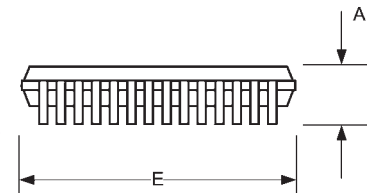
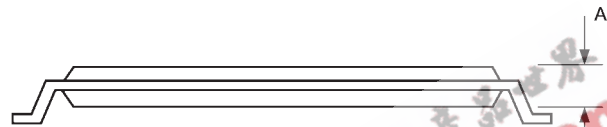


| | | |
|----------------|------------|------------|
| Pkg # | T1 | |
| # Pins | 28 | |
| Symbol | Min | Max |
| A | 0.039 | 0.047 |
| A ₂ | 0.036 | 0.040 |
| b | 0.007 | 0.011 |
| D | 0.461 | 0.469 |
| E | 0.311 | 0.319 |
| e | 0.022 BSC | |
| H _D | 0.520 | 0.535 |

TSOP THIN SMALL OUTLINE PACKAGE (8 x 13.4 mm)

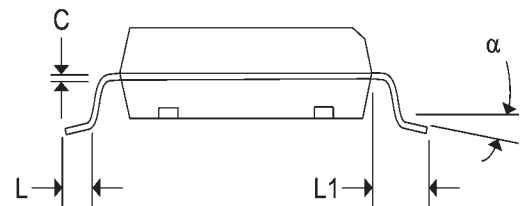
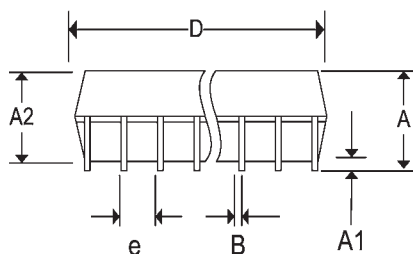
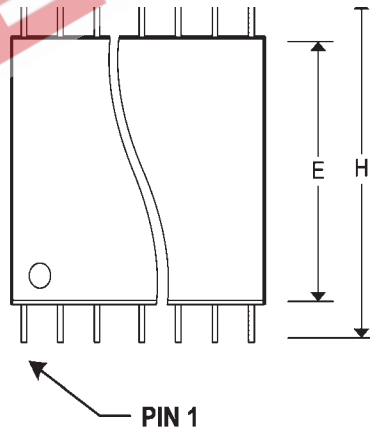


NOTE:
Orientation ID is either next to Pin 1 (midway along row of pins) or in corner on side of package containing Pin 1.



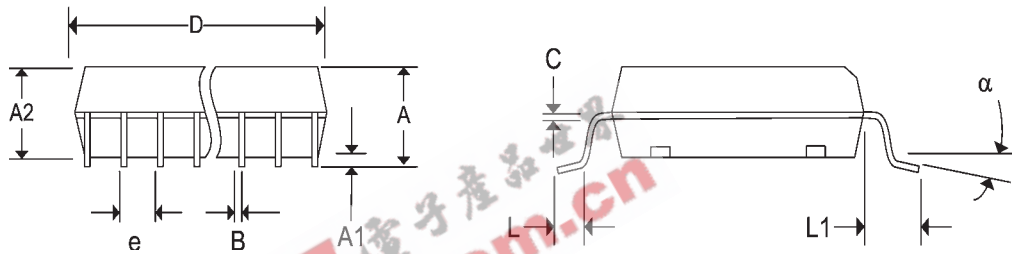
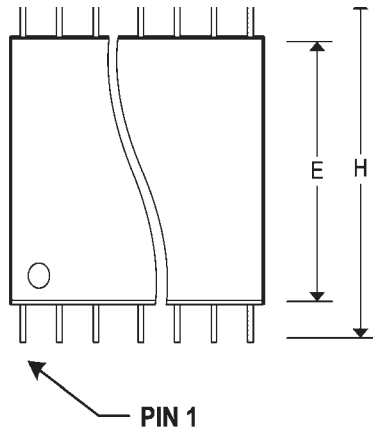
| | | |
|----------------|--------------|------------|
| Pkg # | S11-1 | |
| # Pins | 28 (300 Mil) | |
| Symbol | Min | Max |
| A | 0.093 | 0.104 |
| A ₁ | 0.004 | 0.012 |
| b ₂ | 0.013 | 0.020 |
| C | 0.009 | 0.012 |
| D | 0.696 | 0.712 |
| e | 0.050 BSC | |
| E | 0.291 | 0.299 |
| H | 0.394 | 0.419 |
| h | 0.010 | 0.029 |
| L | 0.016 | 0.050 |
| α | 0° | 8° |

SOIC/SOP SMALL OUTLINE IC PACKAGE



| | | |
|----------|--------------|------------|
| Pkg # | S11-3 | |
| # Pins | 28 (300 Mil) | |
| Symbol | Min | Max |
| A | 0.094 | 0.110 |
| A1 | 0.002 | 0.014 |
| B | 0.014 | 0.020 |
| C | 0.008 | 0.012 |
| D | 0.702 | 0.710 |
| e | 0.050 BSC | |
| E | 0.291 | 0.300 |
| H | 0.463 | 0.477 |
| h | 0.010 | 0.029 |
| L | 0.020 | 0.042 |
| α | 0° | 8° |

SOIC/SOP SMALL OUTLINE IC PACKAGE



REVISIONS

| DOCUMENT NUMBER: | | SRAM119 | |
|-------------------------|------------|------------------------------------|--|
| DOCUMENT TITLE: | | HIGH SPEED 32K x 8 STATIC CMOS RAM | |
| REV. | ISSUE DATE | ORIG. OF CHANGE | DESCRIPTION OF CHANGE |
| OR | 1997 | RKK | New Data Sheet |
| A | Oct-05 | JDB | Change logo to Pyramid |
| B | Oct-05 | JDB | Added SOP Package |
| C | Apr-06 | JDB | Added Lead-Free ordering information. |
| D | May-06 | JDB | Added PDIP to Ordering Information diagram |
| E | Jun-06 | JDB | Added Ceramic DIP package |
| F | Aug-06 | JDB | Updated SOJ package information |
| G | Jun-07 | JDB | Corrected SOP package information |
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