

P4C1048L

LOW POWER 512K x 8

CMOS STATIC RAM



FEATURES

- V_{CC} Current
 - Operating: 35mA
 - CMOS Standby: 100 μ A
- Access Times
 - 45/55/70/100 ns
- Single 5 Volts \pm 10% Power Supply
- Easy Memory Expansion Using \overline{CE} and \overline{OE} Inputs
- Common Data I/O
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Automatic Power Down
- Packages
 - 32-Pin 600 mil Plastic and Ceramic DIP
 - 32-Pin 445 mil SOP
 - 32-Pin TSOP II



DESCRIPTION

The P4C1048L is a 4 Megabit low power CMOS static RAM organized as 512K x 8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V \pm 10% tolerance power supply.

Access times as fast as 45 ns are available. CMOS is utilized to reduce power consumption to a low level.

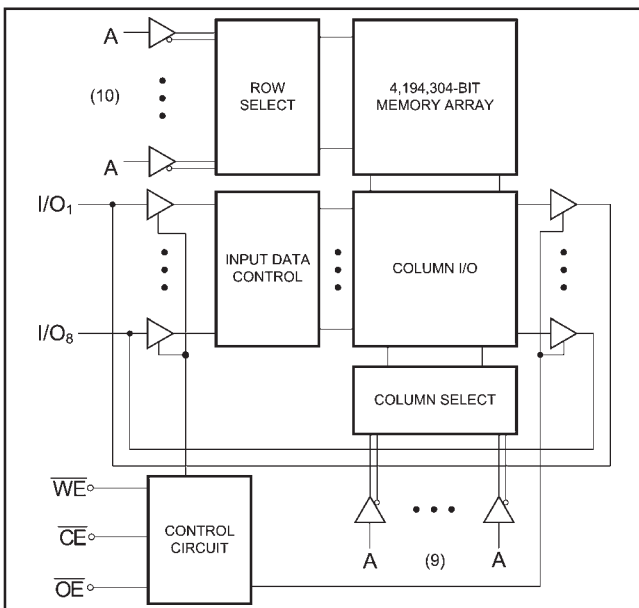
The P4C1048L device provides asynchronous operation with matching access and cycle times. Memory

locations are specified on address pins A_0 to A_{18} . Reading is accomplished by device selection (\overline{CE} low) and output enabling (\overline{OE}) while write enable (\overline{WE}) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either \overline{CE} is HIGH or \overline{WE} is LOW.

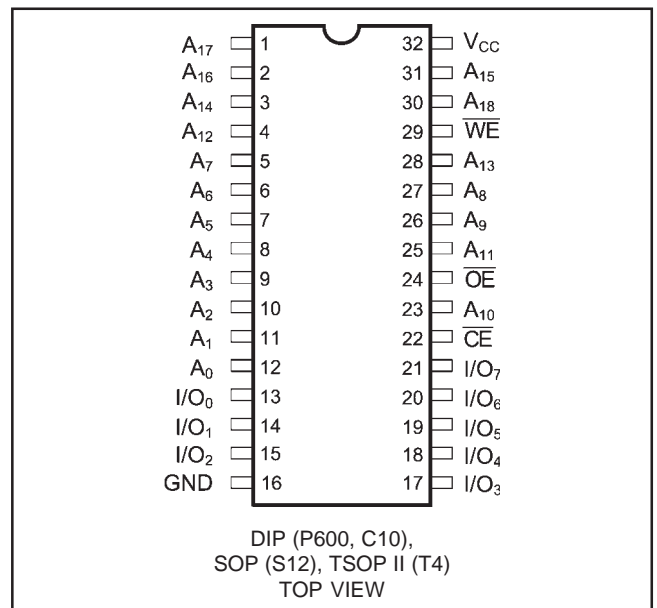
The P4C1048L is packaged in a 32-pin 445 mil plastic SOP, 32-pin TSOP II, or 600 mil plastic or ceramic side-braced DIP.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

| Temperature Range (Ambient) | Supply Voltage |
|-----------------------------|------------------------------|
| Commercial (0°C to 70°C) | $4.5V \leq V_{CC} \leq 5.5V$ |
| Industrial (-40°C to 85°C) | $4.5V \leq V_{CC} \leq 5.5V$ |
| Military (-55°C to 125°C) | $4.5V \leq V_{CC} \leq 5.5V$ |

MAXIMUM RATINGS^(a)

Stresses greater than those listed can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Maximum Ratings for extended periods can adversely affect device reliability.

| Symbol | Parameter | Min | Max | Unit |
|------------|---|------|----------------|------|
| V_{CC} | Supply Voltage with Respect to GND | -0.5 | 7.0 | V |
| V_{TERM} | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 | $V_{CC} + 0.5$ | V |
| T_A | Operating Ambient Temperature | -55 | 125 | °C |
| S_{TG} | Storage Temperature | -65 | 150 | °C |
| I_{OUT} | Output Current into Low Outputs | | 25 | mA |
| I_{LAT} | Latch-up Current | >200 | | mA |

CAPACITANCES^(d)

($V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1.0$ MHz)

| Symbol | Parameter | Test Conditions | Max | Unit |
|-----------|--------------------|-----------------|-----|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 6 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | 8 | pF |

POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | * | | | | Unit |
|----------|---------------------------|-------------------|-----|-----|-----|------|------|
| | | | -45 | -55 | -70 | -100 | |
| I_{CC} | Dynamic Operating Current | Commercial | 20 | 20 | 20 | 20 | mA |
| | | Industrial | 25 | 25 | 25 | 25 | |
| | | Military | 35 | 35 | 35 | 35 | |

*Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate.

The device is continuously enabled for writing, i.e. \overline{CE} and $\overline{WE} \leq V_{IL}$ (max), \overline{OE} is high. Switching inputs are 0V and 3V.

Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS(Over Recommended Operating Temperature & Supply Voltage)^(b)

| Symbol | Parameter | Test Conditions | P4C1048L | | Unit | |
|-----------|--|---|---------------------|----------------|------|---------------|
| | | | Min | Max | | |
| V_{IH} | Input High Voltage | | 2.2 | $V_{CC} + 0.5$ | V | |
| V_{IL} | Input Low Voltage | | -0.5 ^(c) | 0.8 | V | |
| V_{HC} | CMOS Input High Voltage | | $V_{CC} - 0.2$ | $V_{CC} + 0.5$ | V | |
| V_{LC} | CMOS Input Low Voltage | | -0.5 ^(c) | 0.2 | V | |
| V_{OL} | Output Low Voltage (TTL Load) | $I_{OL} = +2.1 \text{ mA}$, $V_{CC} = \text{Min.}$ | | 0.4 | V | |
| V_{OH} | Output High Voltage (TTL Load) | $I_{OH} = -1 \text{ mA}$, $V_{CC} = \text{Min.}$ | 2.4 | | V | |
| I_{LI} | Input Leakage Current | $V_{CC} = \text{Max.}$ $V_{IN} = \text{GND to } V_{CC}$ | Mil. | -10 | +10 | μA |
| | | | Ind./Com'l. | -5 | +5 | |
| I_{LO} | Output Leakage Current | $V_{CC} = \text{Max.}$, $\overline{CE} = V_{IH}$, $V_{OUT} = \text{GND to } V_{CC}$ | Mil. | -10 | +10 | μA |
| | | | Ind./Com'l. | -5 | +5 | |
| I_{SB} | Standby Power Supply Current (TTL Input Levels) | $\overline{CE} \geq V_{IH}$ $V_{CC} = \text{Max.}$, $f = \text{Max.}$, Outputs Open | Mil. | — | 5 | mA |
| | | | Ind./Com'l. | — | 3 | |
| I_{SB1} | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE} \geq V_{HC}$ $V_{CC} = \text{Max.}$, $f = 0$, Outputs Open $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | Mil. | — | 100 | μA |
| | | | Ind./Com'l. | — | 30 | |

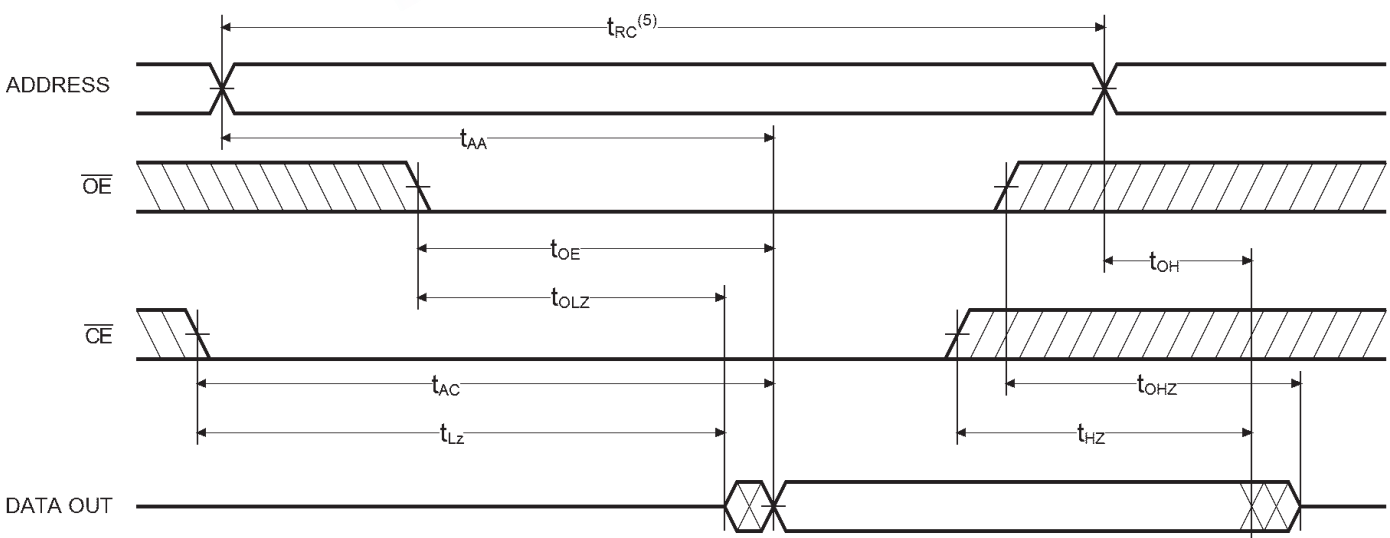
N/A = Not Applicable

AC ELECTRICAL CHARACTERISTICS - READ CYCLE

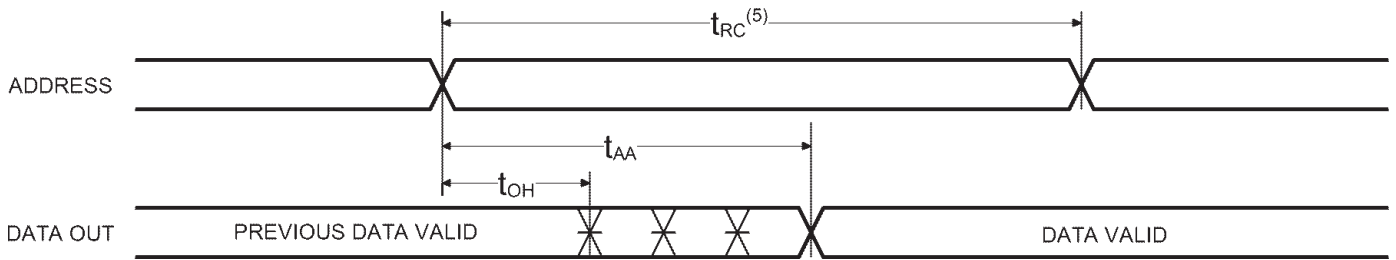
(Over Recommended Operating Temperature & Supply Voltage)

| Symbol | Parameter | -45 | | -55 | | -70 | | -100 | | Unit |
|-----------|----------------------------------|-----|-----|-----|-----|-----|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{RC} | Read Cycle Time | 45 | | 55 | | 70 | | 100 | | ns |
| t_{AA} | Address Access Time | | 45 | | 55 | | 70 | | 100 | ns |
| t_{AC} | Chip Enable Access Time | | 45 | | 55 | | 70 | | 100 | ns |
| t_{OH} | Output Hold from Address Change | 5 | | 5 | | 5 | | 5 | | ns |
| t_{LZ} | Chip Enable to Output in Low Z | 10 | | 10 | | 10 | | 10 | | ns |
| t_{HZ} | Chip Disable to Output in High Z | | 18 | | 20 | | 25 | | 35 | ns |
| t_{OE} | Output Enable Low to Data Valid | | 22 | | 25 | | 35 | | 45 | ns |
| t_{OLZ} | Output Enable Low to Low Z | 5 | | 5 | | 5 | | 5 | | ns |
| t_{OHZ} | Output Enable High to High Z | | 18 | | 20 | | 25 | | 35 | ns |
| t_{PU} | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | ns |
| t_{PD} | Chip Disable to Power Down Time | | 45 | | 55 | | 70 | | 100 | ns |

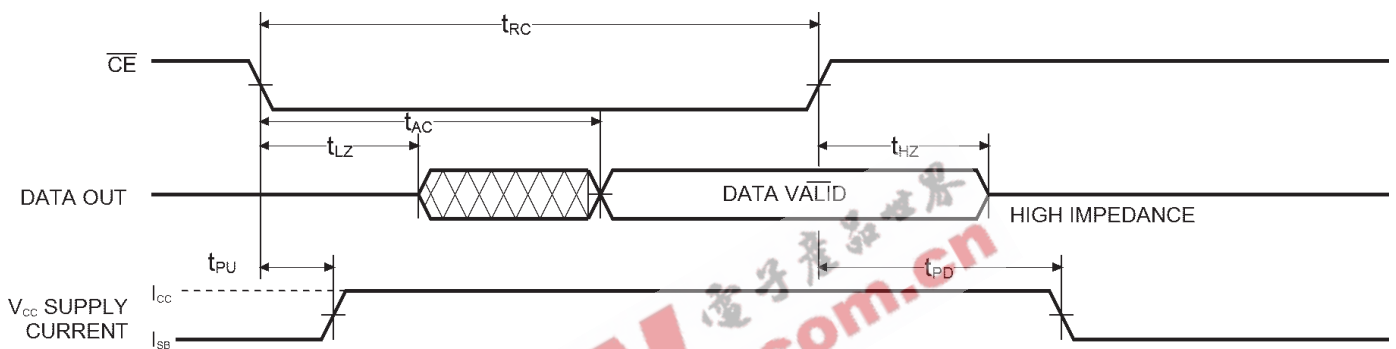
READ CYCLE NO. 1 (\overline{OE} CONTROLLED)⁽¹⁾



READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 (\overline{CE} CONTROLLED)



Notes:

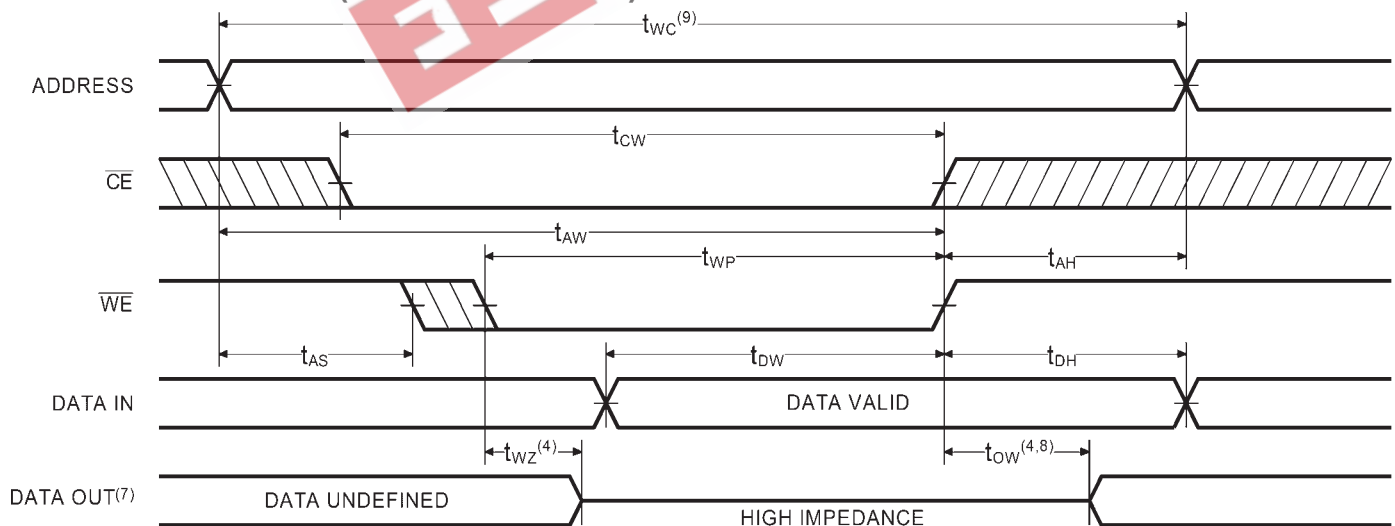
1. \overline{WE} is HIGH for READ cycle.
2. \overline{CE} and \overline{OE} are LOW for READ cycle.
3. ADDRESS must be valid prior to, or coincident with later of \overline{CE} transition LOW.
4. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS - WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

| Symbol | Parameter | -45 | | -55 | | -70 | | -100 | | Unit |
|----------|----------------------------------|-----|-----|-----|-----|-----|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{WC} | Write Cycle Time | 45 | | 55 | | 70 | | 100 | | ns |
| t_{CW} | Chip Enable Time to End of Write | 35 | | 40 | | 60 | | 75 | | ns |
| t_{AW} | Address Valid to End of Write | 35 | | 40 | | 60 | | 75 | | ns |
| t_{AS} | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WP} | Write Pulse Width | 35 | | 40 | | 50 | | 60 | | ns |
| t_{AH} | Address Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| t_{DW} | Data Valid to End of Write | 25 | | 30 | | 35 | | 45 | | ns |
| t_{DH} | Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WZ} | Write Enable to Output in High Z | | 18 | | 20 | | 25 | | 35 | ns |
| t_{OW} | Output Active from End of Write | 5 | | 5 | | 5 | | 5 | | ns |

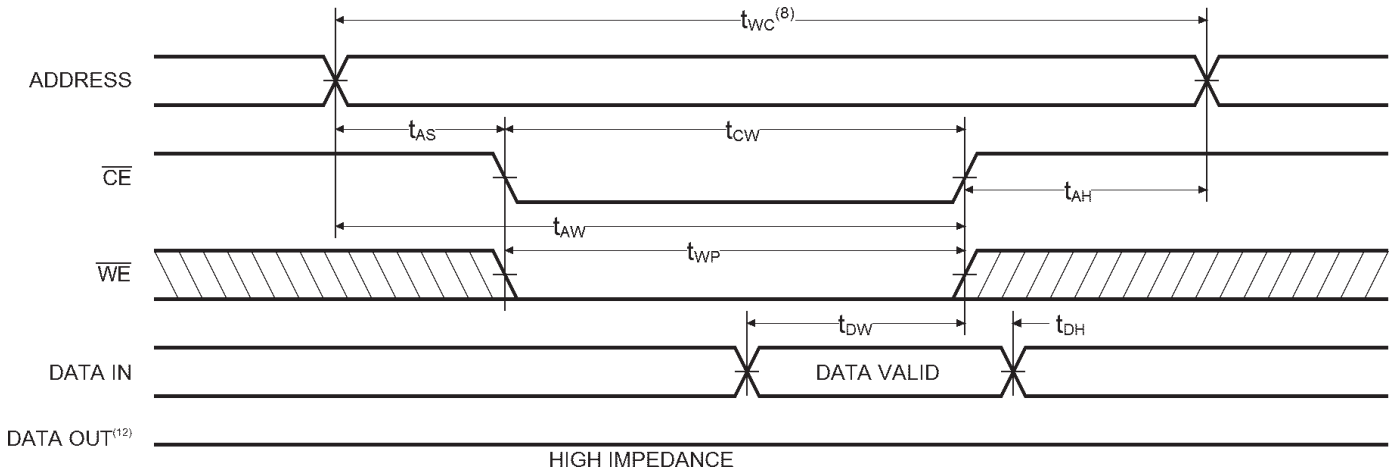
WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)^(6,7)



Notes:

- 6. \overline{CE} and \overline{WE} are LOW for WRITE cycle.
- 7. \overline{OE} is LOW for this WRITE cycle to show t_{WZ} and t_{OW} .
- 8. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.
- 9. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO.2 (\overline{CE} CONTROLLED)⁽⁶⁾



AC TEST CONDITIONS

| | |
|-------------------------------|------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Fig. 1 and 2 |

TRUTH TABLE

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | I/O | Power |
|--------------------|-----------------|-----------------|-----------------|-----------|---------|
| Standby | H | X | X | High Z | Standby |
| D_{OUT} Disabled | L | H | H | High Z | Active |
| Read | L | L | H | D_{OUT} | Active |
| Write | L | X | L | D_{IN} | Active |

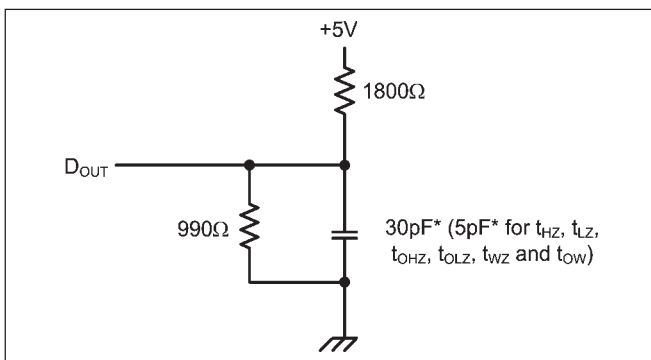


Figure 1. Output Load

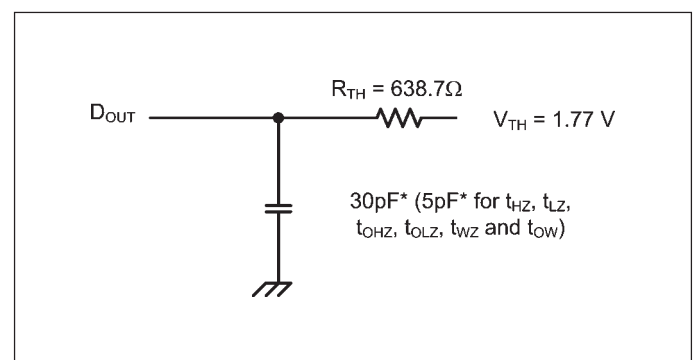


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:

Because of the high speed of the P4C1048L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor is also required between V_{CC} and ground.

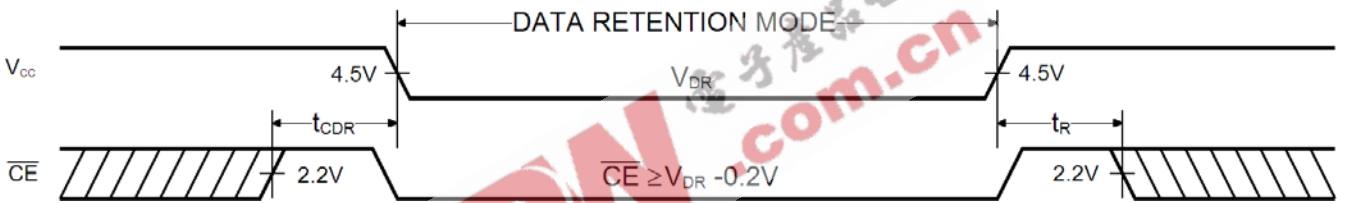
To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.77V (Thevenin Voltage) at the comparator input, and a 589 Ω resistor must be used in series with D_{OUT} to match 639 Ω (Thevenin Resistance).

DATA RETENTION

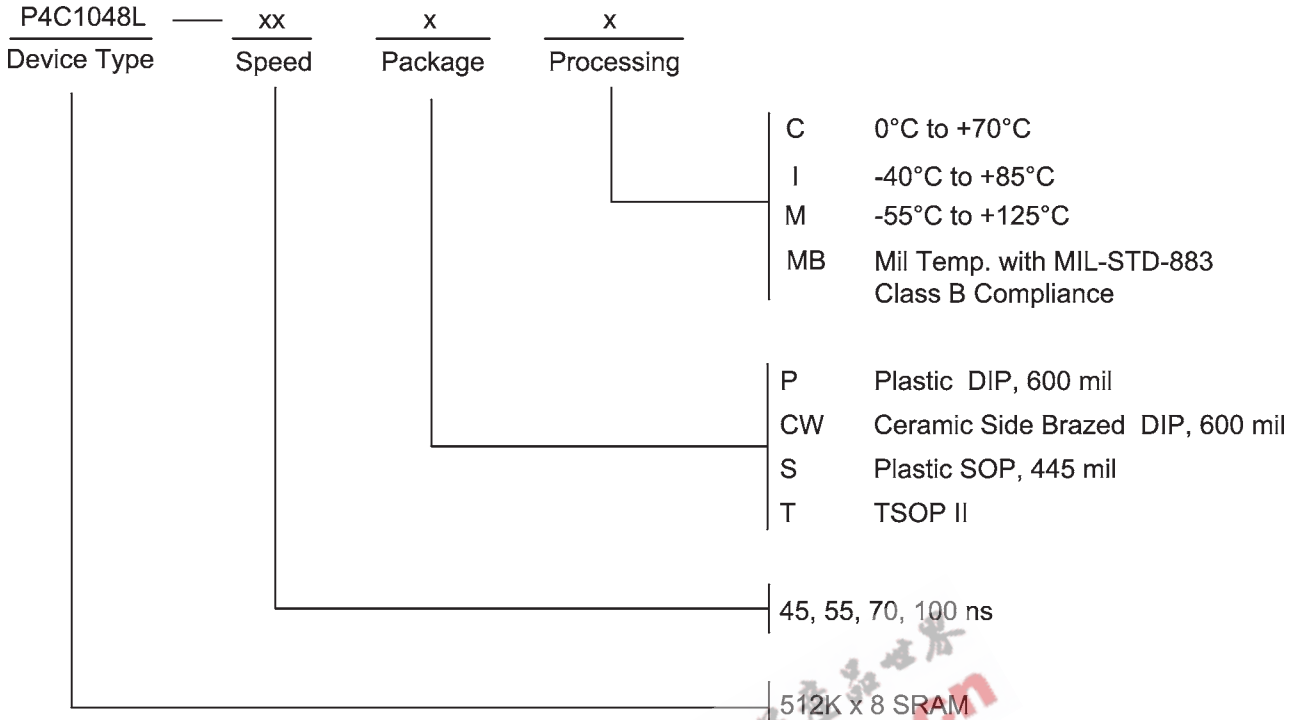
| Symbol | Parameter | Test Conditions | Min | Max | Unit |
|------------|--------------------------------------|---|----------|-----|---------|
| V_{DR} | V_{CC} for Data Retention | $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | 2.0 | 5.5 | V |
| I_{CCDR} | Data Retention Current | $V_{DR} = 2.0V$ | Comm/Ind | 20 | μA |
| | | | Military | 200 | |
| | | $V_{DR} = 3.0V$ | Comm/Ind | 30 | μA |
| | | | Military | 300 | |
| t_{CDR} | Chip Deselect to Data Retention Time | See Retention Waveform | 0 | | ns |
| t_R | Operating Recovery Time | | t_{RC} | | ns |

1. $\overline{CE}_1 \geq V_{DR} - 0.2V$, $CE_2 \geq V_{DR} - 0.2V$ or $CE_2 \leq 0.2V$; or $\overline{CE}_1 \leq 0.2V$, $CE_2 - 0.2V$; $V_{IN} \geq V_{DR} - 0.2V$ or $V_{IN} \leq 0.2V$

LOW V_{CC} DATA RETENTION WAVEFORM



ORDERING INFORMATION



SELECTION GUIDE

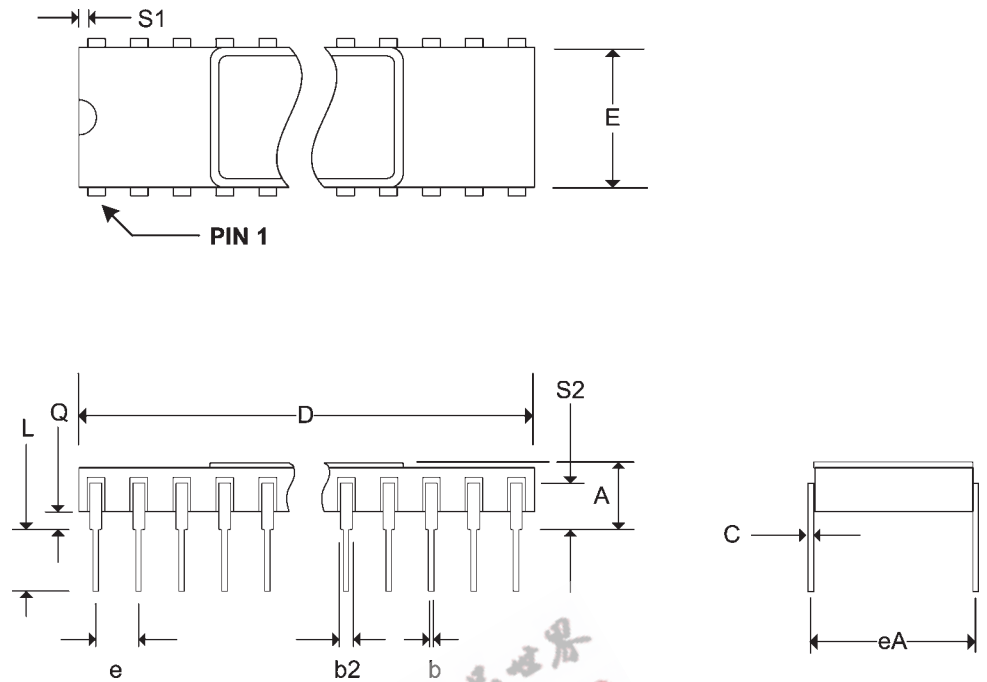
The P4C1048L is available in the following temperature, speed and package options.

| Temperature Range | Package | Speed (ns) | | | |
|---------------------|---------------------------|------------|--------|---------|----------|
| | | 45 | 55 | 70 | 100 |
| Commercial | Plastic DIP (600 mil) | -45PC | -55PC | -70PC | -100PC |
| | Side Brazed DIP (600 mil) | -45CWC | -55CWC | -70CWC | -100CWC |
| | Plastic SOP (445 mil) | -45SC | -55SC | -70SC | -100SC |
| | TSOP II | -45TC | -55TC | -70TC | -100TC |
| Industrial | Plastic DIP (600 mil) | -45PI | -55PI | -70PI | -100PI |
| | Side Brazed DIP (600 mil) | -45CWI | -55CWI | -70CWI | -100CWI |
| | Plastic SOP (445 mil) | -45SI | -55SI | -70SI | -100SI |
| | TSOP II | -45TI | -55TI | -70TI | -100TI |
| Military | Side Brazed DIP (600 mil) | N/A | N/A | -70CWM | -100CWM |
| Military Processed* | Side Brazed DIP (600 mil) | N/A | N/A | -70CWMB | -100CWMB |

* Military temperature range with MIL-STD-883 Class B processing.

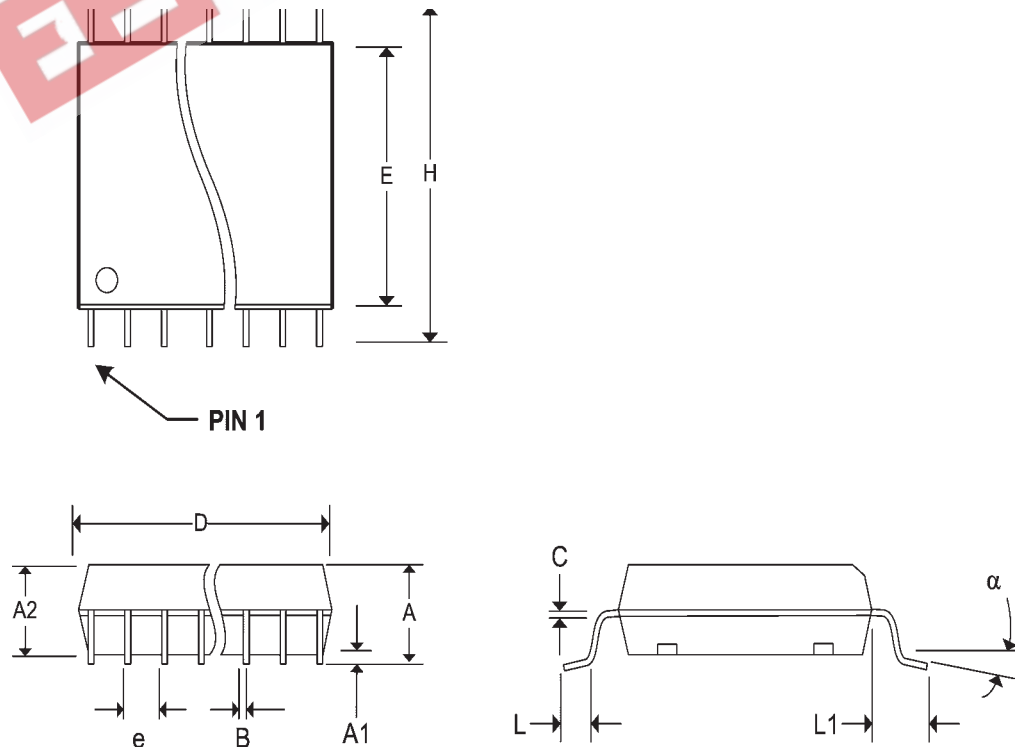
| Pkg # | C10 | |
|--------|--------------|-------|
| # Pins | 32 (600 mil) | |
| Symbol | Min | Max |
| A | - | 0.225 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 1.680 |
| E | 0.510 | 0.620 |
| eA | 0.600 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.070 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

SIDEBRAZED DUAL IN-LINE PACKAGE



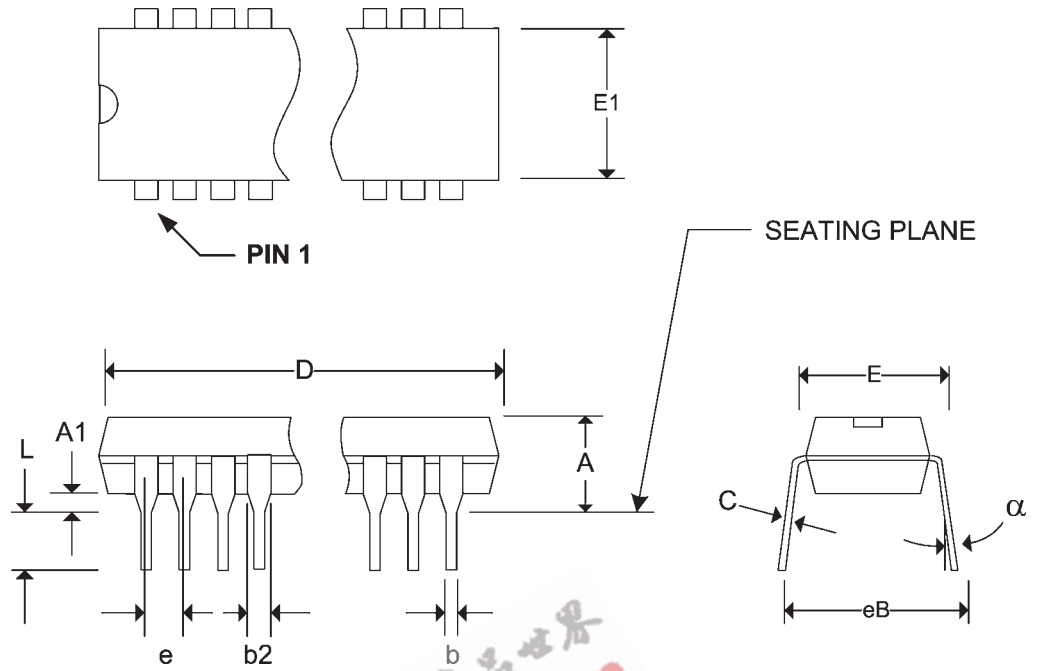
| Pkg # | S12 | |
|----------|--------------|-------|
| # Pins | 32 (445 Mil) | |
| Symbol | Min | Max |
| A | - | 0.118 |
| A1 | 0.004 | - |
| A2 | 0.101 | 0.111 |
| B | 0.014 | 0.020 |
| C | 0.006 | 0.012 |
| D | 0.793 | 0.817 |
| e | 0.050 BSC | |
| E | 0.440 | 0.450 |
| H | 0.546 | 0.566 |
| L | 0.023 | 0.039 |
| L1 | 0.047 | 0.063 |
| α | 0° | 4° |

SOIC/SOP SMALL OUTLINE IC PACKAGES



| | | |
|----------|--------------|------------|
| Pkg # | P600 | |
| # Pins | 32 (600 mil) | |
| Symbol | Min | Max |
| A | 0.160 | 0.200 |
| A1 | 0.015 | - |
| b | 0.014 | 0.023 |
| b2 | 0.045 | 0.070 |
| C | 0.006 | 0.014 |
| D | 1.600 | 1.700 |
| E1 | 0.526 | 0.548 |
| E | 0.590 | 0.610 |
| e | 0.100 BSC | |
| eB | 0.600 BSC | |
| L | 0.120 | 0.150 |
| α | 0° | 15° |

PLASTIC DUAL IN-LINE PACKAGE



| | | |
|----------------|------------|------------|
| Pkg # | T4 | |
| # Pins | 32 | |
| Symbol | Min | Max |
| A | 0.037 | 0.041 |
| A ₂ | - | 0.047 |
| b | 0.012 | 0.020 |
| D | 0.395 | 0.405 |
| E | 0.820 | 0.831 |
| e | 0.050 BSC | |
| H _D | 0.455 | 0.471 |

TSOP II PACKAGE

