P4C1048L LOW POWER 512K x 8 CMOS STATIC RAM

FEATURES

- V_{cc} Current
 Operating: 35mA
 CMOS Standby: 100µA
- Access Times —45/55/70/100 ns
- Single 5 Volts ±10% Power Supply
- Easy Memory Expansion Using CE and OE Inputs

- Common Data I/O
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Automatic Power Down
 - Packages —32-Pin 600 mil Plastic and Ceramic DIP —32-Pin 445 mil SOP
 - -32-Pin TSOP II

DESCRIPTION

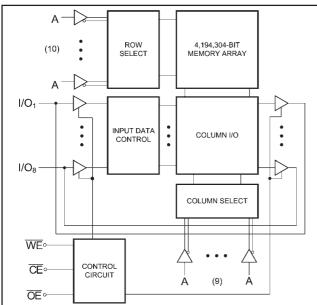
The P4C1048L is a 4 Megabit low power CMOS static RAM organized as $512K \times 8$. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single $5V\pm10\%$ tolerance power supply.

Access times as fast as 45 ns are availale. CMOS is utilized to reduce power consumption to a low level.

The P4C1048L device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{18} . Reading is accomplished by device selection (\overline{CE} low) and output enabling (\overline{OE}) while write enable (\overline{WE}) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either \overline{CE} is HIGH or WE is LOW.

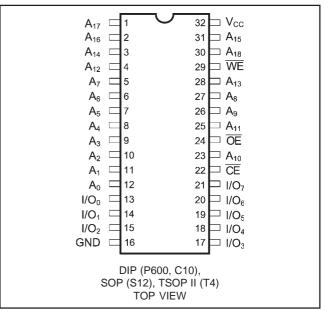
The P4C1048L is packaged in a 32-pin 445 mil plastic SOP, 32-pin TSOP II, or 600 mil plastic or ceramic sidebrazed DIP.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION



Document # SRAM129 REV D

P4C1048L

RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

Temperature Range (Ambient)	Supply Voltage
Commercial (0°C to 70°C)	$4.5V \le V_{cc} \le 5.5V$
Industrial (-40°C to 85°C)	$4.5V \le V_{cc} \le 5.5V$
Military (-55°C to 125°C)	$4.5V \le V_{\rm CC} \le 5.5V$

MAXIMUM RATINGS^(a)

Stresses greater than those listed can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Maximum Ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Мах	Unit
V _{cc}	Supply Voltage with Respect to GND	-0.5	7.0	V
V	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5	V _{cc} + 0.5	V
T _A	Operating Ambient Temperature	-55	125	°C
S _{TG}	Storage Temperature	-65	150	°C
I _{OUT}	Output Current into Low Outputs	32 -5	25	mA
I _{LAT}	Latch-up Current	>200		mA

CAPACITANCES^(d)

 $(V_{cc} = 5.0V, T_{A} = 25^{\circ}C, f = 1.0 \text{ MHz})$

Symbol	Parameter	Test Conditions	Мах	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	pF

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	er Temperature Range		-55	-70	-100	Unit
	I _{cc} Dynamic Operating Current	Commercial	20	20	20	20	
I _{cc}		Industrial	25	25	25	25	mA
		Military	35	35	35	35	

*Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e. \overline{CE} and $\overline{WE} \le V_{IL}$ (max), \overline{OE} is high. Switching inputs are 0V and 3V.

Notes:

b. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.

c. Transient inputs with $V_{_{\rm I\!L}}$ and $I_{_{\rm I\!L}}$ not more negative than –3.0V and

-100mA, respectively, are permissible for pulse widths up to 20 ns.

d. This parameter is sampled and not 100% tested.

a. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)^(b)

Symbol	Parameter	Test Conditions	P4C	P4C1048L	
Cymbol	i arameter		Min	Max	Unit
$V_{\rm IH}$	Input High Voltage		2.2	V_{cc} +0.5	V
V _{IL}	Input Low Voltage		-0.5 ^(c)	0.8	V
$V_{\rm HC}$	CMOS Input High Voltage		V _{cc} –0.2	V_{cc} +0.5	V
V _{LC}	CMOS Input Low Voltage		-0.5 ^(c)	0.2	V
V _{OL}	Output Low Voltage (TTL Load)	$I_{oL} = +2.1 \text{ mA}, V_{CC} = \text{Min.}$		0.4	V
V _{OH}	Output High Voltage (TTL Load)	$I_{OH} = -1 \text{ mA}, V_{CC} = \text{Min.}$	2.4		V
		V _{cc} = Max. M	I. –10	+10	μA
Ι _{LI}	Input Leakage Current	$V_{IN} = GND \text{ to } V_{CC}$ Ind./Com		+5	
		V _{cc} = Max., M	il. –10	+10	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{H}$, $old lind./Com$	'I. —5	+5	
		$V_{out} = GND$ to V_{cc}			
		CE≥V _{III} Mi	I. —	5	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	V _{cc} = Max, Ind./Com	I. —	3	
		$V_{cc} = Max., M$ $\overline{CE} = V_{IH}, Ind./Com$ $V_{out} = GND \text{ to } V_{cc}$ $\overline{CE} \ge V_{IH} $ $V_{cc} = Max, $ $f = Max., Outputs Open$ $\overline{CE} \ge V_{HC} $ Mi $V_{cc} = Max, Ind./Com'$			
		CE≥V., Mi		100	μA
	Standby Power Supply	V _{cc} = Max, Ind./Com'	I.	30	Perri
I _{SB1}	Current (CMOS Input Levels)	f = 0, Outputs Open			
		$V_{\rm IN} \leq V_{\rm LC}$ or $V_{\rm IN} \geq V_{\rm HC}$			

N/A = Not Applicable

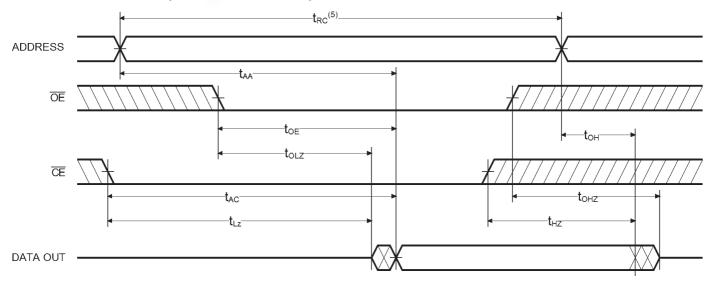


AC ELECTRICAL CHARACTERISTICS - READ CYCLE

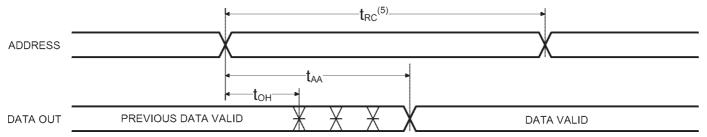
(Over Recommended Operating Temperature & Supply Voltage)

0		-4	45	-{	55	-70		-1	00	11	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit	
t _{RC}	Read Cycle Time	45		55		70		100		ns	
t _{AA}	Address Access Time		45		55		70		100	ns	
t _{AC}	Chip Enable Access Time		45		55		70		100	ns	
t _{он}	Output Hold from Address Change	5		5		5		5		ns	
t _{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns	
t _{HZ}	Chip Disable to Output in High Z		18		20		25		35	ns	
t _{oe}	Output Enable Low to Data Valid		22		25		35		45	ns	
t _{oLZ}	Output Enable Low to Low Z	5		5	Be	5	cr	5		ns	
t _{oHZ}	Output Enable High to High Z		18		20	on	25		35	ns	
t _{PU}	Chip Enable to Power Up Time	0		0		0		0		ns	
t _{PD}	Chip Disable to Power Down Time		45		55		70		100	ns	

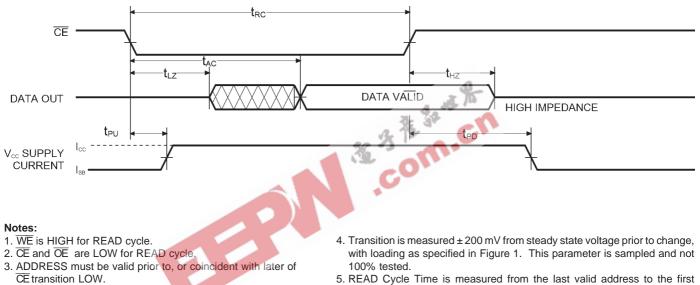
READ CYCLE NO. 1 (OE CONTROLLED)⁽¹⁾



READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 (CECONTROLLED)



5. READ Cycle Time is measured from the last valid address to the first transitioning address.

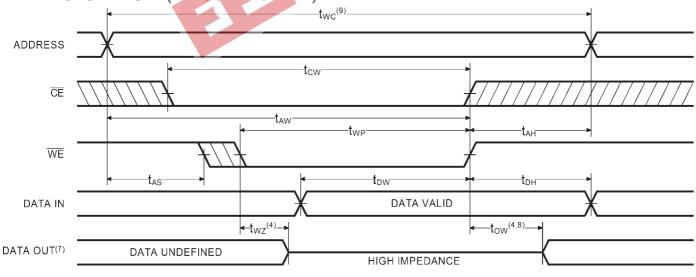


AC CHARACTERISTICS - WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

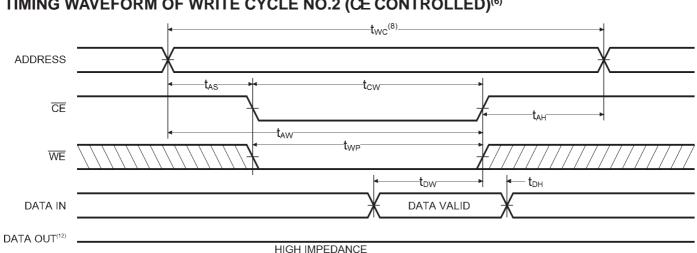
Cumhal	Devementer	-4	45		55	-7	'0	-1	00	Unit
Symbol	Parameter	Min	Max	Min	Max	Min	Мах	Min	Мах	Unit
t _{wc}	Write Cycle Time	45		55		70		100		ns
t _{cw}	Chip Enable Time to End of Write	35		40		60		75		ns
t _{AW}	Address Valid to End of Write	35		40		60		75		ns
t _{AS}	Address Set-up Time	0		0		0		0		ns
t _{wP}	Write Pulse Width	35		40		50		60		ns
t _{AH}	Address Hold Time	0		0		0		0		ns
t _{DW}	Data Valid to End of Write	25		30		35	A	45		ns
t _{DH}	Data Hold Time	0		0		0	75	0		ns
t _{wz}	Write Enable to Output in High Z		18		20	5.34	25		35	ns
t _{ow}	Output Active from End of Write	5		5	C	5		5		ns

WRITE CYCLE NO. 1 (WE CONTROLLED)^(6,7)



Notes:

- 6. \overline{CE} and \overline{WE} are LOW for WRITE cycle.
- OE is LOW for this WRITE cycle to show t_{wz} and t_{ow}.
 If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.
- 9. Write Cycle Time is measured from the last valid address to the first transitioning address.



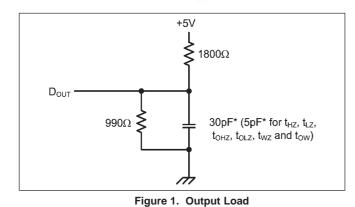
TIMING WAVEFORM OF WRITE CYCLE NO.2 (CE CONTROLLED)⁽⁶⁾

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Fig. 1 and 2

- 8-
3, 35, 14
A REAL COL
TRUTH TABLE

h	Mode	Œ	ŌĒ	WE	I/O	Power
ł.	Standby	Н	Х	Х	High Z	Standby
	D _{out} Disabled	L	н	Н	High Z	Active
	Read	L	L	Н	D _{OUT}	Active
	Write	L	Х	L	D _{IN}	Active



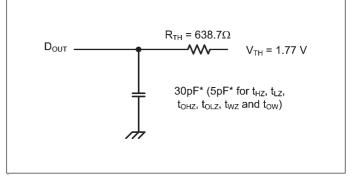


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:

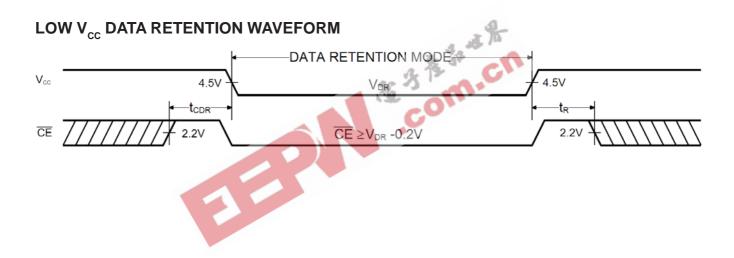
Because of the high speed of the P4C1048L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V $_{cc}$ and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V_{cc} and ground.

To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.77 V (Thevenin Voltage) at the comparator input, and a 589Ω resistor must be used in series with ${\rm D}_{_{\rm OUT}}$ to match 639 Ω (Thevenin Resistance).

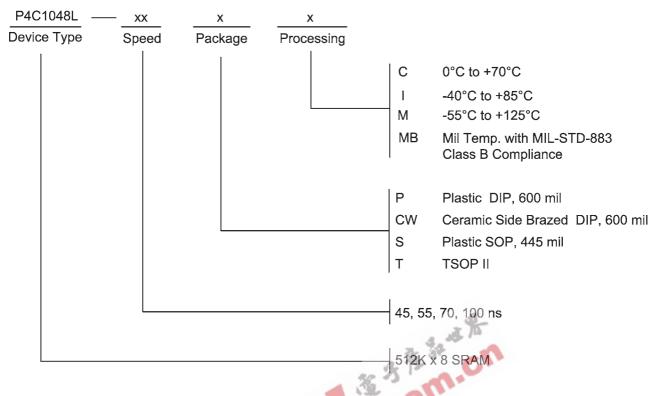
P4C1048L

DATA RETENTION

Symbol	Parameter	Test Conditio	ns	Min	Мах	Unit
V _{DR}	$V_{\rm cc}$ for Data Retention	$\overline{CE} \ge V_{cc} - 0.2V,$ $V_{iN} \ge V_{cc} - 0.2V \text{ or } V$	2.0	5.5	V	
		(1 - 2)	Comm/Ind		20	
	Data Datastica Consent	V _{DR} = 2.0V	Military		200	μA
CCDR	Data Retention Current	<u>)</u> (2.0)/	Comm/Ind		30	
		V _{DR} = 3.0V Military			300	μA
t _{CDR}	Chip Deselect to Data Retention Time	See Retention Way	0		ns	
t _R	Operating Recovery Time			t _{RC}		ns



ORDERING INFORMATION



SELECTION GUIDE

The P4C1048L is available in the following temperature, speed and package options.

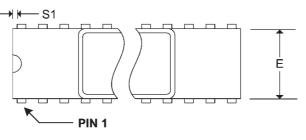
Temperature	Package	Speed (ns)						
Range	Package	45	55	70	100			
Commercial	Plastic DIP (600 mil)	-45PC	-55PC	-70PC	-100PC			
	Side Brazed DIP (600 mil)	-45CWC	-55CWC	-70CWC	-100CWC			
	Plastic SOP (445 mil)	-45SC	-55SC	-70SC	-100SC			
	TSOP II	-45TC	-55TC	-70TC	-100TC			
Industrial	Plastic DIP (600 mil)	-45PI	-55PI	-70PI	-100PI			
	Side Brazed DIP (600 mil)	-45CWI	-55CWI	-70CWI	-100CWI			
	Plastic SOP (445 mil)	-45SI	-55SI	-70SI	-100SI			
	TSOP II	-45TI	-55TI	-70TI	-100TI			
Military	Side Brazed DIP (600 mil)	N/A	N/A	-70CWM	-100CWM			
Military Processed*	Side Brazed DIP (600 mil)	N/A	N/A	-70CWMB	-100CWMB			

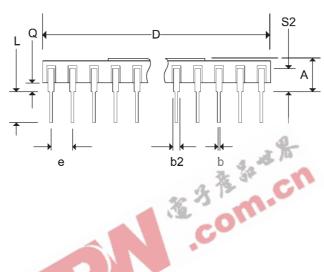
* Military temperature range with MIL-STD-883 Class B processing.

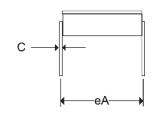


C10 Pkg # # Pins 32 (600 mil) Symbol Min Max А 0.225 b 0.014 0.026 b2 0.045 0.065 С 0.008 0.018 D 1.680 -Е 0.510 0.620 0.600 BSC eA 0.100 BSC е 0.125 0.200 L Q 0.015 0.070 S1 0.005 -S2 0.005 _

SIDEBRAZED DUAL IN-LINE PACKAGE

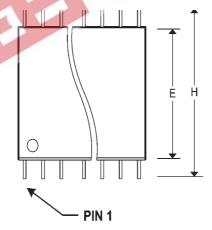


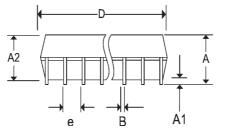


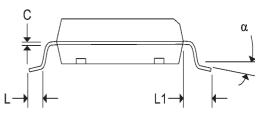


Pkg #	S12	
# Pins	32 (445 Mil)	
Symbol	Min	Max
А	-	0.118
A1	0.004	-
A2	0.101	0.111
В	0.014	0.020
С	0.006	0.012
D	0.793	0.817
е	0.050 BSC	
E	0.440	0.450
Н	0.546	0.566
L	0.023	0.039
L1	0.047	0.063
α	0°	4°

SOIC/SOP SMALL OUTLINE IC PACKAGES







Pkg #	P600	
# Pins	32 (600 mil)	
Symbol	Min	Max
А	0.160	0.200
A1	0.015	-
b	0.014	0.023
b2	0.045	0.070
С	0.006	0.014
D	1.600	1.700
E1	0.526	0.548
Е	0.590	0.610
е	0.100 BSC	
eB	0.600 BSC	
L	0.120	0.150
α	0°	15°

Pkg #

Pins

Symbol

A

 A_2

b D

Е

е

 H_{D}

Τ4

32

0.050 BSC

Max

0.041

0.047

0.020

0.405

0.831

0.471

Min

0.037

-

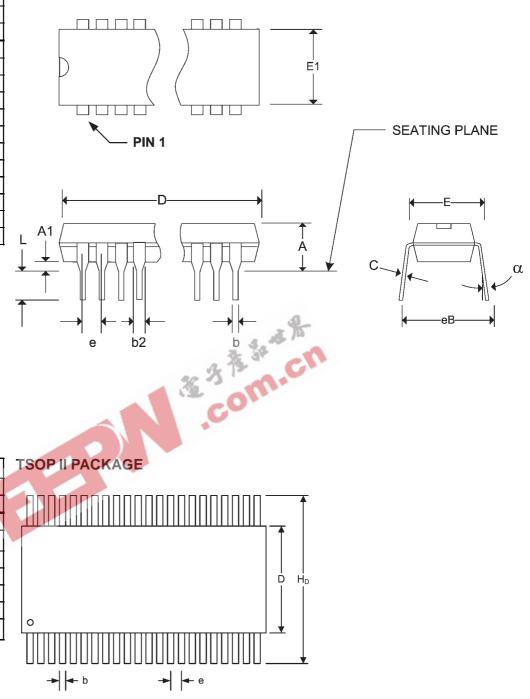
0.012

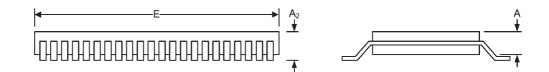
0.395

0.820

0.455

PLASTIC DUAL IN-LINE PACKAGE







REVISIONS

	DCUMENT NUMBER:SRAM129DCUMENT TITLE:P4C1048L LOW POWER 512K x 8 CMOS STATIC RAM			
REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE	
OR	Oct-05	JDB	New Data Sheet	
A	Nov-06	JDB	Minor corrections to DC Electrical Characteristics and Data Retention tables	
В	Dec-06	JDB	Update SOIC/SOP package drawing.	
С	May-07	JDB	Added 45/55 ns and PDIP	
D	Jul-07	JDB	Corrected error in selection guide; added TSOP II package	
			A Contraction of the second seco	
			A TE CO	
			com.cn	