SRAM

256K X 8 LOW POWER CMOS STATIC RAM

FEATURES

- Low-power consumption
  - Active: 40mA at 55ns
  - Stand-by: 5uA (CMOS input/output)
- 55/70/100 ns access time
- Equal access and cycle time
- Single +2.7V to 3.6V Power Supply
- TTL compatible , Tri-state output
- Common I/O capability
- Automatic power-down when deselected
- Available in 32-pin TSOP-I (8x20mm) , TSOP-I(8x13.4mm) , 48-pin CSP packages

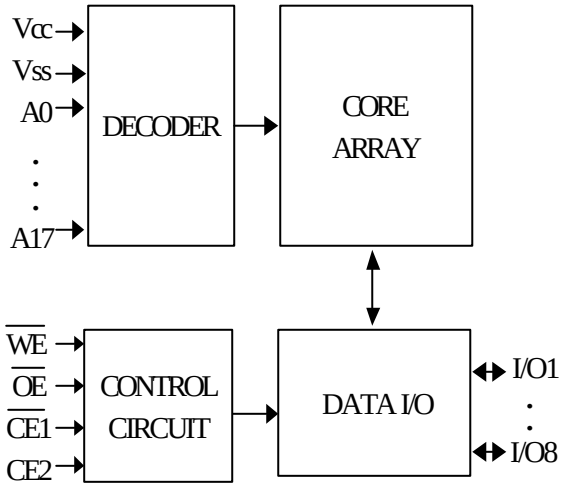
PART NUMBER EXAMPLES

PART NO.	PACKAGE CODE
T15V2M08A-55H	H = TSOP-I(8x20)
T15V2M08A-70P	P= TSOP-I(8x13.4)
T15V2M08A-100C	C = CSP

GENERAL DESCRIPTION

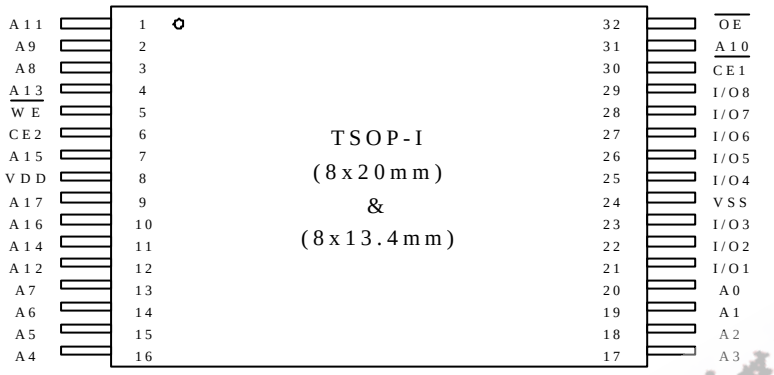
The T15V2M08A is a very Low Power CMOS Static RAM organized as 262,144 words by 8 bits . This device is fabricated by high performance CMOS technology. It can be operated under wide power supply voltage range from +2.7V to +3.6V.

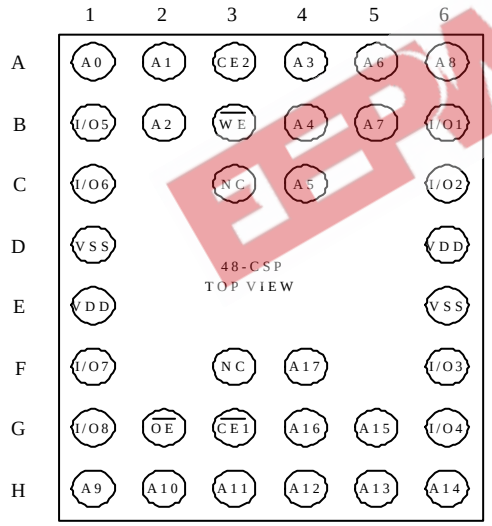
The T15V2M08A inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. Data retention is guaranteed at a power supply voltage as low as 2V.



BLOCK DIAGRAM

PIN CONFIGURATIONS





PIN DESCRIPTIONS

SYMBOL	DESCRIPTIONS		SYMBOL	DESCRIPTIONS
A0 ~ A17	Address inputs		$\overline{OE}$	Output enable input
I/O0~I/O8	Data inputs/outputs		V_{DD}	Power supply
$\overline{CE1}$,CE2	Chip enable		V_{SS}	Ground
$\overline{WE}$	Write enable input		NC	No connection

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYM	MIN.	MAX.	UNIT
Voltage on Any Pin Relative to Gnd	V_R	-0.5	+4.6 V	V
Power Dissipation	P_D	-	0.7	W
Storage Temperature	T_{STG}	-55	+150	°C
Temperature Under Bias	I_{BIAS}	-40	+85	°C

*Note: Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CE}1$	CE2	$\overline{WE}$	$\overline{OE}$	DATA	MODE
H	X	X	X	High-Z	Standby
X	L	X	X	High-Z	Standby
L	H	H	L	Data Out	Active, Read
L	H	H	H	High-Z	Active, Output Disable
L	H	L	X	Data In	Acitve, Write

*Note: X = Don't Care, L = Low, H = High

OPERATING CHARACTERISTICS

(Vcc = 2.7 to 3.6V, Gnd = 0V, Ta = -40°C to 85°C)

PARAMETER	SYM.	TEST CONDITIONS	-55		-70		-100		UNIT
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	Vcc = Max, V_{IN} = Gnd to Vcc	-	1	-	1	-	1	uA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE1}$ = V_{IH} or CE2= V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = Gnd to Vcc	-	1	-	1	-	1	uA
Operating Power Supply Current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2= V_{IH}, $\overline{WE}$ =V_{IH}, $\overline{OE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	-	2	-	2	-	2	mA
Average Operating Current	I_{CC1}	Cycle time=1us, 100% duty, I_{OUT}=0mA, $\overline{CE1}$ ≤ 0.2V, CE2 ≥ V_{CC}-0.2V, V_{IN} ≤ 0.2V	-	3	-	3	-	3	mA
	I_{CC2}	Cycle time=min, 100% duty, I_{OUT}=0mA, $\overline{CE1}$ = V_{IL}, CE2= V_{IH}, V_{IN} = V_{IH} or V_{IL}	-	40	-	35	-	25	mA
Standby Power Supply Current (TTL Level)	I_{SB}	$\overline{CE1}$ = V_{IH} CE2= V_{IL}	-	0.5	-	0.5	-	0.5	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE1}$ ≥ Vcc-0.2V, CE2 ≥ V_{CC}-0.2V or CE2 ≤ 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ Vcc-0.2V	-	5	-	5	-	5	uA
Output Low Voltage	V_{OL}	I_{OL}= 2.0mA	-	0.4	-	0.4	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}= -1.0 mA	2.2	-	2.2	-	2.2	-	V

RECOMMENDED OPERATING CONDITIONS

(Ta = -40°C to 85°C**)

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	2.7	3.0	3.6	V
	Gnd	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.1	-	Vcc+0.3	V
	V_{IL}	-0.3	-	0.6	V

CAPACITANCE

(f = 1 MHz, Ta = 25°C,)

PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/ Output Capacitance	$C_{I/O}$	V_{IN} =V_{OUT}= 0V	8	pF

Note: This parameter is guaranteed by device characterization and is not production tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0.6V to 2.1V
Input Rise and Fall Times	3.0 ns
Input and Output Timing Reference Level	1.4V
Output Load	C_L=30pF+1TTL Load(55ns/70ns)
	C_L=100pF+1TTL Load(Load for 100ns)

AC TEST LOADS AND WAVEFORM

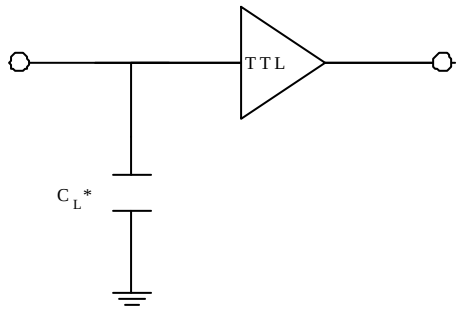


Fig.A * Including Scope and Jig Capacitance

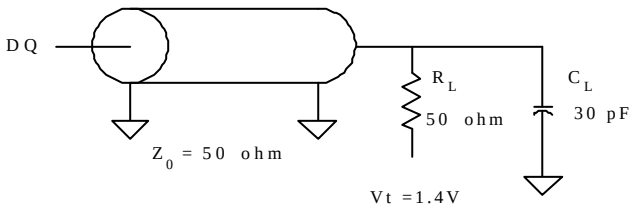


Fig.B Output Load Equivalent

AC CHARACTERISTICS(V_{CC}=2.7 to 3.6V, Gnd = 0V, Ta = -40°C to 85°C)

(1) READ CYCLE

PARAMETER	SYM.	-55		-70		-100		UNIT
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
Chip Enable to Output in Low-Z	t_{LZ}	10	-	10	-	10	-	ns
Chip Disable to Output in High-Z	t_{HZ}	-	20	-	25	-	30	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	-	5	-	5	-	ns
Output Disable to Output in High-Z	t_{OHZ}	-	20	-	25	-	30	ns

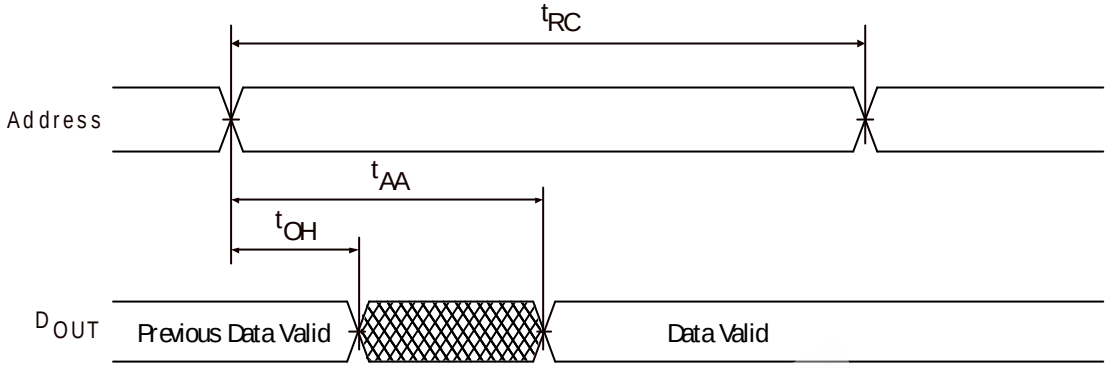
(2)WRITE CYCLE

PARAMETER	SYM.	-55		-70		-100		UNIT
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Chip Enable to Write End	t_{CW}	50	-	60	-	80	-	ns
Address Valid to Write End	t_{AW}	50	-	60	-	80	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	50	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data Valid to Write End	t_{DW}	25	-	30	-	40	-	ns
Data Hold Time	t_{DH}	0	-	0	-	0	-	ns
Write Enable to Output in High-Z	t_{WHZ}	-	25	-	25	-	30	ns
Output Active from Write End	t_{OW}	5	-	5	-	5	-	ns

TIMING WAVEFORMS

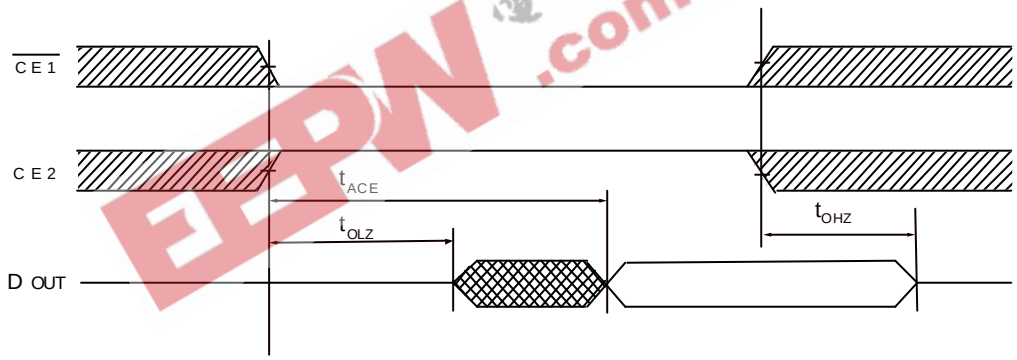
READ CYCLE 1

(Address Controlled)



READ CYCLE 2

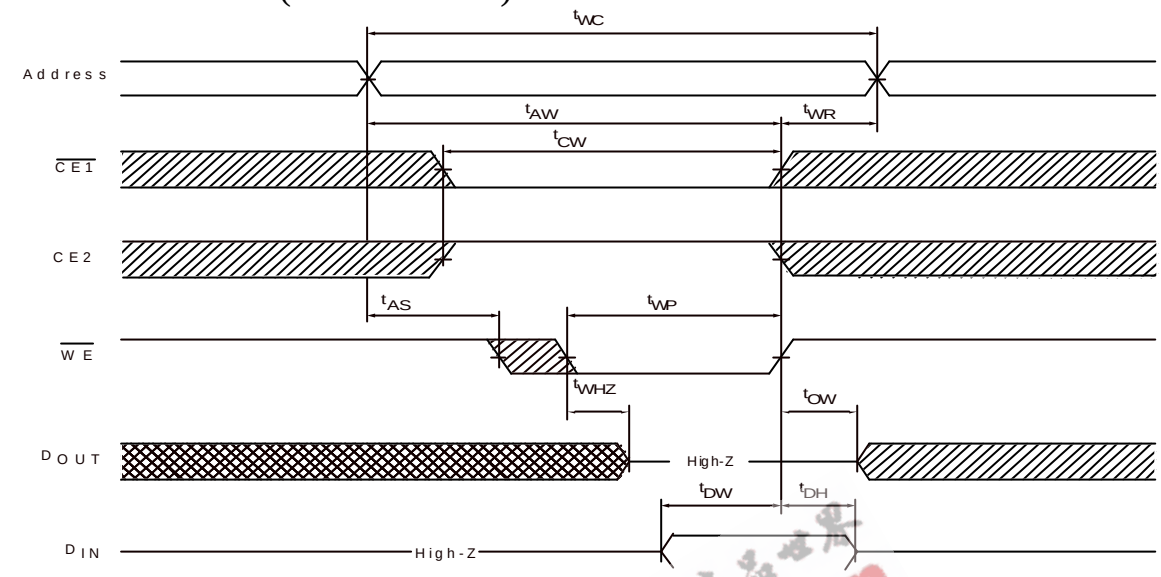
(Chip Enable Controlled)



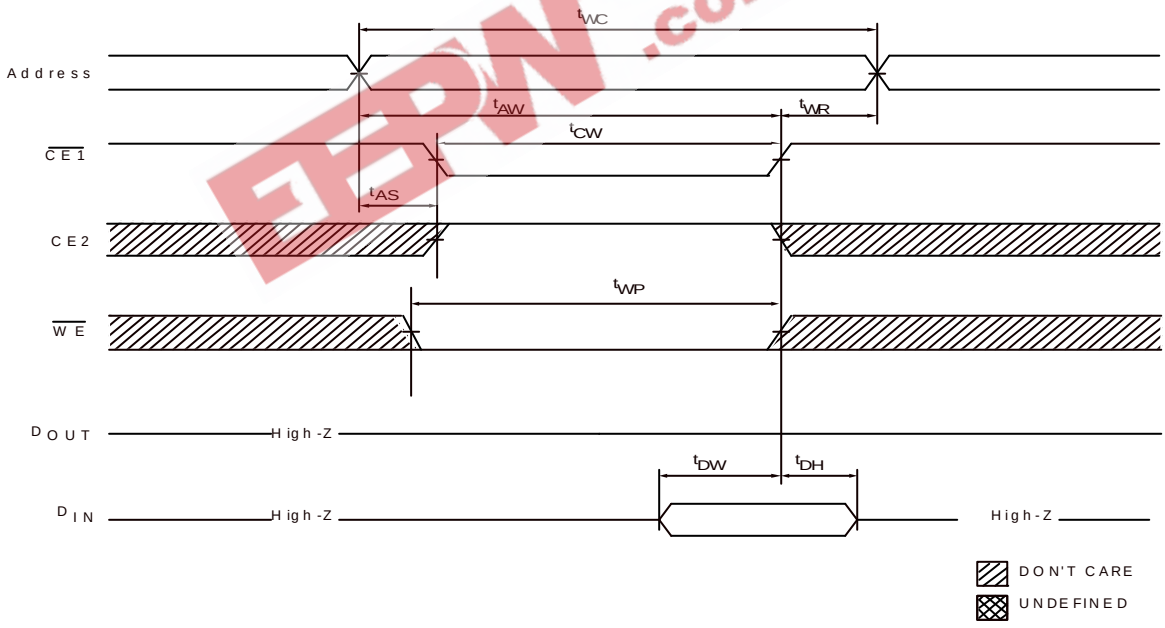
Notes (READ CYCLE) :

1. $\overline{WE}$ are high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition. t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device interconnection.
5. Transition is measured ±200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CE}1 = V_{IL}$.

WRITE CYCLE 1 ($\overline{WE}$ Controlled)



WRITE CYCLE 2 ($\overline{CE}$ Controlled)



NOTES (WRITE CYCLE) :

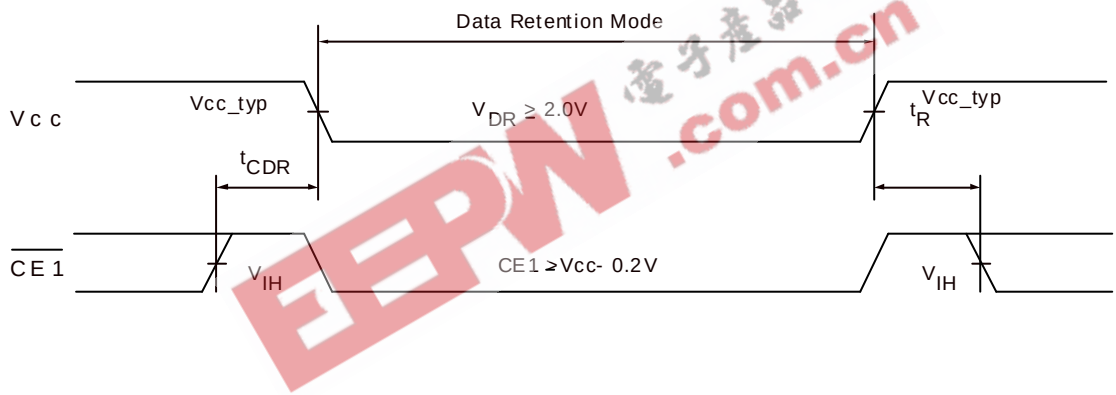
1. A write occurs during the overlap of a low $\overline{CE}1$, a high CE2 and a low $\overline{WE}$. A write begins at the lateat transition among $\overline{CE}1$ goes low, CE2 going high and $\overline{WE}$ going low. A write end at the earliest transition among $\overline{CE}1$ going high, CE2 going low and $\overline{WE}$ going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of $\overline{CE}1$ going low or CE2 going high to the end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change.

DATA RETENTION CHARACTERISTICS

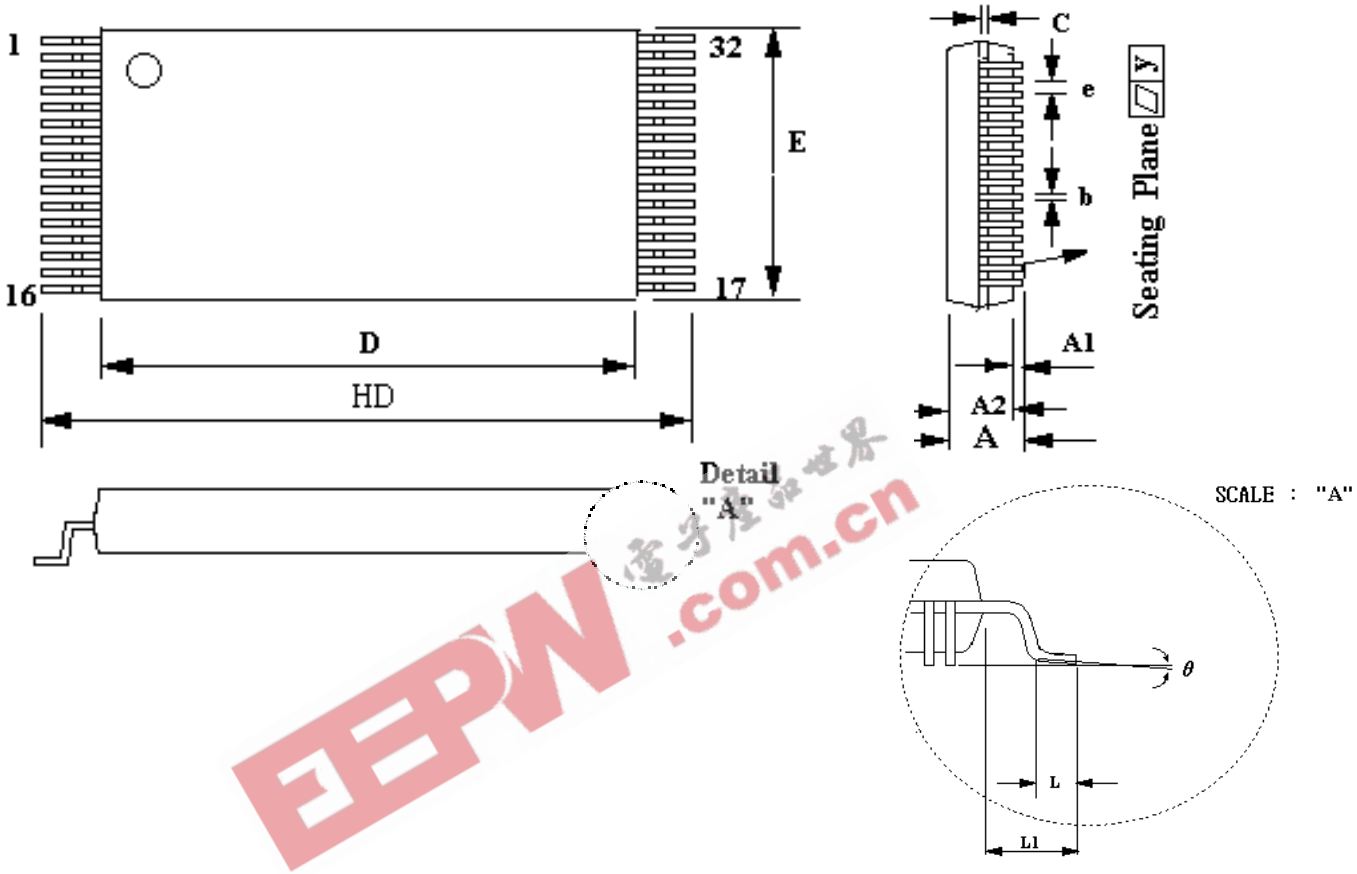
PARAMETER	SYM.	TEST CONDITION	MIN.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	$\overline{CE}1 \geq V_{DD}$ -0.2V	2.0	-	V
Data Retention Current	I_{CCDR}	CE2 ≤ 0.2V	-	5	uA
Chip Deselect to Data Retention Time	t_{CDR}	$V_{IN} \geq$ Vcc -0.2V or	0	-	ns
Operation Recovery Time	t_R	$V_{IN} \leq$ 0.2V	t_{RC}	-	ns

DATA RETENTION WAVEFORM

(Ta = -20°C to 85°C)

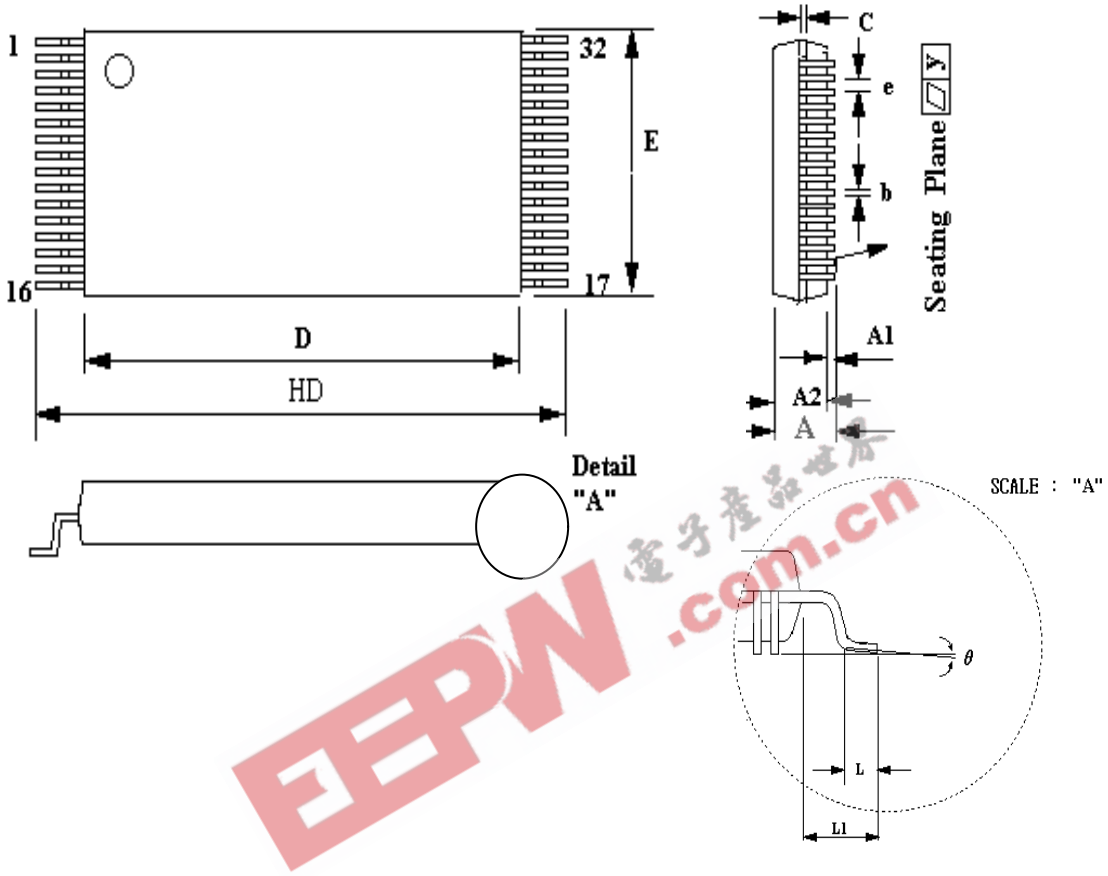


PACKAGE DIMENSIONS
32-LEAD TSOP-I (8x20mm)



SYMBOL	Dimension in inches	Dimension in mm
A	0.044(MAX)	1.10(MAX)
A1	0.004±0.002	0.05±0.05
A2	0.041(MAX)	1.02(MAX)
b	0.008±0.004	0.20±0.10
C	0.006±0.001	0.15±0.02
D	0.724±0.008	18.4±0.2
E	0.315±0.004	8.0±0.1
HD	0.787±0.008	20.0±0.2
e	0.020(TYP.)	0.5(TYP.)
L	0.020±0.004	0.5±0.1
L1	0.031±0.008	0.8±0.2
y	0.002(MAX)	0.05(MAX)
è	0°~5°	0°~5°

PACKAGE DIMENSIONS
32-LEAD TSOP-I (8x13.4mm)



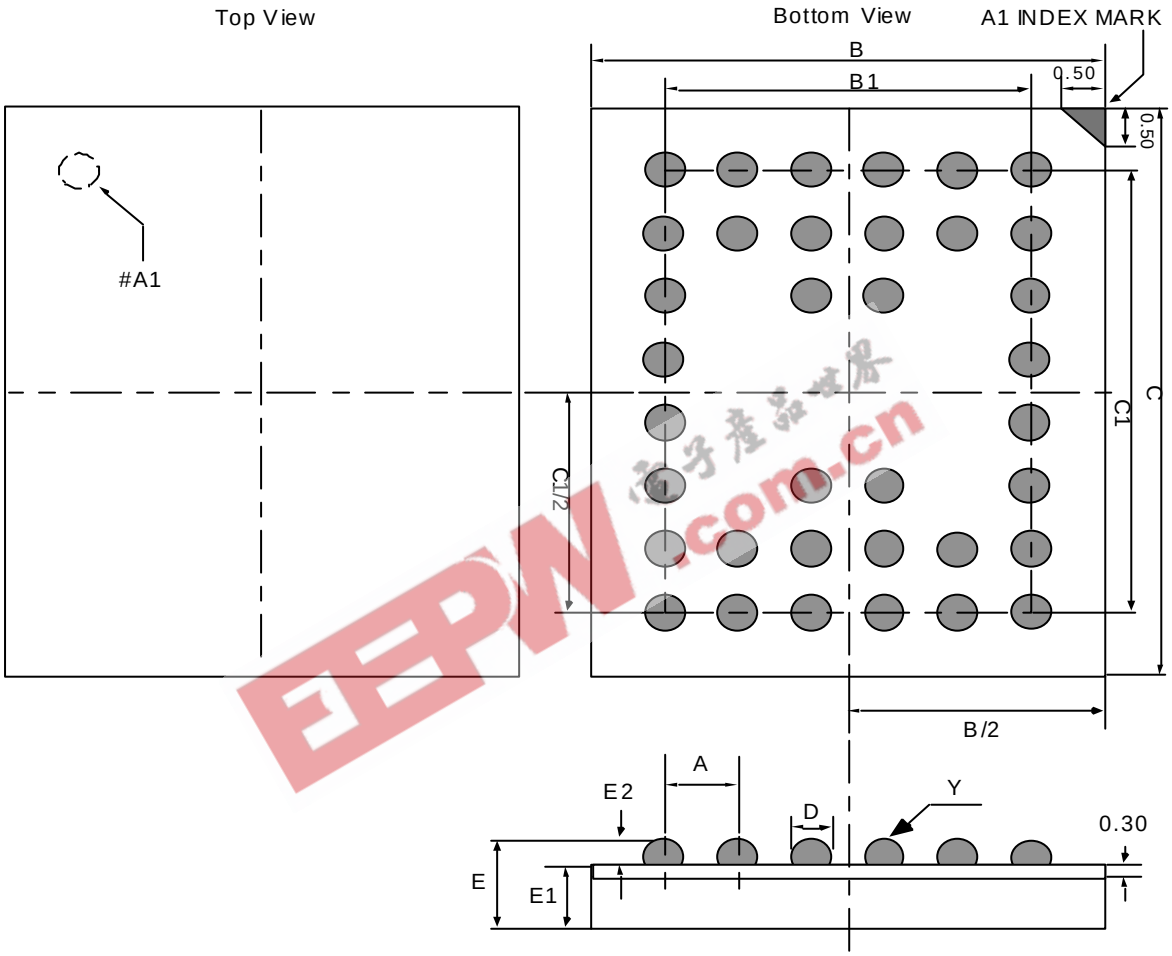
SYMBOL	Dimension in inches	Dimension in mm
A	0.044(MAX)	1.10(MAX)
A1	0.004±0.002	0.05±0.05
A2	0.041(MAX)	1.02(MAX)
b	0.008±0.004	0.20±0.10
C	0.006±0.001	0.15±0.02
D	0.465±0.008	11.8±0.2
E	0.315±0.004	8.0±0.1
HD	0.528±0.008	13.4±0.2
e	0.020(TYP.)	0.5(TYP.)
L	0.020±0.004	0.5±0.1
L1	0.031±0.008	0.8±0.2
y	0.002(MAX)	0.05(MAX)
è	0°~5°	0°~5°

PACKAGE DIMENSIONS

Units : millimeters

48-pin CSP (8 row x 6 column)

48 BALL FINE PITCH BGA (0.75mm ball pitch)



Symbol	min	typ	max
A	-	0.75	-
B	5.95	6.00	6.05
B1	-	3.75	-
C	7.95	8.00	8.05
C1	-	5.25	-
D	0.25	0.30	0.35
E	-	1.10	1.20
E1	-	0.95	-
E2	0.20	0.25	0.30
Y	-	-	0.08

Notes :

1. Bump counts : 48 (8 row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75) typ.
3. All tolerance are ±0.050 unless otherwise specified.
4. 'Y' is coplanarity : 0.08(max)
5. Units : mm