



# Industrial Temperature/Military Screen

## STK12C68-IM

### CMOS nvSRAM

### 8K x 8 *AutoStore*<sup>TM</sup>

### Nonvolatile Static RAM

#### FEATURES

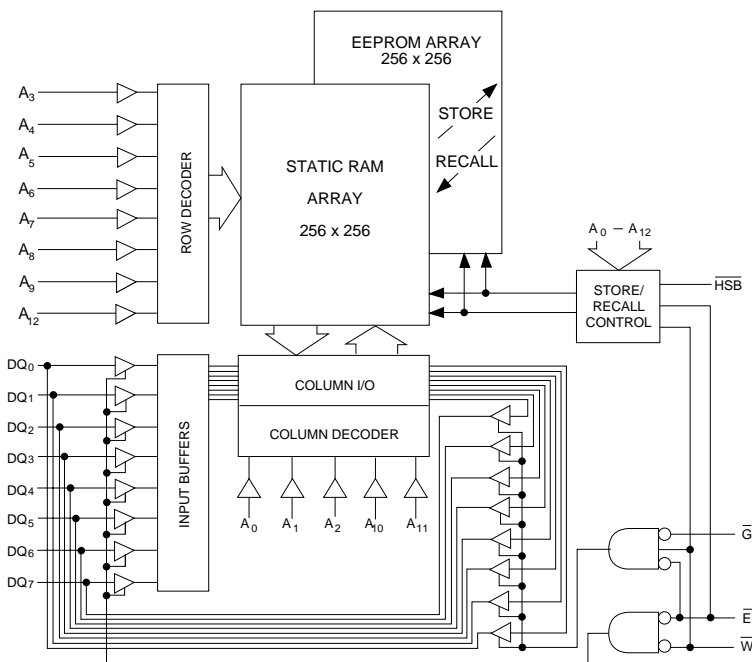
- Industrial Temperature with Military Screening
- 25, 35 and 45ns Access Times
- 15 mA I<sub>CC</sub> at 200ns Access Speed
- Automatic *STORE* to EEPROM on Power Down
- Hardware or Software initiated *STORE* to EEPROM
- Automatic *STORE* Timing
- 100,000 *STORE* cycles to EEPROM
- 10 year data retention in EEPROM
- Automatic *RECALL* on Power Up
- Software initiated *RECALL* from EEPROM
- Unlimited *RECALL* cycles from EEPROM
- Single 5V±10% Operation
- Commercial and Industrial Temperatures
- Available in multiple standard packages

#### DESCRIPTION

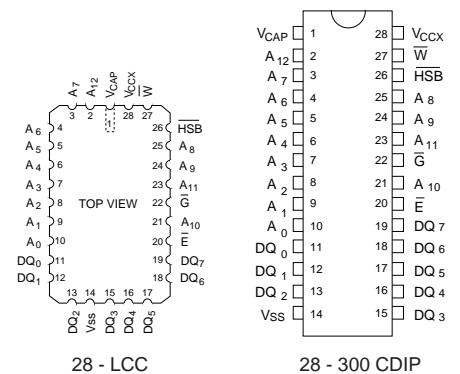
The Simtek STK12C68-IM is a fast static RAM (25, 35 and 45ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) take place automatically upon power down using charge stored in an external 100 μF capacitor. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on power up. Software sequences may also be used to initiate both *STORE* and *RECALL* operations. A *STORE* can also be initiated via a single pin.

The STK12C68-IM is available in the following packages: a 28-pin 300 mil ceramic DIP and a 28-pad LCC. MIL-STD-883 and Standard Military Drawing (SMD 5962-94599) devices are also available.

#### LOGIC BLOCK DIAGRAM



#### PIN CONFIGURATIONS



#### PIN NAMES

A <sub>0</sub> - A <sub>12</sub>	Address Inputs
W	Write Enable
DQ <sub>0</sub> - DQ <sub>7</sub>	Data In/Out
E	Chip Enable
G	Output Enable
V <sub>CCX</sub>	Power (+5V)
V <sub>SS</sub>	Ground
V <sub>CAP</sub>	Capacitor
HSB	Hardware Store/Busy

**ABSOLUTE MAXIMUM RATINGS<sup>a</sup>**

Voltage on typical input relative to  $V_{SS}$ . . . . . -0.6V to 7.0V  
 Voltage on DQ<sub>0-7</sub> and  $\bar{G}$ . . . . . -0.5V to ( $V_{CC}+0.5V$ )  
 Temperature under bias . . . . . -55°C to 125°C  
 Storage temperature. . . . . -65°C to 150°C  
 Power dissipation. . . . . 1W  
 DC output current . . . . . 15mA  
 (One output at a time, one second duration)

**Note a:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC CHARACTERISTICS**

( $V_{CC} = 5.0V \pm 10\%$ )<sup>d</sup>

SYMBOL	PARAMETER	INDUSTRIAL		UNITS	NOTES
		MIN	MAX		
$I_{CC1}^b$	Average $V_{CC}$ Current		95	mA	$t_{AVAV} = 25ns$
			85	mA	$t_{AVAV} = 35ns$
			80	mA	$t_{AVAV} = 45ns$
$I_{CC2}$	Average $V_{CC}$ Current During STORE		7	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
$I_{CC3}^b$	Average $V_{CC}$ Current at $t_{AVAV} = 200ns$		15	mA	$\bar{E} \leq 0.2V, \bar{W} \geq (V_{CC} - 0.2V)$ others $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
$I_{CC4}$	Average $V_{CC}$ current during AutoStore™ Cycle		4	mA	All inputs $\leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
$I_{SB1}^c$	Average $V_{CC}$ Current (Standby, Cycling TTL Input Levels)		39	mA	$t_{AVAV} = 25ns$
			35	mA	$t_{AVAV} = 35ns$
			32	mA	$t_{AVAV} = 45ns$ $\bar{E} \geq V_{IH}$ ; all others cycling
$I_{SB2}^c$	Average $V_{CC}$ Current (Standby, Stable CMOS Input Levels)		3	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
$I_{ILK3}$	Input Leakage Current (Any Input)		$\pm 1$	$\mu A$	$V_{CC} = \max$ $V_{IN} = V_{SS}$ to $V_{CC}$
$I_{OLK}$	Off State Output Leakage Current		$\pm 5$	$\mu A$	$V_{CC} = \max$ $V_{OUT} = V_{SS}$ to $V_{CC}$
$V_{IH}$	Input Logic "1" Voltage	2.2	$V_{CC}+5$	V	All Inputs
$V_{IL}$	Input Logic "0" Voltage	$V_{SS}-5$	0.8	V	All Inputs
$V_{OH}$	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$ except HSB
$V_{OL}$	Output Logic "0" Voltage		0.4	V	$I_{OUT} = 8mA$ except HSB
$T_A$	Operating Temperature	-40	85	°C	

Note b:  $I_{CC1}$  and  $I_{CC3}$  are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.  
 Note c: Bringing  $\bar{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.  
 Note d:  $V_{CC}$  reference levels throughout this datasheet refer to  $V_{CCX}$  if that is where the power supply connection is made, or  $V_{CAP}$  if  $V_{CCX}$  is connected to ground.

**AC TEST CONDITIONS**

Input Pulse Levels. . . . .  $V_{SS}$  to  $V_{CC}$   
 Input Rise and Fall Times. . . . .  $\leq 5ns$   
 Input and Output Timing Reference Levels. . . . . 1.5V  
 Output Load. . . . . See Figure 1

**CAPACITANCE<sup>e</sup>** ( $T_A=25^\circ C, f=1.0MHz$ )

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
$C_{IN}$	Input Capacitance	8	pF	$\Delta V = 0$ to $3V$
$C_{OUT}$	Output Capacitance	7	pF	$\Delta V = 0$ to $3V$

Note e: These parameters are guaranteed but not tested.

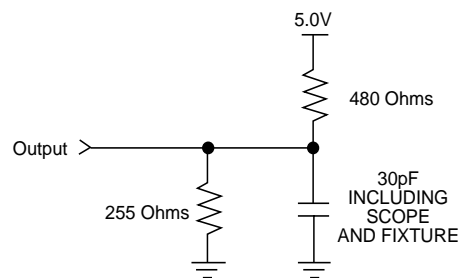


Figure 1: AC Output Loading

## SRAM MEMORY OPERATION

### READ CYCLES #1 & #2

( $V_{CC} = 5.0V \pm 10\%$ )<sup>d</sup>

NO.	SYMBOLS		PARAMETER	STK12C68-25-IM		STK12C68-35-IM		STK12C68-45-IM		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{ELQV}$	$t_{ACS}$	Chip Enable Access Time		25		35		45	ns
2	$t_{AVAV}$	$t_{RC}$	Read Cycle Time	25		35		45		ns
3	$t_{AVQV}^g$	$t_{AA}$	Address Access Time		25		35		45	ns
4	$t_{GLQV}$	$t_{OE}$	Output Enable to Data Valid		10		20		25	ns
5	$t_{AXQX}$	$t_{OH}$	Output Hold After Address Change	5		5		5		ns
6	$t_{ELQX}$	$t_{LZ}$	Chip Enable to Output Active	5		5		5		ns
7	$t_{EHQZ}^h$	$t_{HZ}$	Chip Disable to Output Inactive		10		17		20	ns
8	$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output Active	0		0		0		ns
9	$t_{GHQZ}^h$	$t_{OHZ}$	Output Disable to Output Inactive		10		17		20	ns
10	$t_{ELICCH}^e$	$t_{PA}$	Chip Enable to Power Active	0		0		0		ns
11	$t_{EHICCL}^{c,e}$	$t_{PS}$	Chip Disable to Power Standby		25		35		45	ns

Note c: Bringing  $\bar{E} \geq V_{IH}$  will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

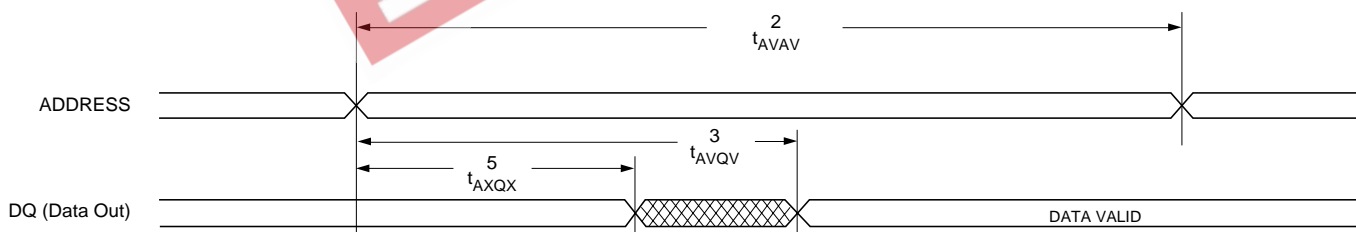
Note e: Parameter guaranteed but not tested.

Note f: For READ CYCLE #1 and #2,  $\bar{W}$  is high for entire cycle.

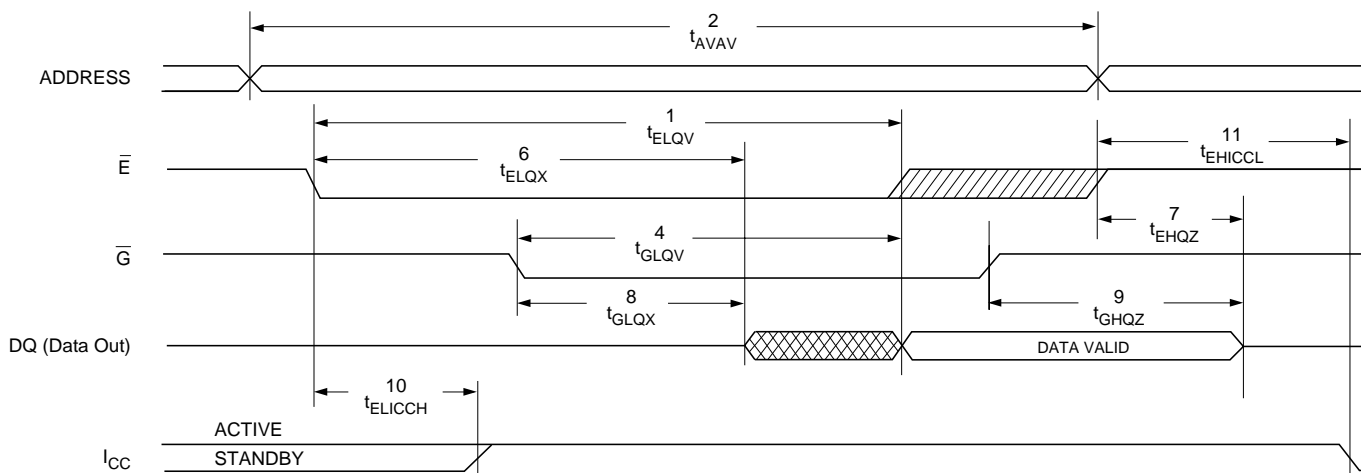
Note g: Device is continuously selected with  $\bar{E}$  low and  $\bar{G}$  low.

Note h: Measured  $\pm 200mV$  from steady state output voltage.

### READ CYCLE #1 <sup>f,g</sup>



### READ CYCLE #2 <sup>f</sup>



WRITE CYCLES #1 & #2

(V<sub>CC</sub> = 5.0V ± 10%)<sup>d</sup>

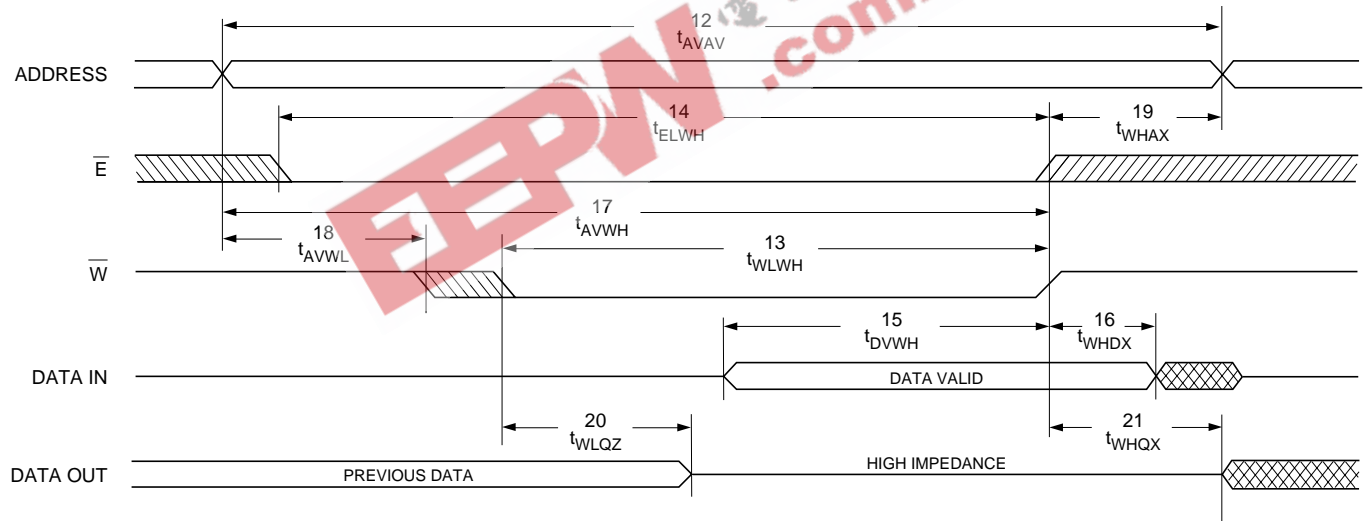
NO.	SYMBOLS			PARAMETER	STK12C68-25-IM		STK12C68-35-IM		STK12C68-45-IM		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t <sub>AVAV</sub>	t <sub>AVAV</sub>	t <sub>WC</sub>	Write Cycle Time	25		35		45		ns
13	t <sub>WLWH</sub>	t <sub>WLEH</sub>	t <sub>WP</sub>	Write Pulse Width	20		30		35		ns
14	t <sub>ELWH</sub>	t <sub>ELEH</sub>	t <sub>CW</sub>	Chip Enable to End of Write	20		30		35		ns
15	t <sub>DVWH</sub>	t <sub>DVEH</sub>	t <sub>DW</sub>	Data Set-up to End of Write	10		18		20		ns
16	t <sub>WHDX</sub>	t <sub>EHDX</sub>	t <sub>DH</sub>	Data Hold After End of Write	0		0		0		ns
17	t <sub>AVWH</sub>	t <sub>AVEH</sub>	t <sub>AW</sub>	Address Set-up to End of Write	20		30		35		ns
18	t <sub>AVWL</sub>	t <sub>AVEL</sub>	t <sub>AS</sub>	Address Set-up to Start of Write	0		0		0		ns
19	t <sub>WHAX</sub>	t <sub>EHAX</sub>	t <sub>WR</sub>	Address Hold After End of Write	0		0		0		ns
20	t <sub>WLQZ</sub> <sup>h,j</sup>		t <sub>WZ</sub>	Write Enable to Output Disable		10		17		20	ns
21	t <sub>WHQX</sub>		t <sub>OW</sub>	Output Active After End of Write	5		5		5		ns

Note h: Measured ±200mV from steady state output voltage.

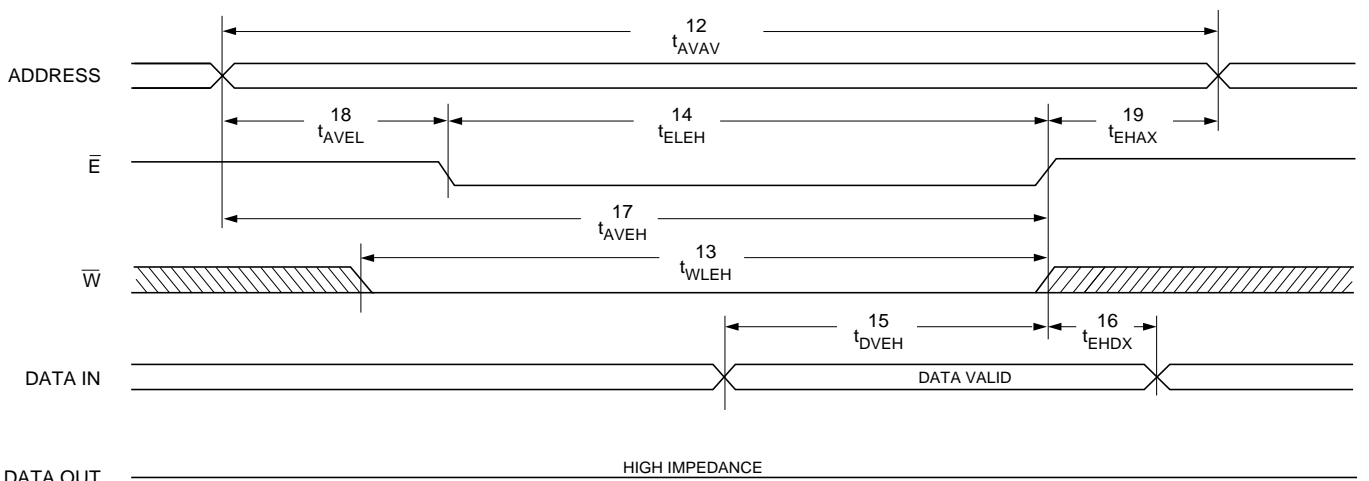
Note i:  $\bar{E}$  or  $\bar{W}$  must be ≥V<sub>IH</sub> during address transitions.

Note j: If  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1:  $\bar{W}$  CONTROLLED<sup>i</sup>



WRITE CYCLE #2:  $\bar{E}$  CONTROLLED<sup>i</sup>



## NONVOLATILE MEMORY OPERATION

### MODE SELECTION

$\bar{E}$	$\bar{W}$	$\overline{HSB}$	A <sub>12</sub> - A <sub>0</sub> (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	l
L	L	H	X	Write SRAM	Input Data	Active	
L	H	H	0000	Read SRAM	Output Data	Active	k,l
			1555	Read SRAM	Output Data		k,l
			0AAA	Read SRAM	Output Data		k,l
			1FFF	Read SRAM	Output Data		k,l
			10F0	Read SRAM	Output Data		k,l
			0F0F	Nonvolatile STORE	Output High Z		k
L	H	H	0000	Read SRAM	Output Data	Active	k,l
			1555	Read SRAM	Output Data		k,l
			0AAA	Read SRAM	Output Data		k,l
			1FFF	Read SRAM	Output Data		k,l
			10F0	Read SRAM	Output Data		k,l
			0F0E	Nonvolatile RECALL	Output High Z		k
X	X	L	X	STORE/Inhibit	Output High Z	I <sub>CC2</sub> /Standby	m

Note k: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle.  $\bar{W}$  must be high during all six consecutive cycles. See STORE cycle and RECALL cycle tables and diagrams for further details.

Note l: I/O state assumes that  $\bar{G} \leq V_{IL}$ . Activation of nonvolatile cycles does not depend on the state of  $\bar{G}$ .

Note m:  $\overline{HSB}$  initiated STORE operation actually occurs only if a WRITE has been done since last STORE operation. After the STORE (if any) completes, the part will go into standby mode inhibiting all operation until  $\overline{HSB}$  rises.

### HARDWARE STORE/RECALL

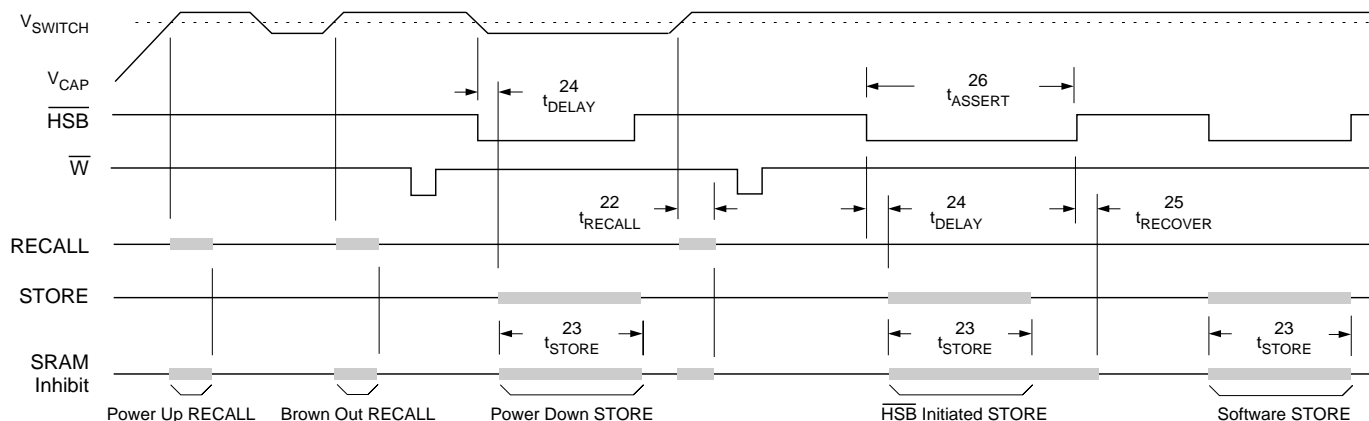
NO.	SYMBOLS		PARAMETER	MIN	MAX	UNITS	NOTES
22	t <sub>RECALL</sub>		RECALL Cycle Duration		20	μs	Note o
23	t <sub>STORE</sub>	t <sub>HLHH</sub>	STORE Cycle Duration		10	ms	V <sub>CC</sub> ≥ 4.5V
24	t <sub>DELAY</sub>	t <sub>HLQZ</sub>	HSB Low to Inhibit On	1		μs	
25	t <sub>RECOVER</sub>	t <sub>HHQX</sub>	$\overline{HSB}$ High to Inhibit Off		700	ns	Note e
26	t <sub>ASSERT</sub>	t <sub>HLHX</sub>	External STORE Pulse Width	250		ns	Note e
	V <sub>SWITCH</sub>		Low Voltage Trigger Level	4.0	4.5	V	
	I <sub>HSB_OL</sub>		$\overline{HSB}$ Output Low Current	3		mA	$\overline{HSB} = V_{OL}$ , Note e, n
	I <sub>HSB_OH</sub>		$\overline{HSB}$ Output High Current	5	60	μA	$\overline{HSB} = V_{IL}$ , Note e, n

Note e: These parameters guaranteed but not tested.

Note n:  $\overline{HSB}$  is an I/O that has a weak internal pullup; it is basically an open drain output. It is meant to allow up to 32 STK12C68-IMs to be ganged together for simultaneous storing. Do not use  $\overline{HSB}$  to pullup any external circuitry other than other STK12C68  $\overline{HSB}$  pins.

Note o: A RECALL cycle is initiated automatically at power up when V<sub>CC</sub> exceeds V<sub>SWITCH</sub>. t<sub>RESTORE</sub> is measured from the point at which V<sub>CC</sub> exceeds 4.5V.

### HARDWARE STORE/RECALL



SOFTWARE STORE/RECALL CYCLE

(V<sub>CC</sub> = 5.0V ± 10%)<sup>d</sup>

NO.	SYMBOLS		PARAMETER	STK12C68-25-IM		STK12C68-35-IM		STK12C68-45-IM		UNITS
	Std.	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
27	t <sub>AVAV</sub>	t <sub>RC</sub>	Store/Recall Initiation Cycle Time	25		35		45		ns
28	t <sub>ELQZ</sub> <sup>p</sup>		Chip Enable to Output Inactive		650		650		650	ns
29	t <sub>AVELN</sub>	t <sub>AE</sub>	Address Set-up to Chip Enable	0		0		0		ns
30	t <sub>ELEHN</sub> <sup>p,q</sup>	t <sub>EP</sub>	Chip Enable Pulse Width	20		25		35		ns
31	t <sub>EHAXN</sub>	t <sub>EA</sub>	Chip Disable to Address Change	0		0		0		ns
32	t <sub>RESTORE</sub>		Power-up Recall Duration		550		550		550	μs

Note p: Once the software *STORE* or *RECALL* cycle is initiated, it completes automatically, ignoring all inputs.

Note q: Noise on the  $\bar{E}$  pin may trigger multiple read cycles from the same address and abort the address sequence.

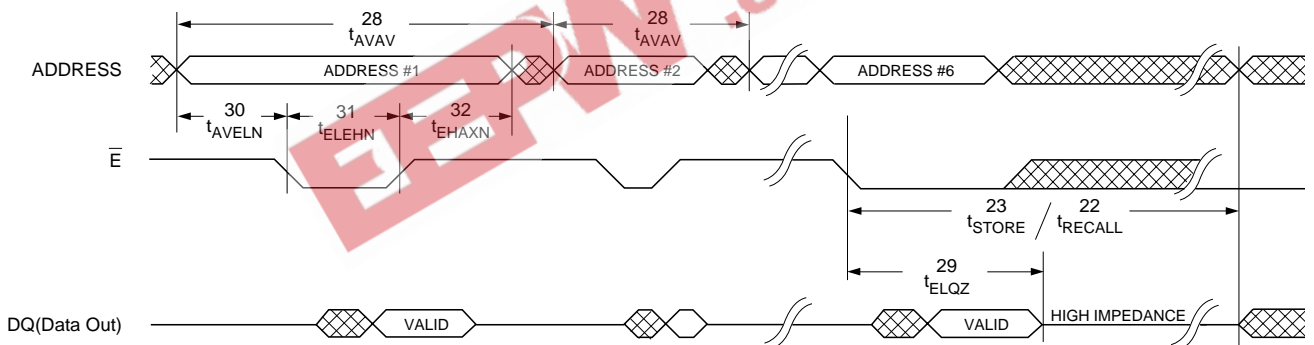
Note r: If the Chip Enable Pulse Width is less than t<sub>ELQV</sub> (see *READ CYCLE #2*) but greater than or equal to t<sub>ELEHN</sub>, then the data may not be valid at the end of the low pulse, however the *STORE* or *RECALL* will still be initiated.

Note s: W must be HIGH when  $\bar{E}$  is LOW during the address sequence in order to initiate a nonvolatile cycle.  $\bar{G}$  may be either HIGH or LOW throughout.

Addresses #1 through #6 are found in the *MODE SELECTION* table. Address #6 determines whether the STK12C68-IM performs a *STORE* or *RECALL*.

Note t:  $\bar{E}$  must be used to clock in the address sequence for the Software *STORE* and *RECALL* cycles.

SOFTWARE STORE/RECALL CYCLE q,r,t





## DEVICE OPERATION

The STK12C68-IM has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

*STORE* cycles may be initiated under user control via a software sequence or  $\overline{\text{HSB}}$  assertion and are also automatically initiated when the power supply voltage level of the chip falls below  $V_{\text{SWITCH}}$ . *RECALL* operations are automatically initiated upon power-up and whenever the power supply voltage level rises above  $V_{\text{SWITCH}}$ . *RECALL* cycles may also be initiated by a software sequence.

### SRAM READ

The STK12C68-IM performs a READ cycle whenever  $\overline{\text{E}}$  and  $\overline{\text{G}}$  are LOW and  $\overline{\text{HSB}}$  and  $\overline{\text{W}}$  are HIGH. The address specified on pins  $\text{A}_{0-12}$  determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{\text{AVQV}}$ . If the READ is initiated by  $\overline{\text{E}}$  or  $\overline{\text{G}}$ , the outputs will be valid at  $t_{\text{ELQV}}$  or at  $t_{\text{GLQV}}$ , whichever is later. The data outputs will repeatedly respond to address changes within the  $t_{\text{AVQV}}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{\text{E}}$  or  $\overline{\text{G}}$  is brought HIGH or  $\overline{\text{W}}$  or  $\overline{\text{HSB}}$  is brought LOW.

### SRAM WRITE

A write cycle is performed whenever  $\overline{\text{E}}$  and  $\overline{\text{W}}$  are LOW and  $\overline{\text{HSB}}$  is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{\text{E}}$  or  $\overline{\text{W}}$  go HIGH at the end of the cycle. The data on pins  $\text{DQ}_{0-7}$  will be written into the memory if it is valid  $t_{\text{DVWH}}$  before the end of a  $\overline{\text{W}}$  controlled WRITE or  $t_{\text{DVEH}}$  before the end of an  $\overline{\text{E}}$  controlled WRITE.

It is recommended that  $\overline{\text{G}}$  be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If  $\overline{\text{G}}$  is left LOW, internal circuitry will turn off the output buffers  $t_{\text{WLQZ}}$  after  $\overline{\text{W}}$  goes LOW.

### SOFTWARE STORE

The STK12C68-IM software *STORE* cycle is initiated by executing sequential READ cycles from six specific

address locations. By relying on READ cycles only, the STK12C68-IM implements nonvolatile operation while remaining compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into the nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of addresses is used for *STORE* initiation, it is critical that no other read or write accesses intervene in the sequence or the sequence will be aborted.

To initiate the *STORE* cycle the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate <i>STORE</i> Cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that  $\overline{\text{G}}$  be LOW for the sequence to be valid. After the  $t_{\text{STORE}}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

### SOFTWARE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

1.	Read address	0000(hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate <i>RECALL</i> Cycle

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the

EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

**AUTOMATIC RECALL**

During power-up, or after any low power condition ( $V_{CAP} < V_{SWITCH}$ ), when  $V_{CAP}$  exceeds the sense voltage of  $V_{SWITCH}$ , a *RECALL* cycle will automatically be initiated.

If the STK12C68-IM is in a *WRITE* state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected between *W* and system  $V_{CC}$ .

**HARDWARE PROTECT**

The STK12C68-IM offers hardware protection against inadvertent *STORE* operation during low voltage conditions. When  $V_{CAP} < V_{SWITCH}$ , all externally initiated *STORE* operations will be inhibited.

**HSB OPERATION**

The Hardware Store Busy pin ( $\overline{HSB}$ ) is an open drain circuit acting as both input and output to perform two different functions. When driven low by the internal chip circuitry it indicates that a *STORE* operation (initiated via any means) is in progress within the chip. When driven low by external circuitry for longer than  $t_{ASSERT}$ , the chip will conditionally initiate a *STORE* operation after  $t_{DELAY}$ .

*READ* and *WRITE* operations that are in progress when  $\overline{HSB}$  is driven low (either by internal or external circuitry) will be allowed to complete before the *STORE* operation is performed, in the following manner. After  $\overline{HSB}$  goes low, the part will continue normal SRAM operations for  $t_{DELAY}$ . During  $t_{DELAY}$ , a transition on any address or control signal will terminate SRAM operation and cause the *STORE* to commence. Note that if an SRAM write is attempted after  $\overline{HSB}$  has been forced low, the write will not occur and the *STORE* operation will begin immediately.

HARDWARE-STORE-BUSY ( $\overline{HSB}$ ) is a high speed, low drive capability bi-directional control line. In order to allow a bank of STK12C68-IMs to perform synchronized *STORE* functions, the  $\overline{HSB}$  pin from a number of chips may be connected together. Each chip contains a small internal current source to pull  $\overline{HSB}$  HIGH when it is not being driven low. To decrease the sensitivity of this signal to noise generated on the PC board, it

may optionally be pulled to  $V_{CCX}$  via an external resistor with a value such that the combined load of the resistor and all parallel chip connections does not exceed  $I_{\overline{HSB\_OL}}$  at  $V_{OL}$ . Do not connect this or any other pull-up to the  $V_{CAP}$  node.

If  $\overline{HSB}$  is to be connected to external circuits other than other STK12C68-IMs, an external pull-up resistor should be used.

During any *STORE* operation, regardless of how it was initiated, the STK12C68-IM will continue to drive the  $\overline{HSB}$  pin low, releasing it only when the *STORE* is complete. Upon completion of a *STORE* operation, the part will be disabled until  $\overline{HSB}$  actually goes HIGH.

**AUTOMATIC STORE OPERATION**

During normal operation, the STK12C68-IM will draw current from  $V_{CCX}$  to charge up a capacitor connected to the  $V_{CAP}$  pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the  $V_{CAP}$  pin drops below  $V_{SWITCH}$ , the part will automatically disconnect the  $V_{CAP}$  pin from  $V_{CCX}$  and initiate a *STORE* operation.

*Figure 1* shows the proper connection of capacitors for automatic store operation. The charge storage capacitor should have a capacity of at least 100 $\mu$ F ( $\pm 20\%$ ) at 6V. Each STK12C68-IM must have its own 100 $\mu$ F capacitor. Each STK12C68-IM *must* have a high quality, high frequency bypass capacitor of 0.1 $\mu$ F connected between  $V_{CAP}$  and  $V_{SS}$ , using leads and traces that are as short as possible.

If the *AutoStore*<sup>TM</sup> function is not required, then  $V_{CAP}$  should be tied directly to the power supply and  $V_{CCX}$  should be tied to ground. In this mode, *STORE* operations may be triggered through software control or the  $\overline{HSB}$  pin. In either event,  $V_{CAP}$  (Pin 1) *must* always have a proper bypass capacitor connected to it.

In order to prevent unneeded *STORE* operations, automatic *STOREs* as well as those initiated by externally driving  $\overline{HSB}$  LOW will be ignored unless at least one *WRITE* operation has taken place since the most recent *STORE* cycle. Note that if  $\overline{HSB}$  is driven low via external circuitry and no *WRITES* have taken place, the part will still be disabled until  $\overline{HSB}$  is allowed to return HIGH. Software initiated *STORE* cycles are performed regardless of whether or not a *WRITE* operation has taken place.



### PREVENTING AUTOMATIC STORES

The *AutoStore*<sup>TM</sup> function can be disabled on the fly by holding  $\overline{\text{HSB}}$  HIGH with a driver capable of sourcing 15mA at a  $\text{VOH}$  of at least 2.2V as it will have to overpower the internal pull-down device that drives  $\overline{\text{HSB}}$  low for 20 $\mu\text{s}$  at the onset of an *AutoStore*<sup>TM</sup>. When the STK12C68-IM is connected for *AutoStore*<sup>TM</sup> operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CCX}}$  and a 100 $\mu\text{F}$  capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH}}$  on the way down, the STK12C68-IM will attempt to pull  $\overline{\text{HSB}}$  low; if  $\overline{\text{HSB}}$  doesn't actually get below  $V_{\text{IL}}$ , the part will stop trying to pull  $\overline{\text{HSB}}$  LOW and abort the *AutoStore*<sup>TM</sup> attempt.

### LOW AVERAGE ACTIVE POWER

The STK12C68-IM has been designed to draw significantly less power when  $\overline{\text{E}}$  is LOW (chip enabled) but the access cycle time is longer than 55ns. *Figure 2* below shows the relationship between  $I_{\text{CC}}$  and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels. *Figure 3* shows the same relationship for WRITE cycles. When  $\overline{\text{E}}$  is HIGH, the chip consumes only standby currents, and these plots do not apply.

The cycle time used in *Figure 2* corresponds to the length of time from the later of the last address transition or  $\overline{\text{E}}$  going LOW to the earlier of  $\overline{\text{E}}$  going HIGH or the next address transition.  $\overline{\text{W}}$  is assumed to be HIGH, while the state of  $\overline{\text{G}}$  does not matter. Additional current is consumed when the address lines change state while  $\overline{\text{E}}$  is asserted. The cycle time used in *Figure 3* corresponds to the length of time from the later of  $\overline{\text{W}}$  or  $\overline{\text{E}}$  going LOW to the earlier of  $\overline{\text{W}}$  or  $\overline{\text{E}}$  going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled ( $\overline{\text{E}}$  HIGH); 3) the cycle time for accesses ( $\overline{\text{E}}$  LOW); 4) the ratio of reads to writes; 5) the operating temperature; 6) the  $V_{\text{CC}}$  level; and 7) output load.

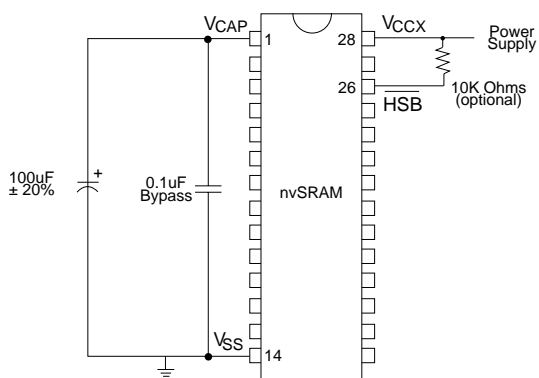


Figure 1  
Schematic Diagram

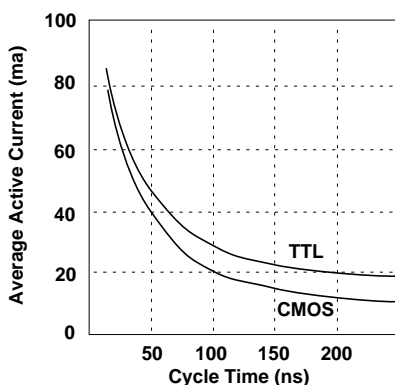


Figure 2  
 $I_{\text{CC}}$  (Max) Reads

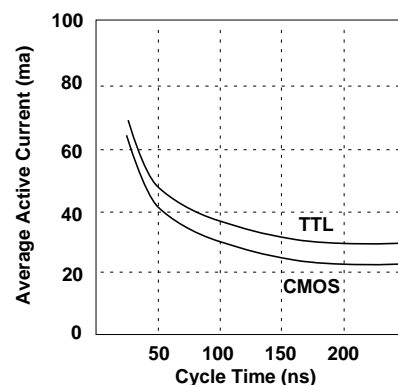


Figure 3  
 $I_{\text{CC}}$  (Max) Writes

Note: Typical at 25° C

### ORDERING INFORMATION

STK12C68 - C 35 IM

Temperature Range

IM = Industrial (-40 to +85°C) with Military Screening

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

C = Ceramic 28 pin 300 mil DIP with Gold Lead Finish

K = Ceramic 28 pin 300 mil DIP with Solder DIP

L = Ceramic 28 pin LCC

