STK10C68

STK10C68-M SMD#5962-93056

8K x 8 nvSRAM

QuantumTrap™ CMOS Nonvolatile Static RAM

Obsolete - Not Recommend for new Designs

FEATURES

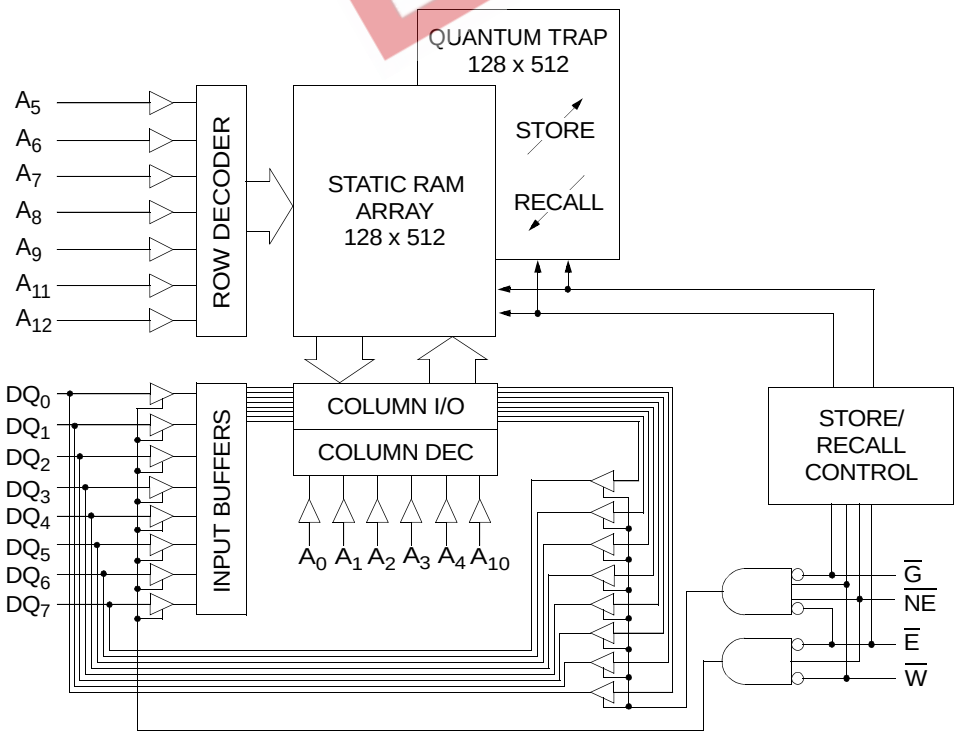
- **25ns, 35ns, 45ns and 55ns Access Times**
- ***STORE* to Nonvolatile Elements Initiated by Hardware**
- ***RECALL* to SRAM Initiated by Hardware or Power Restore**
- **Automatic *STORE* Timing**
- **10mA Typical I_{CC} at 200ns Cycle Time**
- **Unlimited READ, WRITE and *RECALL* Cycles**
- **1,000,000 *STORE* Cycles to Nonvolatile Elements (Industrial/Commercial)**
- **100-Year Data Retention (Industrial/Commercial)**
- **Commercial, Industrial and Military Temperatures**
- **28-Pin DIP, SOIC and LCC Packages**

DESCRIPTION

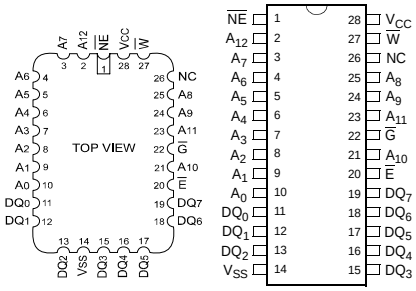
The Simtek STK10C68 is a fast static RAM with a nonvolatile element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in Nonvolatile Elements. Data may easily be transferred from the SRAM to the Nonvolatile Elements (the *STORE* operation), or from the Nonvolatile Elements to the SRAM (the *RECALL* operation), using the $\overline{NE}$ pin. Transfers from the Nonvolatile Elements to the SRAM (the *RECALL* operation) also take place automatically on restoration of power. The STK10C68 combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

The STK10C68 features industry-standard pinout for nonvolatile RAMs. MIL-STD-883 and Standard Military Drawing (SMD #5962-93056) devices are available.

BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - LCC

28 - DIP
28 - SOIC

PIN NAMES

A_0 - A_{12}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . . –0.5V to 7.0V
Voltage on Input Relative to V_{SS} . . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL/ MILITARY		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}[b]	Average V_{CC} Current		85 75 65 N/A		90 75 65 55	mA mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns t_{AVAV} = 55ns
I_{CC2}[c]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max
I_{CC3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{SB1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		27 23 20 N/A		28 24 21 20	mA mA mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 55ns, $\overline{E} \geq V_{IH}$
I_{SB2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		750		1500	µA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Note a: Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	–40/-55	85/125	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC2} is the average current required for the duration of the *STORE* cycle (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0V to 3V
Input Rise and Fall Times . . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE[e]

(T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

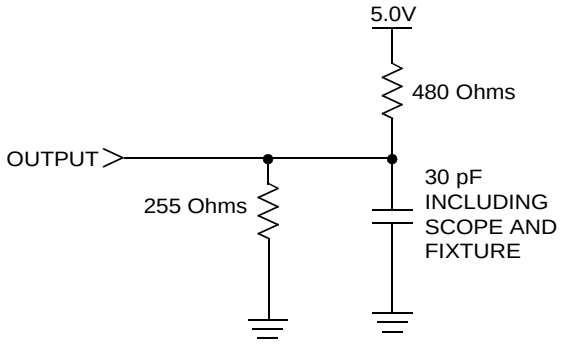


Figure 1: AC Output Loading

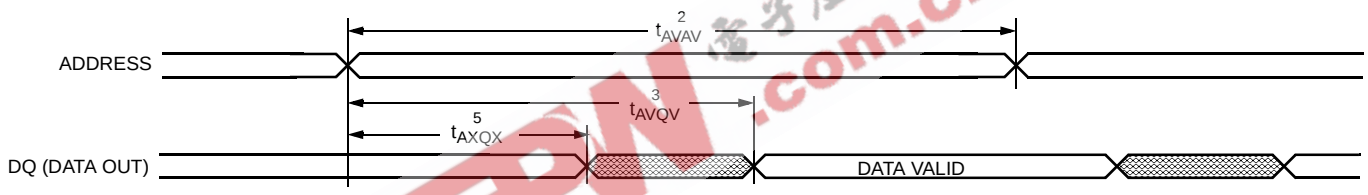
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

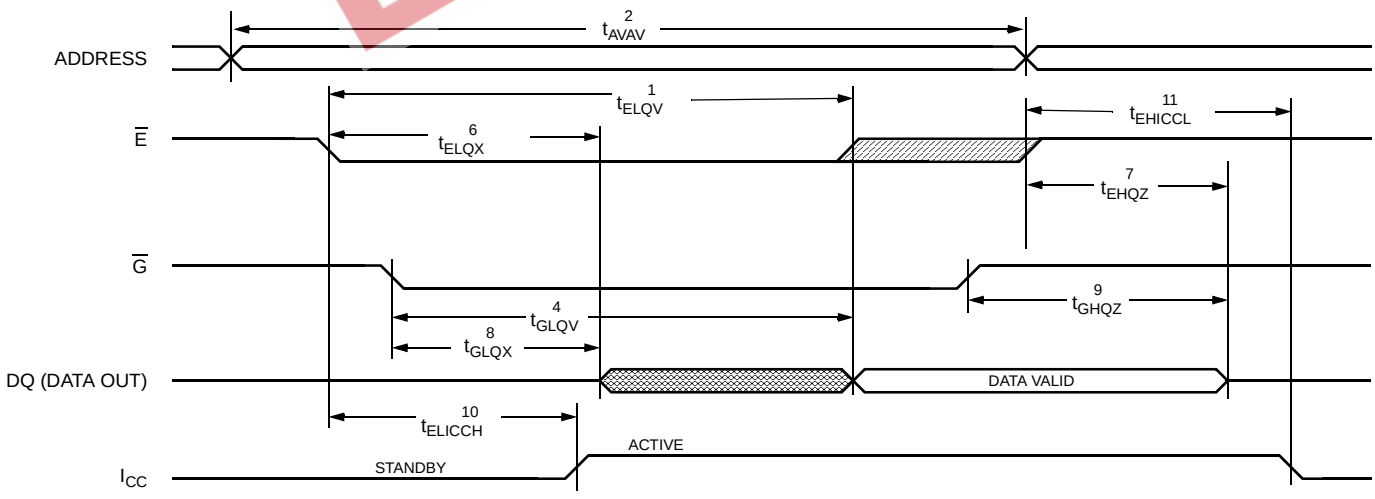
NO.	SYMBOLS		PARAMETER	STK10C68-25		STK10C68-35		STK10C68-45		STK10C68-55		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45		55	ns
2	t_{AVAV}[f]	t_{RC}	Read Cycle Time	25		35		45		55		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		25		35		45		55	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20		25	ns
5	t_{AXQX}[g]	t_{OH}	Output Hold after Address Change	5		5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns
7	t_{EHQZ}[h]	t_{HZ}	Chip Disable to Output Inactive		10		10		12		12	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		10		10		12		12	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t_{EHICCL}[d, e]	t_{PS}	Chip Disable to Power Standby		25		35		45		55	ns

Note f: $\overline{W}$ must be high during SRAM READ cycles and low during SRAM WRITE cycles. $\overline{NE}$ must be high during entire cycle.
Note g: I/O state assumes $\overline{E}$, $\overline{G} \le V_{IL}$, $\overline{W} \ge V_{IH}$, and $\overline{NE} \ge V_{IH}$; device is continuously selected.
Note h: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[f, g]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[f]



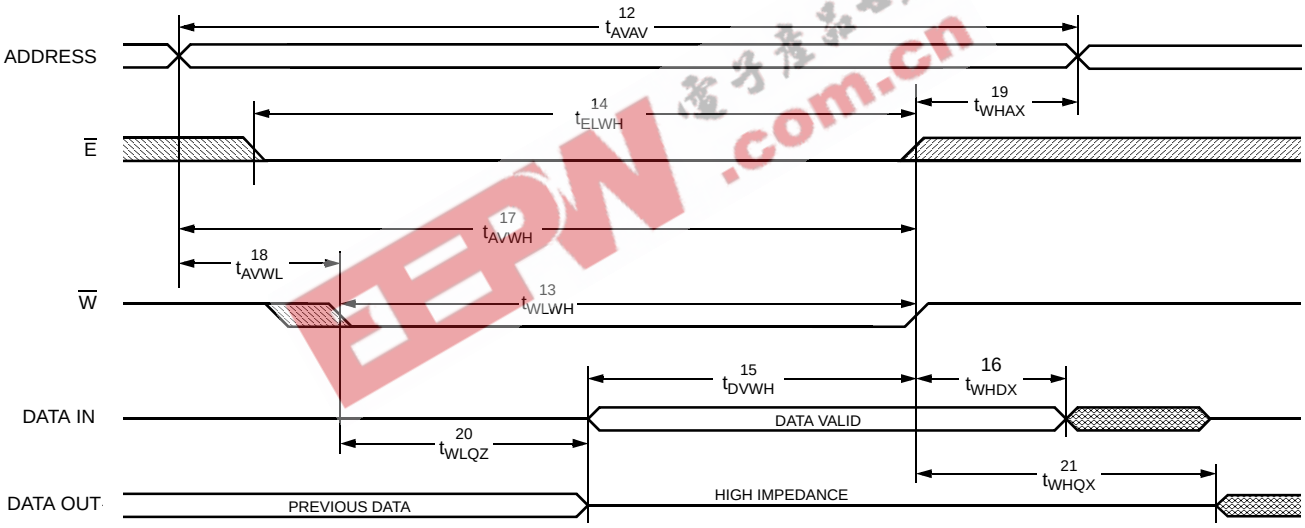
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

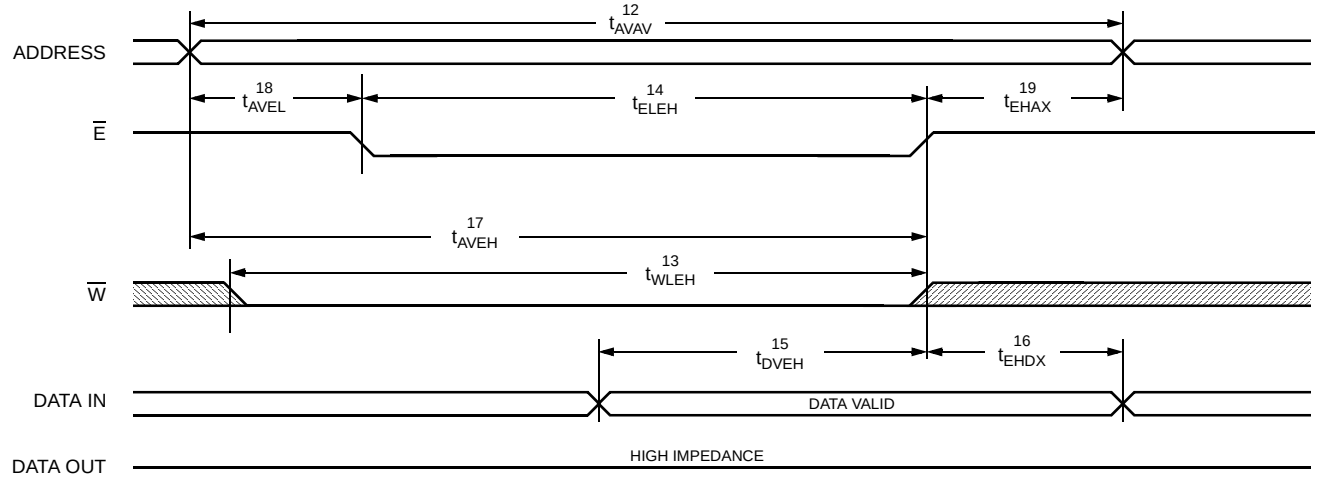
NO.	SYMBOLS			PARAMETER	STK10C68-25		STK10C68-35		STK10C68-45		STK10C68-55		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		45		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		45		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		30		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		45		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		0		ns
20	t_{WLQZ}[h, i]		t_{WZ}	Write Enable to Output Disable		10		13		14		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		5		ns

Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions. $\overline{NE}$ ≥ V_{IH}.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[j]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[j]



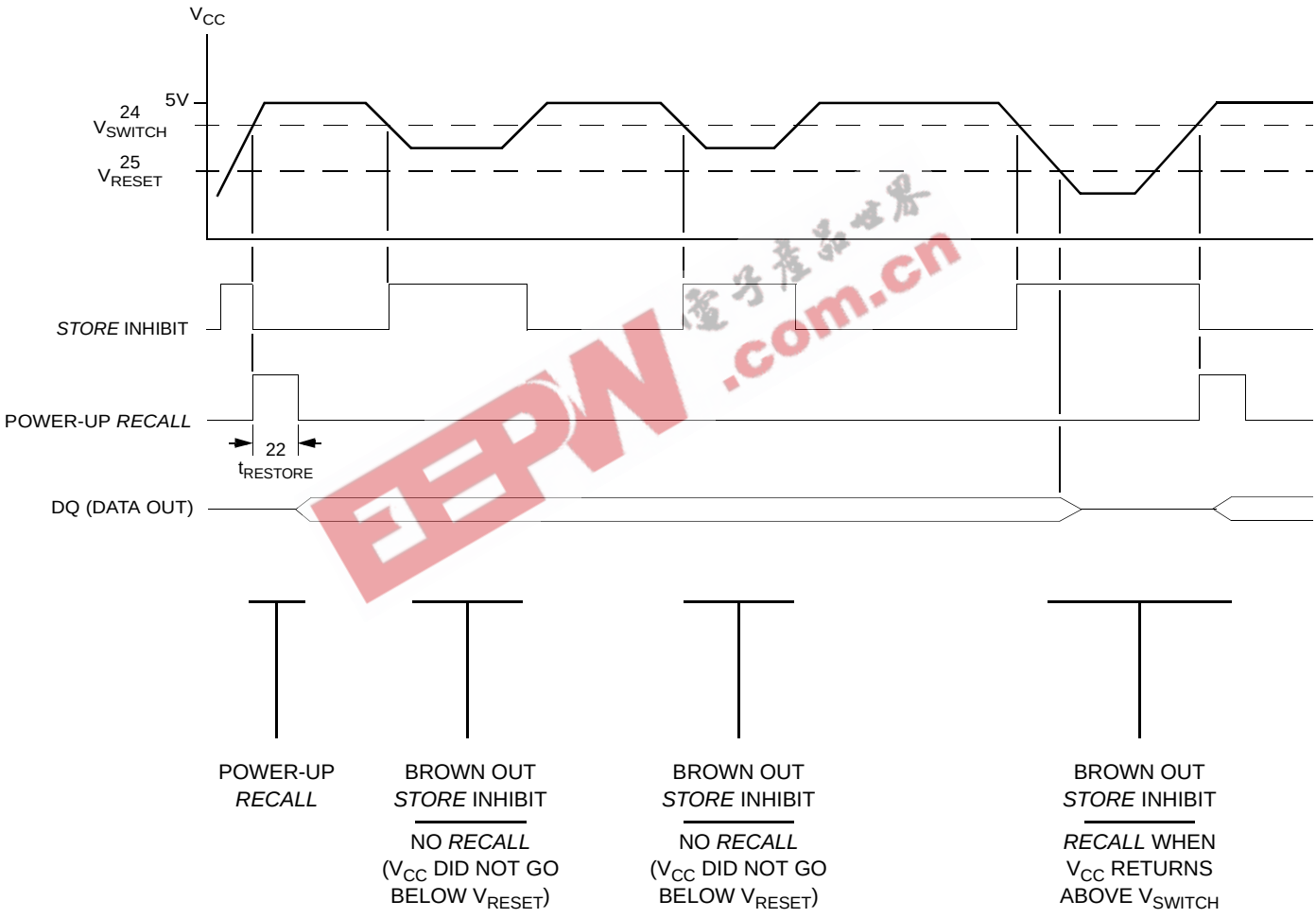
STORE INHIBIT/POWER-UP *RECALL*

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK10C68		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-up *RECALL* Duration		550	µs	k
23	t_{STORE}	*STORE* Cycle Duration		10	ms	
24	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
25	V_{RESET}	Low Voltage Reset Level		3.6	V	

Note k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

STORE INHIBIT/POWER-UP *RECALL*



MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$	MODE	POWER
H	X	X	X	Not Selected	Standby
L	H	L	H	Read SRAM	Active
L	L	X	H	Write SRAM	Active
L	H	L	L	Nonvolatile *RECALL*[l]	Active
L	L	H	L	Nonvolatile *STORE*	I_{CC2}
L L	L H	L H	L X	No Operation	Active

Note l: An automatic *RECALL* takes place at power up, starting when V_{CC} exceeds 4.25V and taking $t_{RESTORE}$.

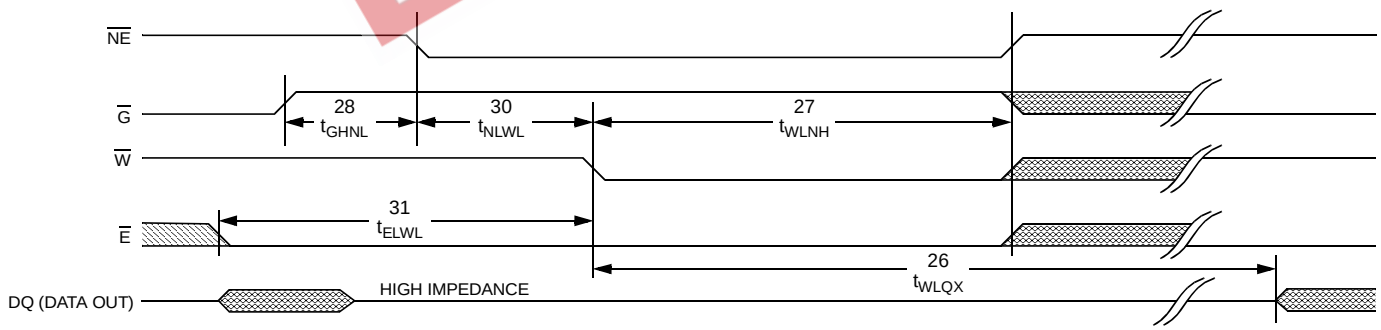
STORE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

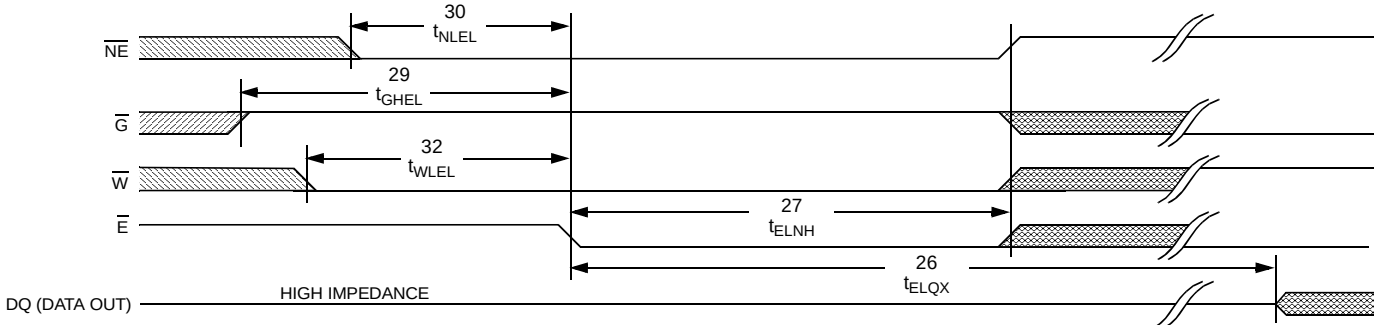
NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	Alt.				
26	t_{WLQX}[m]	t_{ELQX}	t_{STORE}	*STORE* Cycle Time		10	ms
27	t_{WLNH}[n]	t_{ELNH}	t_{WC}	*STORE* Initiation Cycle Time	20		ns
28	t_{GHNL}			Output Disable Set-up to $\overline{NE}$ Fall	0		ns
29		t_{GHEL}		Output Disable Set-up to $\overline{E}$ Fall	0		ns
30	t_{NLWL}	t_{NLEL}		$\overline{NE}$ Set-up	0		ns
31	t_{ELWL}			Chip Enable Set-up	0		ns
32		t_{WLEL}		Write Enable Set-up	0		ns

Note m: Measured with $\overline{W}$ and $\overline{NE}$ both returned high, and $\overline{G}$ returned low. *STORE* cycles are inhibited below 4.0V.
Note n: Once t_{WC} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the *STORE* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$, $\overline{W}$ or $\overline{E}$ may be used to terminate the *STORE* initiation cycle.
Note o: If $\overline{E}$ is low for any period of time in which $\overline{W}$ is high while $\overline{G}$ and $\overline{NE}$ are low, then a *RECALL* cycle may be initiated.

STORE CYCLE #1: $\overline{W}$ Controlled[o]



STORE CYCLE #2: $\overline{E}$ Controlled[o]



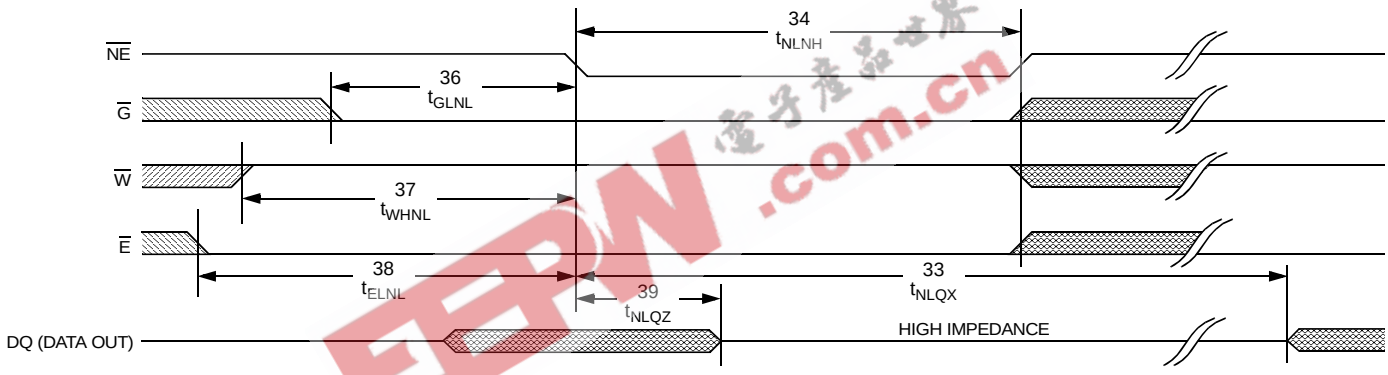
RECALL CYCLES #1, #2 & #3

(V_{CC} = 5.0V ± 10%)

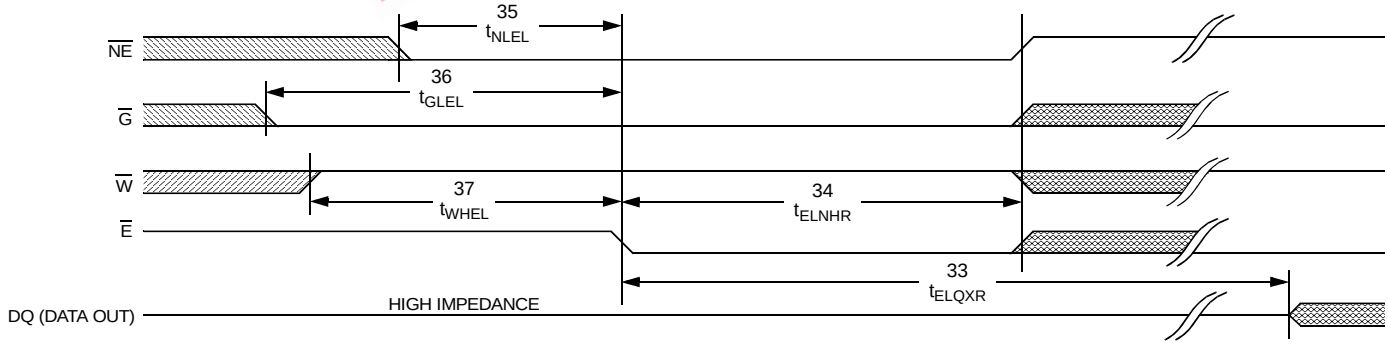
NO.	SYMBOLS			PARAMETER	MIN	MAX	UNITS
	#1	#2	#3				
33	t_{NLQX}[p]	t_{ELQXR}	t_{GLQXR}	*RECALL* Cycle Time		20	µs
34	t_{NLNH}[q]	t_{ELNHR}	t_{GLNH}	*RECALL* Initiation Cycle Time	20		ns
35		t_{NLEL}	t_{NLGL}	$\overline{NE}$ Set-up	0		ns
36	t_{GLNL}	t_{GLEL}		Output Enable Set-up	0		ns
37	t_{WHNL}	t_{WHEL}	t_{WHGL}	Write Enable Set-up	0		ns
38	t_{ELNL}	t_{GLEL}	t_{ELGL}	Chip Enable Set-up	0		ns
39	t_{NLQZ}			$\overline{NE}$ Fall to Outputs Inactive		20	ns
40	$t_{RESTORE}$			Power-up *RECALL* Duration		550	µs

Note p: Measured with $\overline{W}$ and $\overline{NE}$ both high, and $\overline{G}$ and $\overline{E}$ low.
Note q: Once t_{NLNH} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the *RECALL* cycle is completed automatically. Any of $\overline{NE}$, $\overline{G}$ or $\overline{E}$ may be used to terminate the *RECALL* initiation cycle.
Note r: If $\overline{W}$ is low at any point in which both $\overline{E}$ and $\overline{NE}$ are low and $\overline{G}$ is high, then a *STORE* cycle will be initiated instead of a *RECALL*.

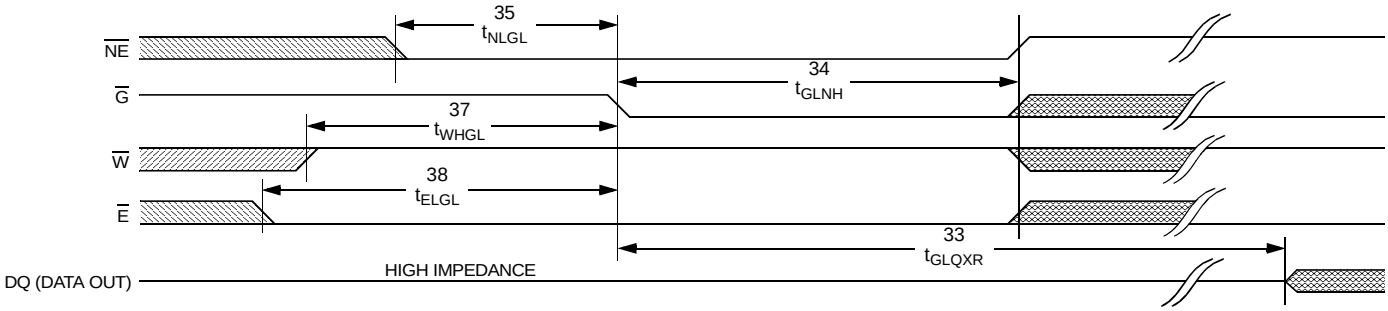
RECALL CYCLE #1: $\overline{NE}$ Controlled[o]



RECALL CYCLE #2: $\overline{E}$ Controlled[o]



RECALL CYCLE #3: $\overline{G}$ Controlled[o, r]



DEVICE OPERATION

The STK10C68 has two modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pin. When in SRAM mode, the memory operates as a standard fast static RAM. While in nonvolatile mode, data is transferred in parallel from SRAM to Nonvolatile Elements or from Nonvolatile Elements to SRAM.

NOISE CONSIDERATIONS

Note that the STK10C68 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK10C68 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{NE}$ and $\overline{W}$ are high. The address specified on pins A_{0-12} determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high or $\overline{W}$ or $\overline{NE}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{NE}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

NONVOLATILE *STORE*

A *STORE* cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ and low and $\overline{G}$ is high. While any sequence that achieves this state will initiate a *STORE*, only $\overline{W}$ initiation (*STORE* cycle #1) and $\overline{E}$ initiation (*STORE* cycle #2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a *STORE* cycle, previous nonvolatile data is erased and the SRAM contents are then programmed into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled and the DQ_{0-7} pins are tri-stated until the cycle is complete.

If $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ and $\overline{NE}$ are high at the end of the cycle, a READ will be performed and the outputs will go active, signaling the end of the *STORE*.

NONVOLATILE *RECALL*

A *RECALL* cycle is performed when $\overline{E}$, $\overline{G}$ and $\overline{NE}$ are low and $\overline{W}$ is high. Like the *STORE* cycle, *RECALL* is initiated when the last of the four clock signals goes to the *RECALL* state. Once initiated, the *RECALL* cycle will take t_{NLQX} to complete, during which all inputs are ignored. When the *RECALL* completes, any READ or WRITE state on the input pins will take effect.

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

As with the *STORE* cycle, a transition must occur on any one control pin to cause a *RECALL*, preventing inadvertent multi-triggering. On power up, once V_{CC} exceeds the V_{CC} sense voltage of 4.25V, a *RECALL* cycle is automatically initiated. Due to this automatic *RECALL*, SRAM operation cannot commence until $t_{RESTORE}$ after V_{CC} exceeds approximately 4.25V.

POWER-UP *RECALL*

During power up, or after any low-power condition (V_{CC} < 3.0V), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of 4.25V, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK10C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

HARDWARE PROTECT

The STK10C68 offers two levels of protection to suppress inadvertent *STORE* cycles. If the control signals ($\overline{E}$, $\overline{G}$, $\overline{W}$ and $\overline{NE}$) remain in the *STORE* condition at the end of a *STORE* cycle, a second *STORE* cycle will not be started. The *STORE* (or *RECALL*) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, *STORE*s are inhibited when V_{CC} is below 4.0V, protecting against inadvertent *STORE*s.

LOW AVERAGE ACTIVE POWER

The STK10C68 draws significantly less current when it is cycled at times longer than 55ns. Figure 2 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK10C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

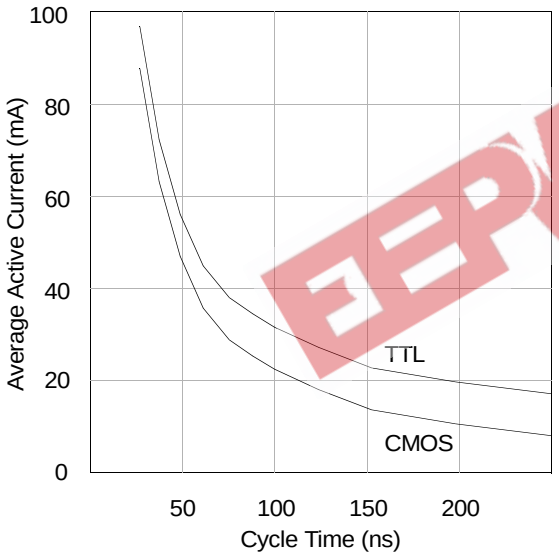


Figure 2: I_{CC} (max) Reads

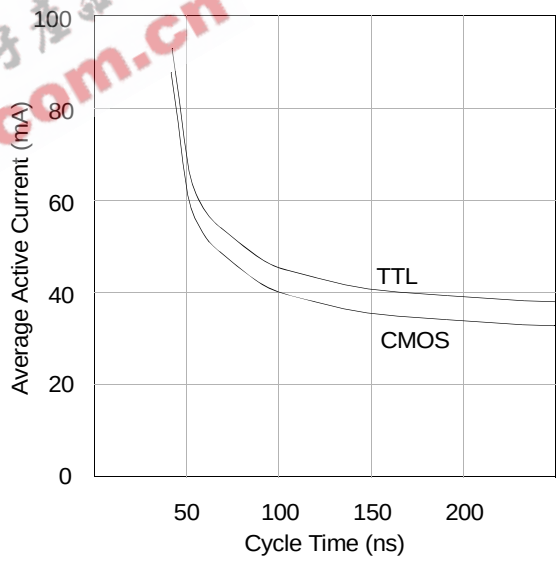


Figure 3: I_{CC} (max) Writes

ORDERING INFORMATION

STK10C68 - 5 P F 45 I

Temperature Range
Blank = Commercial (0 to 70°C)
I = Industrial (–40 to 85°C)
M = Military (–55 to 125°C)

Access Time
25 = 25ns
35 = 35ns
45 = 45ns
55 = 55ns (Military only)

Lead Finish (Plastic only)
Blank = 85%Sn/15%Pb
F = 100% Sn (Matte Tin)

Package
P = Plastic 28-pin 300 mil DIP
S = Plastic 28-pin 350 mil SOIC
C = Ceramic 28-pin 300 mil DIP (gold lead finish)
K = Ceramic 28-pin 300 mil DIP (solder dip finish)
L = Ceramic 28 pin LCC

Retention / Endurance
Blank = Comm/Ind (100 years/10^6cycles)
5 = Military (10 years/10^5cycles)

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Lead Finish
A = Solder DIP lead finish
C = Gold lead DIP finish
X = Lead finish “A” or “C” is acceptable

Package
MX = Ceramic 28 pin 300-mil DIP
MY = Ceramic 28 pin LCC

Access Time
04 = 55ns
05 = 45ns
06 = 35ns

Document Revision History

Revision	Date	Summary
0.0	December 2002	Combined commercial, industrial and military data sheets. Removed 20 nsec device.
0.1	September 2003	Added lead-free lead finish
0.2	March 2006	Marked as Obsolete, Not recommended for new design.