

524,288 WORD X 8 BIT DYNAMIC RAM

DESCRIPTION

The TC514800AJLL/AFTLL is the new generation dynamic RAM organized 524,288 word by 8 bit. The TC514800AJLL/AFTLL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514800AJLL/AFTLL to be packaged in a standard 28 pin plastic SOJ, and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of $5V \pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 524,288 word by 8 bit organization
- Fast access time and cycle time
- Single power supply of $5V \pm 10\%$ with a built-in V_{BB} generator
- Low Power
 - 578mW MAX. Operating (TC514800AJLL/AFTLL-70)
 - 495mW MAX. Operating (TC514800AJLL/AFTLL-80)
 - 1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, \overline{CAS} before \overline{RAS} refresh, \overline{RAS} -only refresh, Hidden refresh, Self Refresh
- Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514800AJLL : SOJ28-P-400
TC514800AFTLL : TSOP28-P-400

KEY PARAMETERS

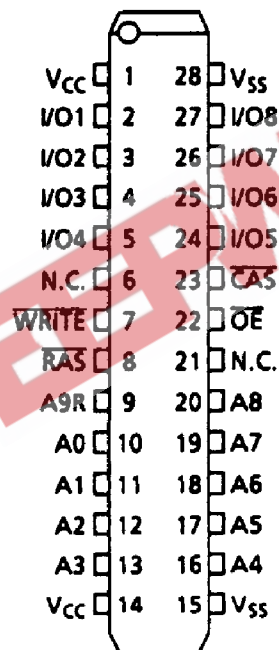
ITEM	TC514800AJLL/AFTLL	
	-70	-80
t_{RAC} \overline{RAS} Access Time	70ns	80ns
t_{AA} Column Address Access Time	35ns	40ns
t_{CAC} \overline{CAS} Access Time	20ns	20ns
t_{RC} Cycle Time	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

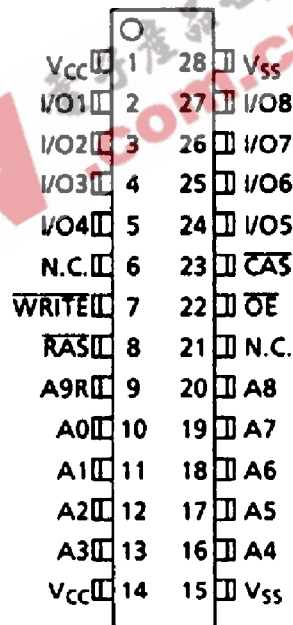
A0~A8, A9R	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WRITE	Read/Write Input
OE	Output Enable
I/O1~I/O8	Data Input/Output
V _{CC}	Power (+5V)
V _{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

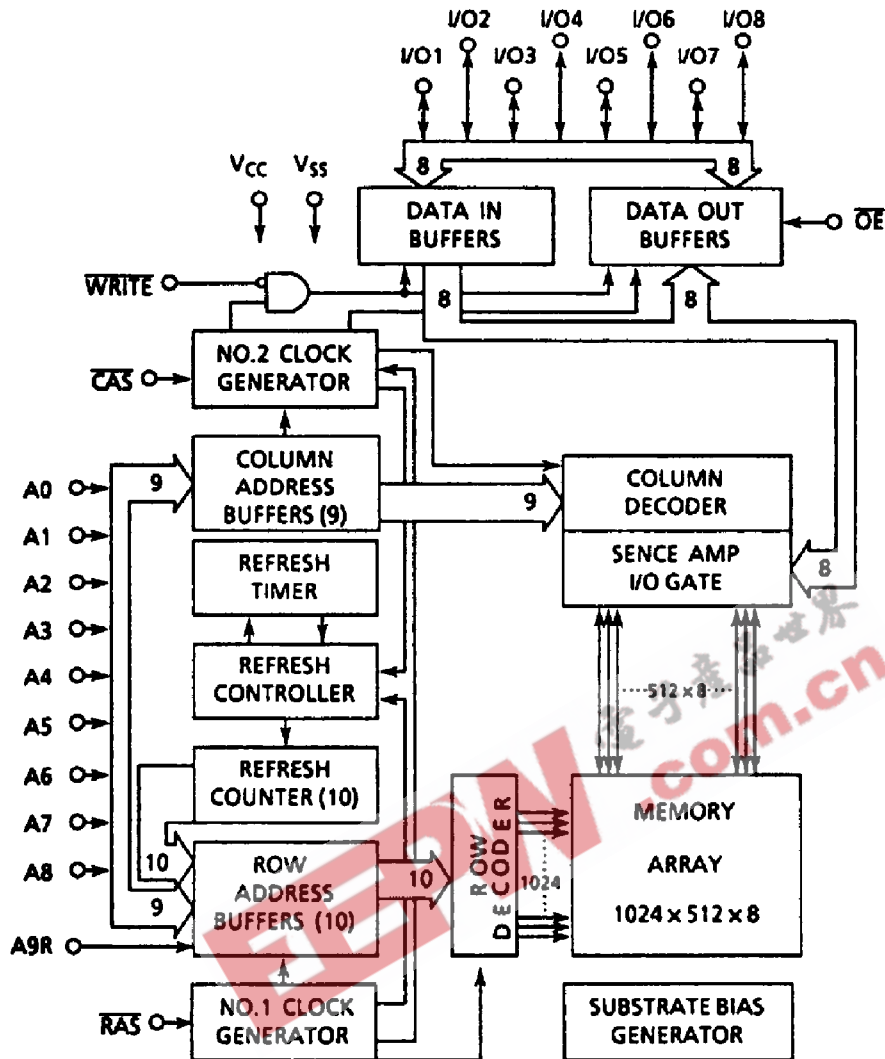
Plastic SOJ



Plastic TSOP
(Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V _{IH}	Input High Voltage	2.4	-	6.5	V	2
V _{IL}	Input Low Voltage (A0~A8, A9R, RAS, CAS, WRITE, OE)	-1.0*1	-	0.8	V	2
V _{IL}	Input Low Voltage (I/O1~I/O8)	-0.5*2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns

*2 -2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX	UNIT	NOTE	
I _{CC1}	OPERATING CURRENT Average Power Supply Operating Current (RAS, CAS, Address Cycling: t _{RC} =t _{RC} MIN.)	TC514800AJLL/AFTL-70	-	105	mA	3,4 5
		TC514800AJLL/AFTL-80	-	90		
I _{CC2}	STANDBY CURRENT Power Supply Standby Current (RAS=CAS=V _{IH})			2	mA	
I _{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS=V _{IH} : t _{RC} =t _{RC} MIN.)	TC514800AJLL/AFTL-70	-	105	mA	3, 5
		TC514800AJLL/AFTL-80	-	90		
I _{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode (RAS =V _{IL} , CAS, Address Cycling: t _{PC} =t _{PC} MIN.)	TC514800AJLL/AFTL-70	-	75	mA	3,4 5
		TC514800AJLL/AFTL-80	-	65		
I _{CC5}	STANDBY CURRENT Power Supply Standby Current (RAS=CAS=V _{CC} -0.2V)			200	μA	
I _{CC6}	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, CAS Before RAS Mode (RAS, CAS, Cycling: t _{RC} =t _{RC} MIN.)	TC514800AJLL/AFTL-70	-	105	mA	3
		TC514800AJLL/AFTL-80	-	90		
I _{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery Back Up Mode (RAS=CAS Before RAS Cycling or 0.2V, OE=V _{CC} -0.2V or 0.2V WRITE =V _{CC} -0.2V or 0.2V, A0~A8, A9R=V _{CC} -0.2V or 0.2V, I/O~I/O8=V _{CC} -0.2V, 0.2V or OPEN: t _{RC} =125μs, t _{RAS} =t _{RAS} MIN. ~1μs)			300	μA	3,6
I _{CC8}	SELF REFRESH CURRENT Average Power Supply Current, Self Refresh Mode (RAS=CAS=V _{IL} , WRITE=V _{CC} -0.2V or 0.2V, OE=V _{CC} -0.2V or 0.2V A0~8=V _{CC} -0.2V or 0.2V, I/O1~8=V _{CC} -0.2V, 0.2V or OPEN)			200	μA	
I _{I(L)}	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V _{IN} ≤ 0.5V, All Other Pins Not Under Test=0V)			-10	10	μA
I _{O(L)}	OUTPUT LEAKAGE CURRENT (D _{OUT} is disabled, (0V ≤ V _{OUT} ≤ 5.5V),			-10	10	μA
V _{OH}	OUTPUT LEVEL Output "H" Level Voltage (I _{OUT} =-5mA)			2.4	-	V
V _{OL}	OUTPUT LEVEL Output "L" Level Voltage (I _{OUT} =4.2mA)			-	0.4	V

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS
(V_{CC} = 5V ± 10%, T_a = 0~70°C)(Notes 7,8,9)

SYMBOL	PARAMETER	TC514800AJLL/AFTLL				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t _{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t _{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t _{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t _{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t _{RAC}	Access Time from RAS	-	70	-	80	ns	10,15,16
t _{CAC}	Access Time from CAS	-	20	-	20	ns	10,15
t _{AA}	Access Time from Column Address	-	35	-	40	ns	10,16
t _{CPA}	Access Time from CAS Precharge	-	40	-	45	-	10
t _{CLZ}	CAS to Output in Low-Z	0	-	0	-	ns	10
t _{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t _T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t _{RP}	RAS Presharge Time	50	-	60	-	ns	
t _{RAS}	RAS Pulse Width	70	10,000	80	10,000	ns	
t _{RASP}	RAS Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t _{RSH}	RAS Hold Time	20	-	20	-	ns	
t _{RHCP}	RAS Hold Time From CAS Precharge (Fast Page Mode)	40	-	45	-	ns	
t _{CSH}	CAS Hold Time	70	-	80	-	ns	
t _{CAS}	CAS Pulse Width	20	10,000	20	10,000	ns	
t _{RCD}	RAS to CAS Delay Time	20	50	20	60	ns	15
t _{RAD}	RAS to Column Address Delay Time	15	35	15	40	ns	16
t _{CRP}	CAS to RAS Precharge Time	5	-	5	-	ns	
t _{CP}	CAS Precharge Time	10	-	10	-	ns	
t _{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t _{RAH}	Row Address Hold Time	10	-	10	-	ns	
t _{ASC}	Column Address Set-Up Time	0	-	0	0	ns	
t _{CAH}	Column Address Hold Time	15	-	15	-	ns	
t _{AR}	Column Address Hold Time referenced to RAS	55	-	60	-	ns	
t _{RAL}	Column Address To RAS Lead Time	35	-	40	-	ns	
t _{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t _{RCH}	Read Command Hold Time	0	-	0	-	ns	12
t _{RRH}	Read Command Hold Time referenced to RAS	0	-	0	-	ns	12
t _{WCH}	Write Command Hold Time	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514400AJLL/AFTLL				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WCR}	Write Command Hold Time referenced RAS	55	-	60	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to RAS Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to CAS Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	15	-	ns	13
t_{DHR}	Data Hold Time referenced to RAS	55	-	60	-	ns	
t_{REF}	Refresh Period	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	CAS to WRITE Delay Time	50	-	50	-	ns	14
t_{RWD}	RAS to WRITE Delay Time	100	-	110	-	ns	14
t_{AWD}	Column Address to WRITE Delay Time	65	-	70	-	ns	14
t_{CPWD}	CAS Precharge to WRITE Delay Time	70	-	75	-	ns	14
t_{CSR}	CAS Set-up Time (CAS before RAS Cycle)	5	-	5	-	ns	
t_{CHR}	CAS Hold Time (CAS before RAS Cycle)	15	-	15	-	ns	
t_{RPC}	RAS to CAS Precharge Time	0	-	0	-	ns	
t_{CPT}	CAS Precharge Time (CAS before RAS Counter Test Cycle)	40	-	40	-	ns	
t_{ROH}	RAS Hold Time referenced to \overline{OE}	10	-	10	-	ns	
t_{OEA}	\overline{OE} Access Time	-	20	-	20	ns	10
t_{OED}	\overline{OE} to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from \overline{OE}	0	20	0	20	ns	11
t_{OEH}	\overline{OE} Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{RASS}	RAS Pulse Width (CAS before RAS Self Refresh)	100	-	100	-		
t_{RPS}	RAS Precharge Time (CAS before RAS Self Refresh)	130	-	150	-	ns	
t_{CHS}	CAS Hold time (CAS before RAS Self Refresh)	-50	-	-60	-	ns	

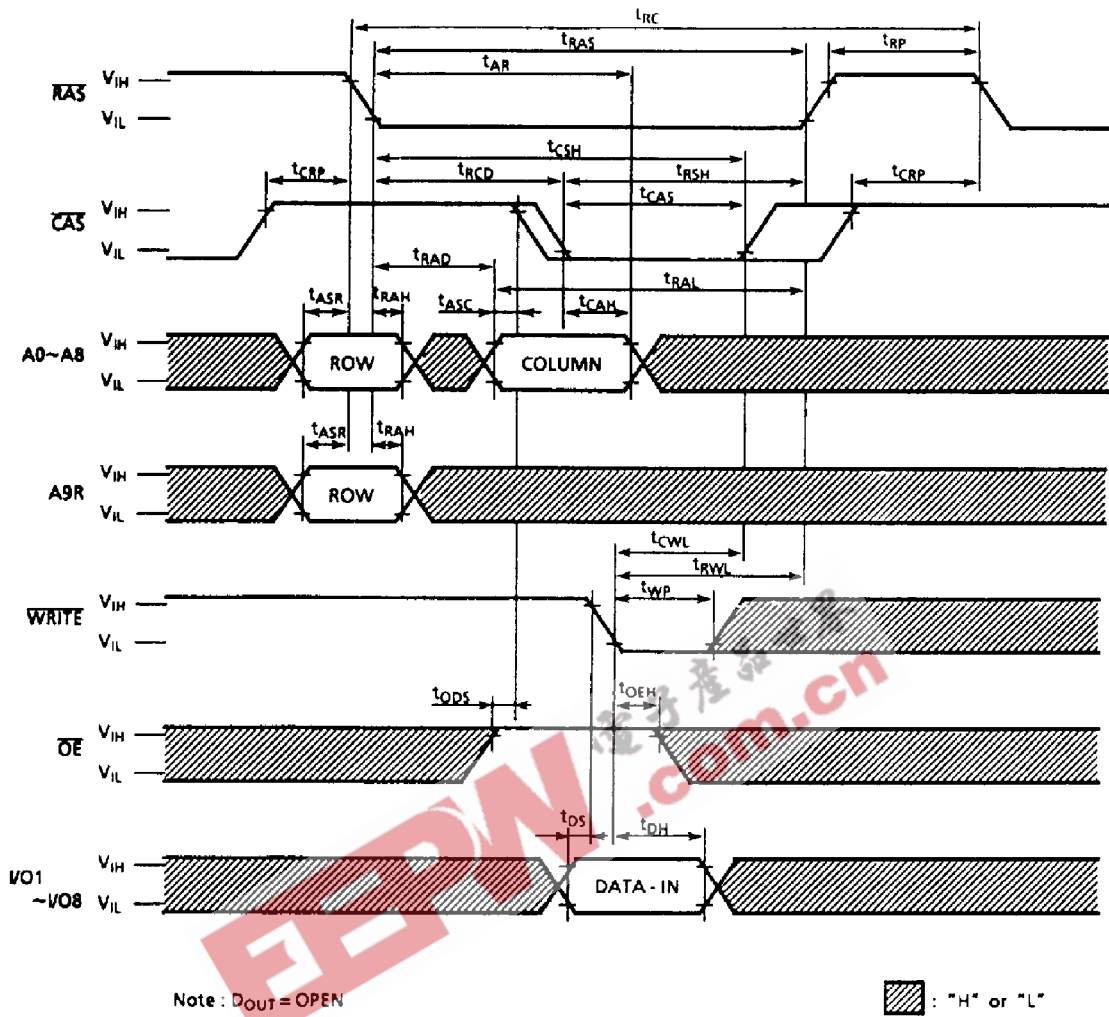
CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $f = 1MHz$, $T_a = 0\sim 70^\circ C$)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8, A9R)	-	5	pF
C_{I2}	Input Capacitance (RAS, CAS, WRITE, OE)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O8)	-	7	pF

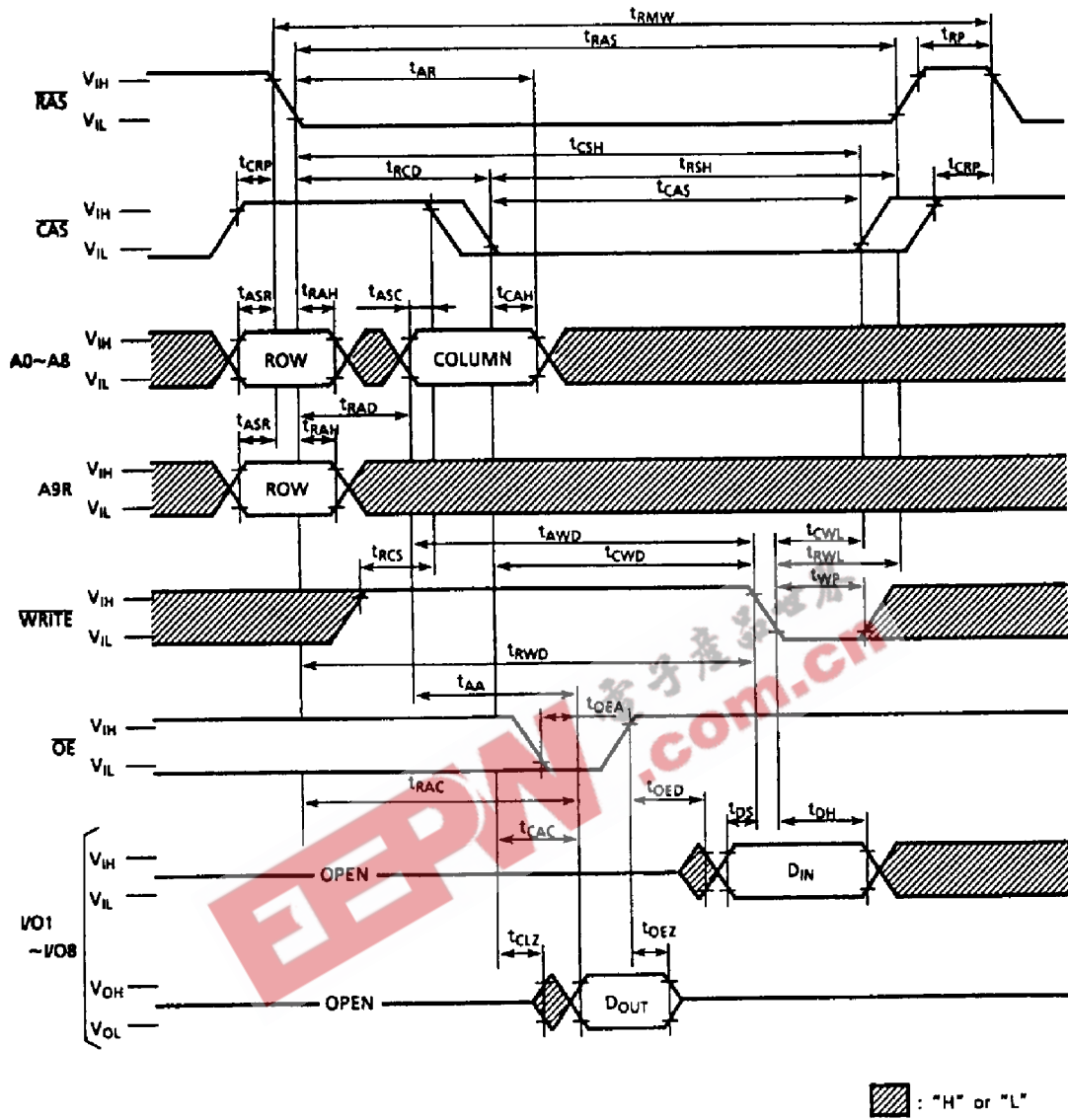
NOTES:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- All voltages are referenced to V_{SS} .
- I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} depend on cycle rate.
- I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
- Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4} , it can be changed once or less during a fast page mode cycle (t_{PC}).
- $t_{RAS(max.)}=1\mu s$ is only applied to refresh of battery-back up. $t_{RAS(max.)}=10\mu s$ is applied to functional operating.
- An initial pause of $200\mu s$ is required after power-up followed by 8 RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS before \overline{RAS} refresh cycles instead 8 RAS only refresh cycles are required.
- AC measurements assume $t_T=5ns$.
- V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Measured with a load equivalent to 2 TTL loads and 100pF.
- t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to \overline{CAS} leading edge in early write cycles and to WRITE leading edge in Read-Modify-Write cycles.
- t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWD} > t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condition is satisfied, the condition of the data out (at access time) is indeterminate.
- Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC} .
- Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA} .

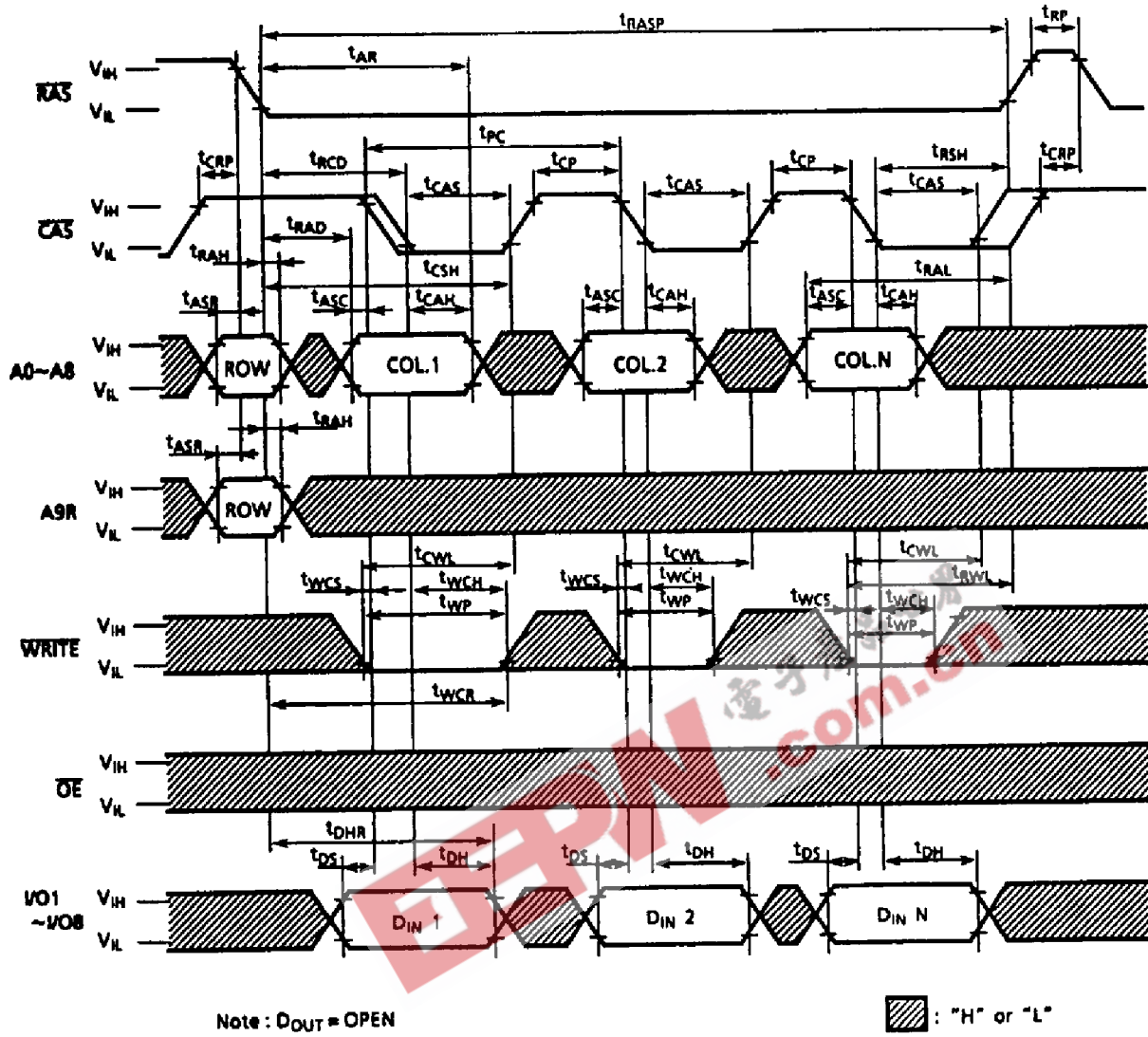
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



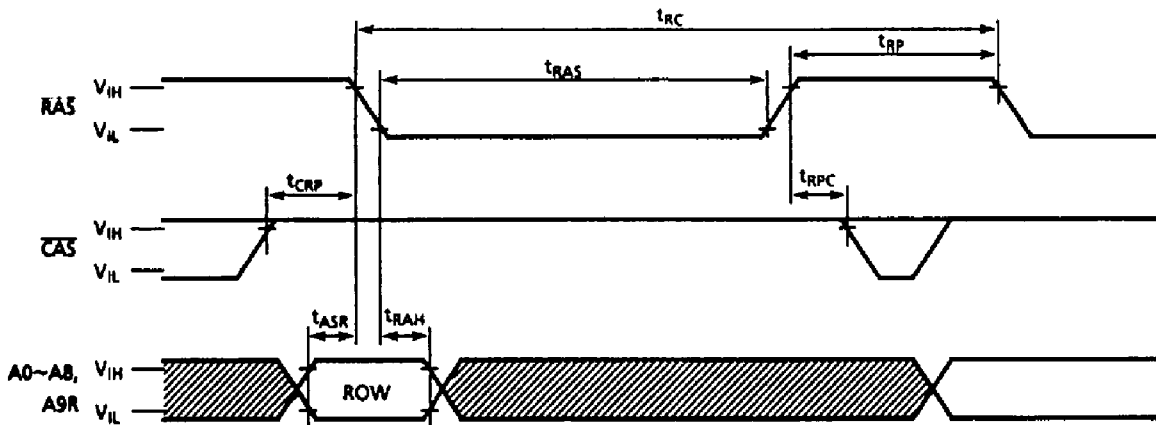
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE WRITE CYCLE



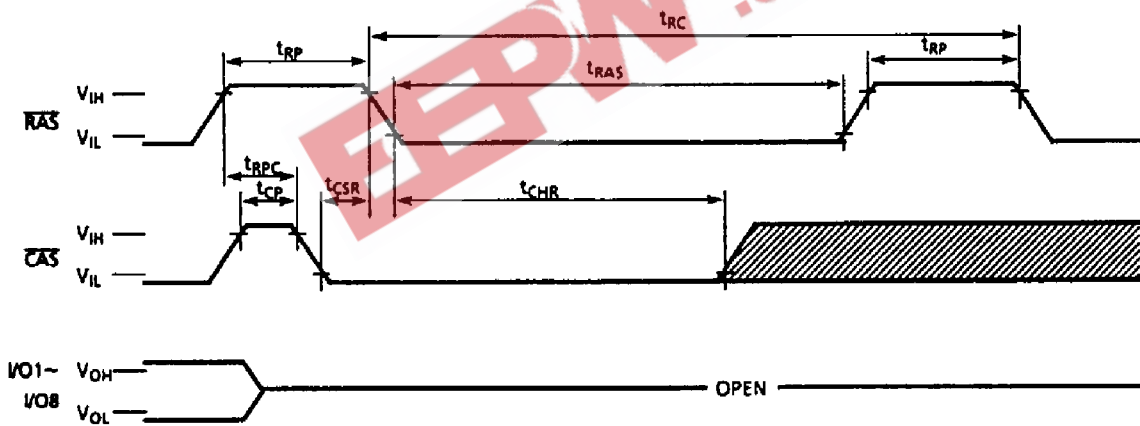
RAS ONLY REFRESH CYCLE



Note: WRITE, \overline{OE} , D_{IN} = "H" or "L"
 D_{OUT} = OPEN

▨ : "H" or "L"

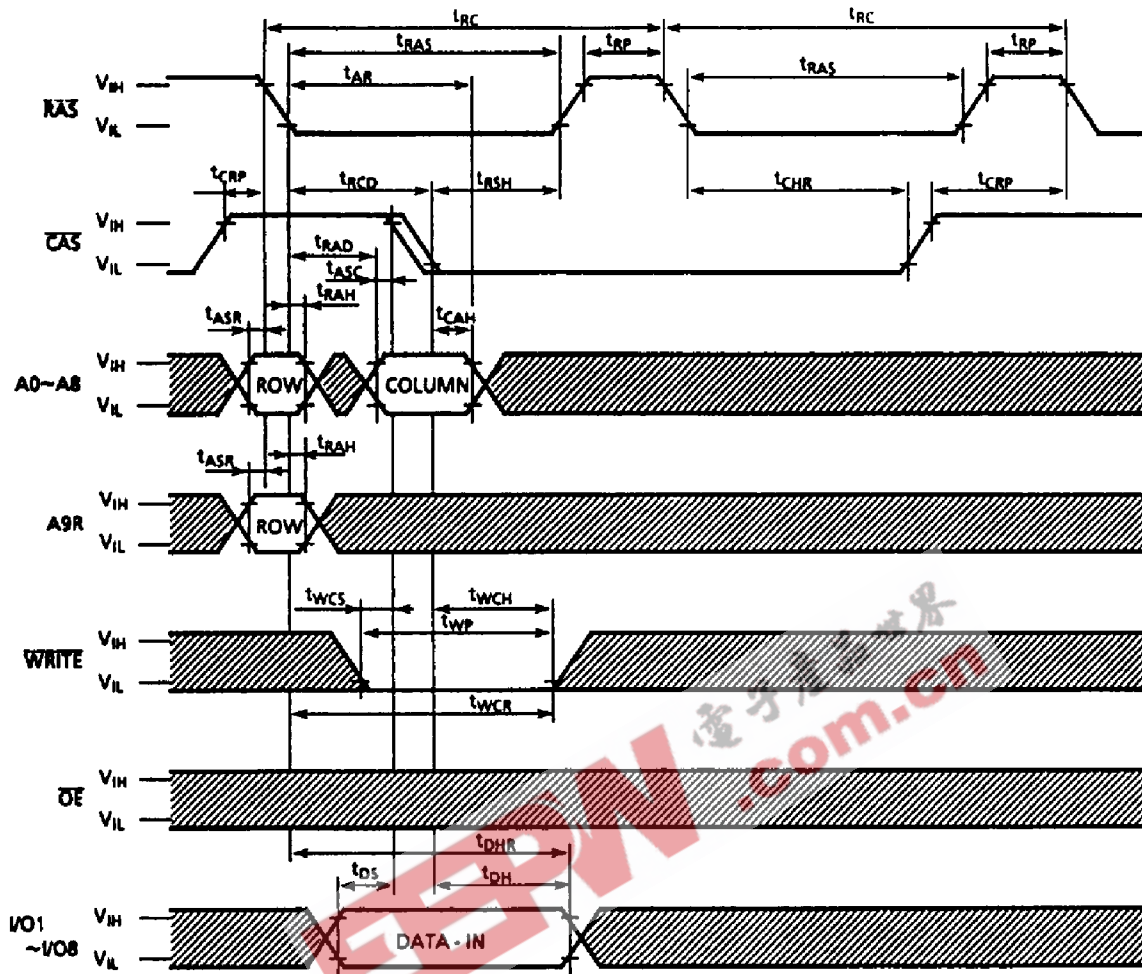
CAS BEFORE RAS REFRESH CYCLE



Note: D_{IN} , WRITE, \overline{OE} , A0~A8, A9R = "H" or "L"

▨ : "H" or "L"

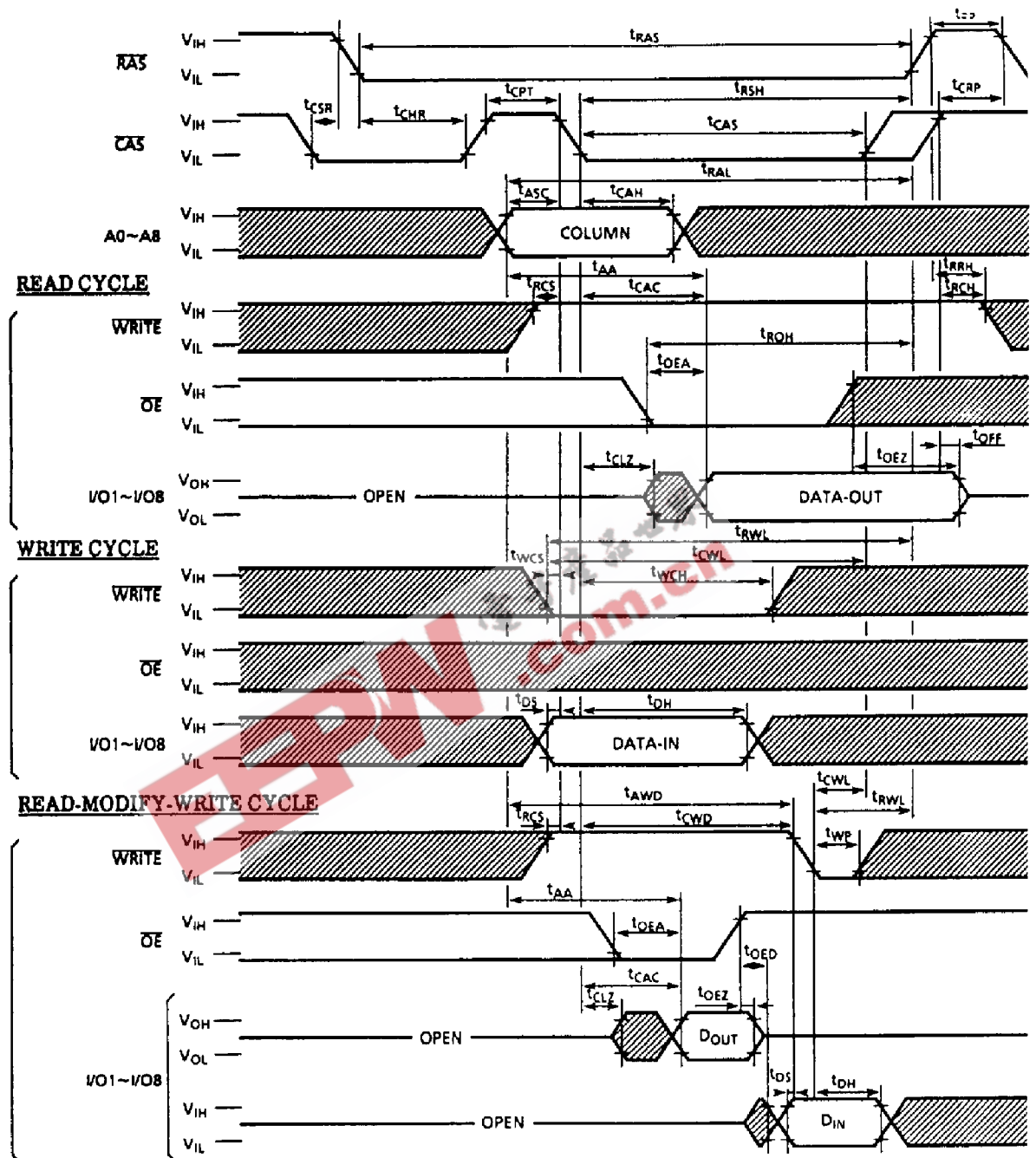
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



Note: A9R = "H" or "L"

▨ : "H" or "L"