

ABSOLUTE MAXIMUM RATINGS^a

Voltage on Input Relative to Ground	-0.5V to 7.0V
Voltage on Input Relative to V _{SS}	-0.6V to (V _{CC} + 0.5V)
Voltage on DQ ₀₋₇	-0.5V to (V _{CC} + 0.5V)
Temperature under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Power Dissipation	1W
DC Output Current (1 output at a time, 1s duration)	15mA

Note a: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I _{CC1} ^b	Average V _{CC} Current		85		90	mA	t _{AVAV} = 25ns t _{AVAV} = 35ns t _{AVAV} = 45ns
			75		75	mA	
			65		65	mA	
I _{CC2} ^c	Average V _{CC} Current during STORE		3		3	mA	All Inputs Don't Care, V _{CC} = max
I _{CC3} ^b	Average V _{CC} Current at t _{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\bar{V} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I _{SB1} ^d	Average V _{CC} Current (Standby, Cycling TTL Input Levels)		25		26	mA	t _{AVAV} = 25ns, $\bar{E} \geq V_{IH}$ t _{AVAV} = 35ns, $\bar{E} \geq V_{IH}$ t _{AVAV} = 45ns, $\bar{E} \geq V_{IH}$
			21		22	mA	
			18		19	mA	
I _{SB2} ^d	V _{CC} Standby Current (Standby, Stable CMOS Input Levels)		750		750	μA	$\bar{E} \geq (V_{CC} - 0.2V)$ All Others V _{IN} ≤ 0.2V or ≥ (V _{CC} - 0.2V)
I _{ILK}	Input Leakage Current		±1		±1	μA	V _{CC} = max V _{IN} = V _{SS} to V _{CC}
I _{OLK}	Off-State Output Leakage Current		±5		±5	μA	V _{CC} = max V _{IN} = V _{SS} to V _{CC} , \bar{E} or $\bar{G} \geq V_{IH}$
V _{IH}	Input Logic “1” Voltage	2.2	V _{CC} + .5	2.2	V _{CC} + .5	V	All Inputs
V _{IL}	Input Logic “0” Voltage	V _{SS} - .5	0.8	V _{SS} - .5	0.8	V	All Inputs
V _{OH}	Output Logic “1” Voltage	2.4		2.4		V	I _{OUT} = -4mA
V _{OL}	Output Logic “0” Voltage		0.4		0.4	V	I _{OUT} = 8mA
T _A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.

Note c: I_{CC2} is the average current required for the duration of the STORE cycle (t_{STORE}).

Note d: $\bar{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE^e (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C _{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C _{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

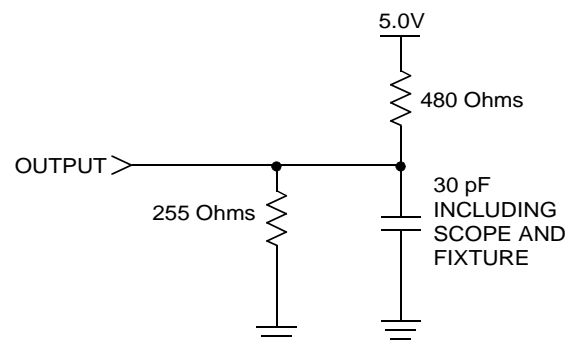


Figure 1: AC Output Loading

SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

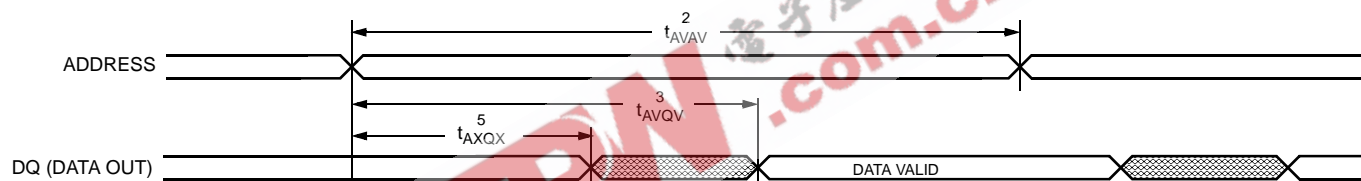
NO.	SYMBOLS		PARAMETER	STK11C48-25		STK11C48-35		STK11C48-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t _{ELQV}	t _{ACS}	Chip Enable Access Time		25		35		45	ns
2	t _{AVAV} ^f	t _{RC}	Read Cycle Time	25		35		45		ns
3	t _{AVQV} ^g	t _{AA}	Address Access Time		25		35		45	ns
4	t _{GLQV}	t _{OE}	Output Enable to Data Valid		10		15		20	ns
5	t _{AXQX} ^g	t _{OH}	Output Hold after Address Change	5		5		5		ns
6	t _{ELQX}	t _{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t _{EHQZ} ^h	t _{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t _{GLQX}	t _{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t _{GHQZ} ^h	t _{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t _{ELICCH} ^e	t _{PA}	Chip Enable to Power Active	0		0		0		ns
11	t _{EHICCL} ^{d, e}	t _{PS}	Chip Disable to Power Standby		25		35		45	ns

Note f: \bar{W} must be high during SRAM READ cycles and low during SRAM WRITE cycles.

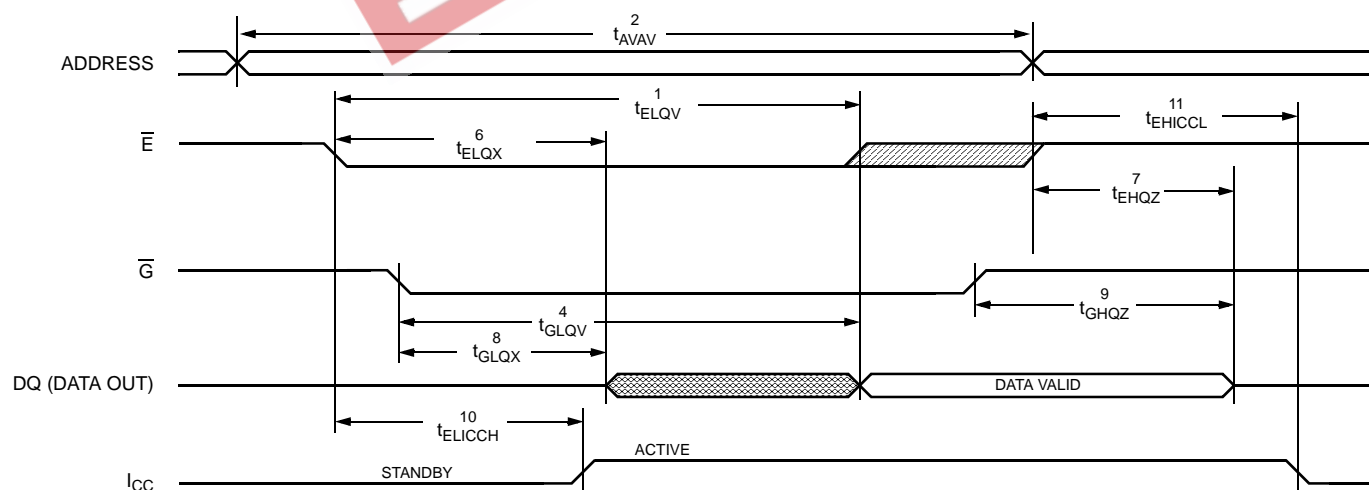
Note g: I/O state assumes $\bar{E}, \bar{G} < V_{IL}$ and $\bar{W} > V_{IH}$; device is continuously selected.

Note h: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled^{f, g}



SRAM READ CYCLE #2: \bar{E} Controlled^f



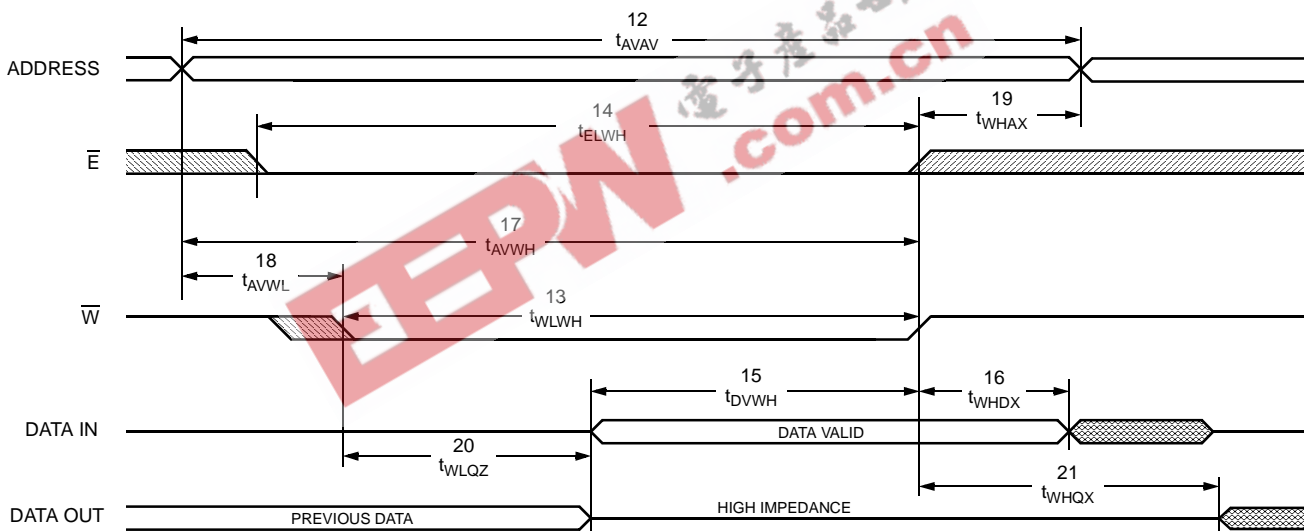
SRAM WRITE CYCLES #1 & #2

($V_{CC} = 5.0V \pm 10\%$)

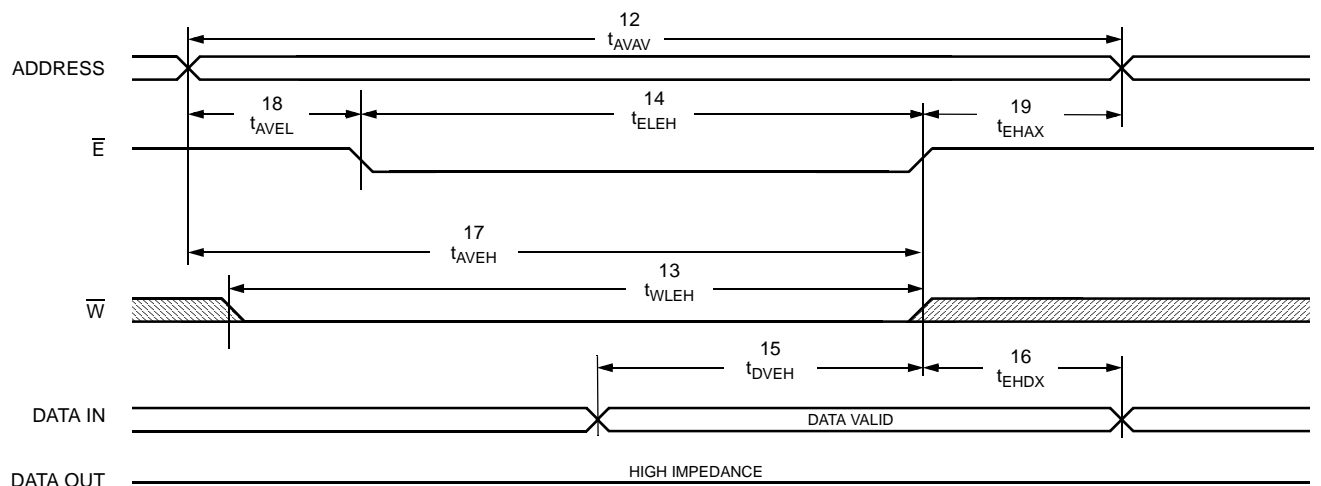
NO.	SYMBOLS			PARAMETER	STK11C48-25		STK11C48-35		STK11C48-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	$t_{WLQZ}^{h,i}$		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		ns

Note i: If \bar{W} is low when \bar{E} goes low, the outputs remain in the high-impedance state.
 Note j: \bar{E} or \bar{W} must be $\geq V_{IH}$ during address transitions.

SRAM WRITE CYCLE #1: \bar{W} Controlled^j



SRAM WRITE CYCLE #2: \bar{E} Controlled^j



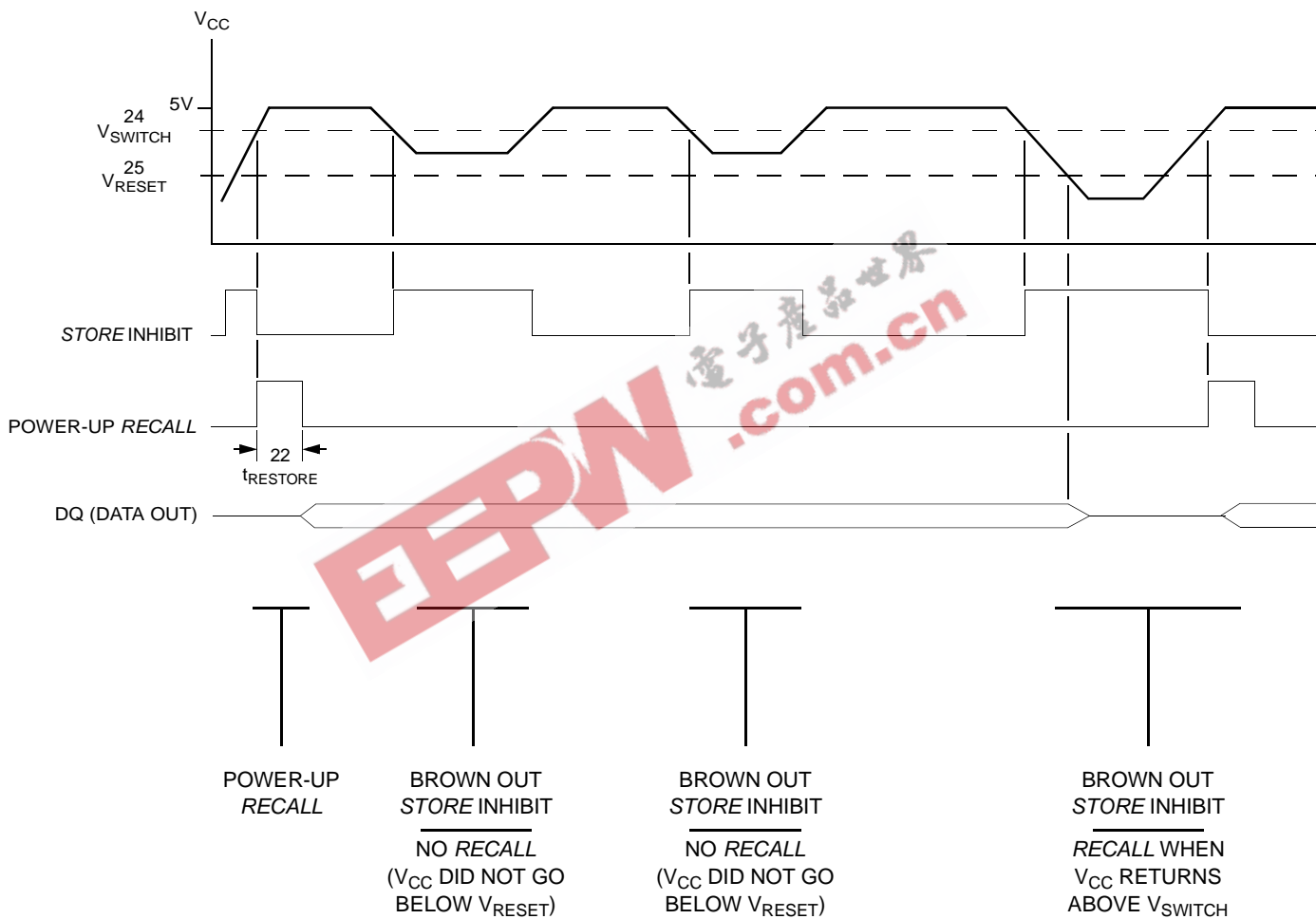
STORE INHIBIT/POWER-UP RECALL

($V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOLS	PARAMETER	STK11C48		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-up <i>RECALL</i> Duration		550	μs	k
23	t_{STORE}	<i>STORE</i> Cycle Duration		10	ms	
24	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
25	V_{RESET}	Low Voltage Reset Level		3.6	V	

Note k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH} .

STORE INHIBIT/POWER-UP RECALL



SOFTWARE STORE/RECALL MODE SELECTION

\bar{E}	\bar{W}	A ₁₀ - A ₀ (hex)	MODE	I/O	NOTES
L	H	000	Read SRAM	Output Data	I
		555	Read SRAM	Output Data	
		2AA	Read SRAM	Output Data	
		7FF	Read SRAM	Output Data	
		0F0	Read SRAM	Output Data	
		70F	Nonvolatile STORE	Output High Z	
L	H	000	Read SRAM	Output Data	I
		555	Read SRAM	Output Data	
		2AA	Read SRAM	Output Data	
		7FF	Read SRAM	Output Data	
		0F0	Read SRAM	Output Data	
		70E	Nonvolatile RECALL	Output High Z	

Note I: The six consecutive addresses must be in the order listed. \bar{W} must be high during all six consecutive cycles to enable a nonvolatile cycle.

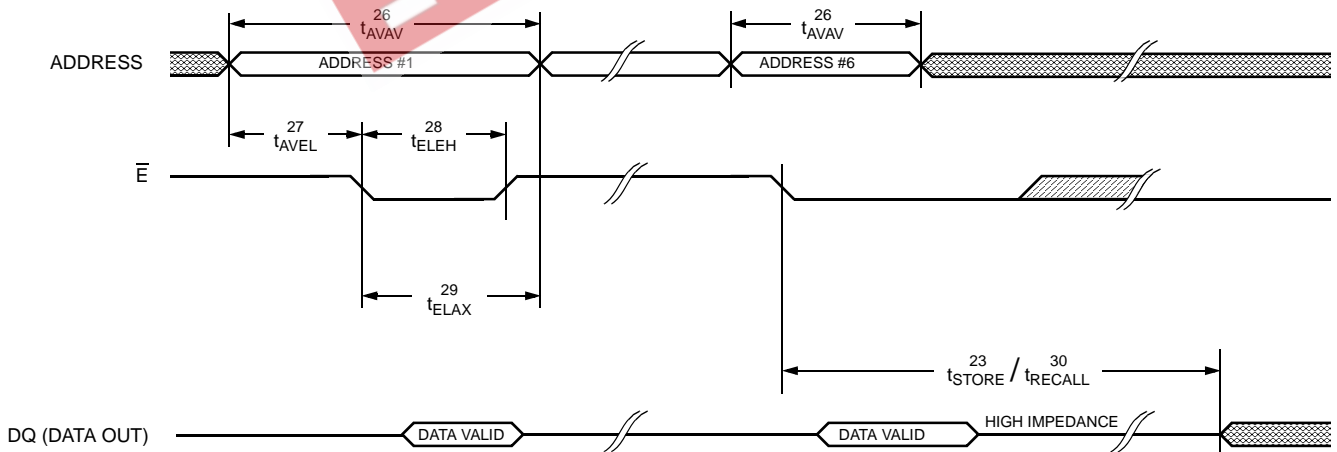
SOFTWARE STORE/RECALL CYCLE^{m, n} (V_{CC} = 5.0V ± 10%)^b

NO.	SYMBOLS	PARAMETER	STK11C48-25		STK11C48-35		STK11C48-45		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
26	t _{AVAV}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
27	t _{AVEL} ^m	Address Set-up Time	0		0		0		ns
28	t _{ELEH} ^m	Clock Pulse Width	20		25		30		ns
29	t _{ELAX} ^m	Address Hold Time	20		20		20		ns
30	t _{RECALL} ^m	RECALL Duration		20		20		20	μs

Note m: The software sequence is clocked with \bar{E} controlled reads.

Note n: The six consecutive addresses must be in the order listed in the Software STORE/RECALL Mode Selection Table: (000, 555, 2AA, 7FF, 0F0, 70F) for a STORE cycle or (000, 555, 2AA, 7FF, 0F0, 70E) for a RECALL cycle. \bar{W} must be high during all six consecutive cycles.

SOFTWARE STORE/RECALL CYCLE: \bar{E} Controlledⁿ



DEVICE OPERATION

The STK11C48 is a versatile memory chip that provides several modes of operation. The STK11C48 can operate as a standard 8K x 8 SRAM. It has an 8K x 8 Nonvolatile Elements shadow to which the SRAM information can be copied or from which the SRAM can be updated in nonvolatile mode.

NOISE CONSIDERATIONS

Note that the STK11C48 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 μ F connected between V_{CC} and V_{SS} , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK11C48 performs a READ cycle whenever \bar{E} and \bar{G} are low and \bar{W} is high. The address specified on pins A_{0-10} determines which of the 2,048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by \bar{E} or \bar{G} , the outputs will be valid at t_{ELQV} or at t_{GLQV} , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until \bar{E} or \bar{G} is brought high.

SRAM WRITE

A WRITE cycle is performed whenever \bar{E} and \bar{W} are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either \bar{E} or \bar{W} goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a \bar{W} controlled WRITE or t_{DVEH} before the end of an \bar{E} controlled WRITE.

It is recommended that \bar{G} be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If \bar{G} is left low, internal circuitry will turn off the output buffers t_{WLQZ} after \bar{W} goes low.

SOFTWARE NONVOLATILE STORE

The STK11C48 software STORE cycle is initiated by executing sequential READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1.	Read address	000 (hex)	Valid READ
2.	Read address	555 (hex)	Valid READ
3.	Read address	2AA (hex)	Valid READ
4.	Read address	7FF (hex)	Valid READ
5.	Read address	0F0 (hex)	Valid READ
6.	Read address	70F (hex)	Initiate STORE cycle

The software sequence must be clocked with \bar{E} controlled READs.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that \bar{G} be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of READ operations must be performed:

1.	Read address	000 (hex)	Valid READ
2.	Read address	555 (hex)	Valid READ
3.	Read address	2AA (hex)	Valid READ
4.	Read address	7FF (hex)	Valid READ
5.	Read address	0F0 (hex)	Valid READ
6.	Read address	70E (hex)	Initiate RECALL cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the Nonvolatile Element cells. The nonvolatile data can be recalled an unlimited number of times.

POWER-UP RECALL

During power up, or after any low-power condition ($V_{CC} < V_{RESET}$), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH} , a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK11C48 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between \bar{W} and system V_{CC} or between \bar{E} and system V_{CC} .

HARDWARE PROTECT

The STK11C48 offers hardware protection against inadvertent *STORE* operation during low-voltage conditions. When $V_{CC} < V_{SWITCH}$, all software *STORE* operations are inhibited.

LOW AVERAGE ACTIVE POWER

The STK11C48 draws significantly less current when it is cycled at times longer than 50ns. Figure 2 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, $V_{CC} = 5.5V$, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK11C48 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READS to WRITES; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

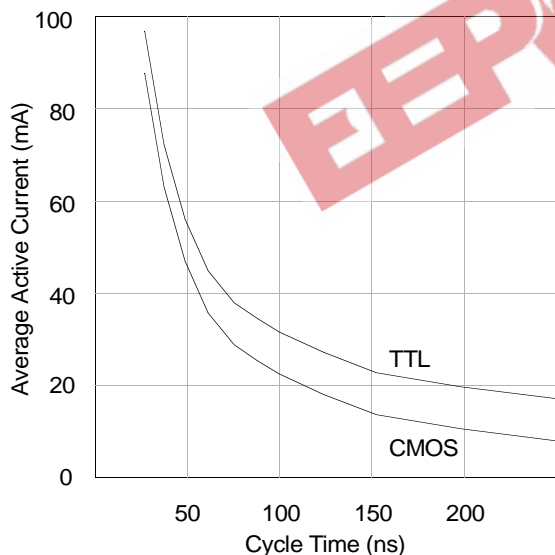


Figure 2: I_{CC} (max) Reads

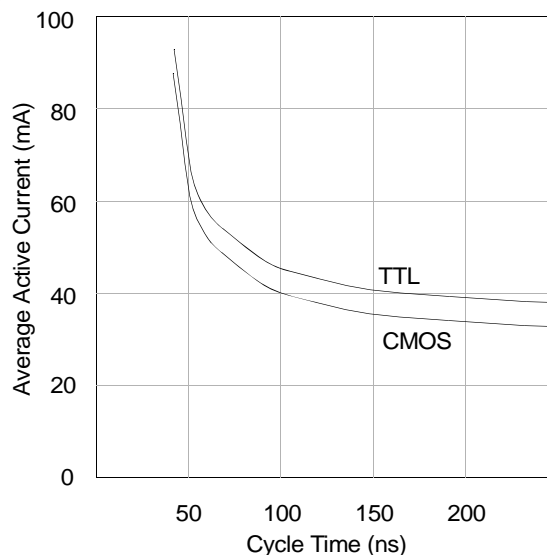
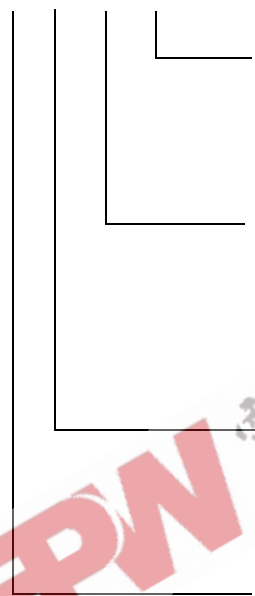


Figure 3: I_{CC} (max) Writes

ORDERING INFORMATION

STK11C48 - P F 45 I



Temperature Range

Blank = Commercial (0 to 70°C)

I = Industrial (-40 to 85°C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Lead Finish

Blank = 85%Sn/15%Pb

F = 100% Sn (Matte Tin)

Package

P = Plastic 28-pin 300 mil DIP

N = Plastic 28-pin 300 mil SOIC

S = Plastic 28-pin 350 mil SOIC

STK11C48

Document Revision History

Revision	Date	Summary
0.0	October 2002	Removed 20 nsec device.
0.1	September 2003	Added lead-free lead finish
0.2	March 2006	Marked as Obsolete, Not recommended for new design.

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