



# STK12C68

## STK12C68-M SMD#5962-94599

### 8K x 8 *AutoStore*<sup>™</sup> nvSRAM

### *QuantumTrap*<sup>™</sup> CMOS

### Nonvolatile Static RAM

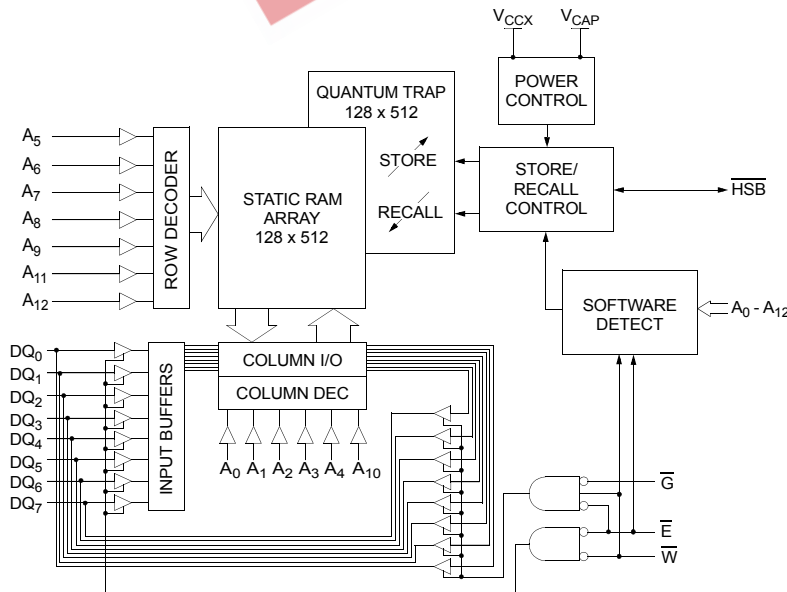
#### FEATURES

- 25ns, 35ns, 45ns and 55ns Access Times
- “Hands-off” Automatic *STORE* with External 68μF Capacitor on Power Down
- *STORE* to Nonvolatile Elements Initiated by Hardware, Software or *AutoStore*<sup>™</sup> on Power Down
- *RECALL* to SRAM Initiated by Software or Power Restore
- 10mA Typical I<sub>CC</sub> at 200ns Cycle Time
- Unlimited READ, WRITE and *RECALL* Cycles
- 1,000,000 *STORE* Cycles to Nonvolatile Elements (Commercial/Industrial)
- 100-Year Data Retention in Nonvolatile Elements (Commercial/Industrial)
- Commercial, Industrial and Military Temperatures
- 28-Pin SOIC, DIP and LCC Packages

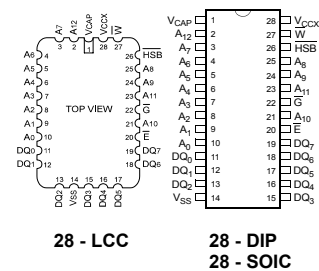
#### DESCRIPTION

The Simtek STK12C68 is a fast static RAM with a nonvolatile element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, non-volatile data resides in Nonvolatile Elements. Data transfers from the SRAM to the Nonvolatile Elements (the *STORE* operation) can take place automatically on power down. A 68μF or larger capacitor tied from V<sub>CAP</sub> to ground guarantees the *STORE* operation, regardless of power-down slew rate or loss of power from “hot swapping”. Transfers from the Nonvolatile Elements to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of *STORE* and *RECALL* cycles can also be software controlled by entering specific read sequences. A hardware *STORE* may be initiated with the HSB pin.

#### BLOCK DIAGRAM



#### PIN CONFIGURATIONS



#### PIN NAMES

A <sub>0</sub> - A <sub>12</sub>	Address Inputs
DQ <sub>0</sub> - DQ <sub>7</sub>	Data In/Out
$\bar{E}$	Chip Enable
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
HSB	Hardware Store Busy (I/O)
V <sub>CCX</sub>	Power (+ 5V)
V <sub>CAP</sub>	Capacitor
V <sub>SS</sub>	Ground

# STK12C68

## ABSOLUTE MAXIMUM RATINGS<sup>a</sup>

Voltage on Input Relative to Ground . . . . . -0.5V to 7.0V  
 Voltage on Input Relative to V<sub>SS</sub> . . . . . -0.6V to (V<sub>CC</sub> + 0.5V)  
 Voltage on DQ<sub>0-7</sub> or HSB . . . . . -0.5V to (V<sub>CC</sub> + 0.5V)  
 Temperature under Bias . . . . . -55°C to 125°C  
 Storage Temperature . . . . . -65°C to 150°C  
 Power Dissipation . . . . . 1W  
 DC Output Current (1 output at a time, 1s duration) . . . . . 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ± 10%)<sup>e</sup>

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL/ MILITARY		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I <sub>CC1</sub> <sup>b</sup>	Average V <sub>CC</sub> Current		85		90	mA	t <sub>AVAV</sub> = 25ns t <sub>AVAV</sub> = 35ns t <sub>AVAV</sub> = 45ns t <sub>AVAV</sub> = 55ns
			75		75	mA	
			65		65	mA	
			55		55	mA	
I <sub>CC2</sub> <sup>c</sup>	Average V <sub>CC</sub> Current during STORE		3		3	mA	All Inputs Don't Care, V <sub>CC</sub> = max
I <sub>CC3</sub> <sup>b</sup>	Average V <sub>CC</sub> Current at t <sub>AVAV</sub> = 200ns 5V, 25°C, Typical		10		10	mA	$\bar{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I <sub>CC4</sub> <sup>c</sup>	Average V <sub>CAP</sub> Current during AutoStore™ Cycle		2		2	mA	All Inputs Don't Care
I <sub>SB1</sub> <sup>d</sup>	Average V <sub>CC</sub> Current (Standby, Cycling TTL Input Levels)		27		28	mA	t <sub>AVAV</sub> = 25ns, $\bar{E} \geq V_{IH}$ t <sub>AVAV</sub> = 35ns, $\bar{E} \geq V_{IH}$ t <sub>AVAV</sub> = 45ns, $\bar{E} \geq V_{IH}$ t <sub>AVAV</sub> = 55ns, $\bar{E} \geq V_{IH}$
			23		24	mA	
			20		21	mA	
			19		19	mA	
I <sub>SB2</sub> <sup>d</sup>	V <sub>CC</sub> Standby Current (Standby, Stable CMOS Input Levels)		1.5		2.5	mA	$\bar{E} \geq (V_{CC} - 0.2V)$ All Others V <sub>IN</sub> ≤ 0.2V or ≥ (V <sub>CC</sub> - 0.2V)
I <sub>ILK</sub>	Input Leakage Current		±1		±1	µA	V <sub>CC</sub> = max V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>OLK</sub>	Off-State Output Leakage Current		±5		±5	µA	V <sub>CC</sub> = max V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub> , $\bar{E}$ or $\bar{G} \geq V_{IH}$
V <sub>IH</sub>	Input Logic "1" Voltage	2.2	V <sub>CC</sub> + .5	2.2	V <sub>CC</sub> + .5	V	All Inputs
V <sub>IL</sub>	Input Logic "0" Voltage	V <sub>SS</sub> - .5	0.8	V <sub>SS</sub> - .5	0.8	V	All Inputs
V <sub>OH</sub>	Output Logic "1" Voltage	2.4		2.4		V	I <sub>OUT</sub> = -4mA except HSB
V <sub>OL</sub>	Output Logic "0" Voltage		0.4		0.4	V	I <sub>OUT</sub> = 8mA except HSB
V <sub>BL</sub>	Logic "0" Voltage on HSB Output		0.4		0.4	V	I <sub>OUT</sub> = 3mA
T <sub>A</sub>	Operating Temperature	0	70	-40/-55	85/125	°C	

Note b: I<sub>CC1</sub> and I<sub>CC3</sub> are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.  
 Note c: I<sub>CC2</sub> and I<sub>CC4</sub> are the average currents required for the duration of the respective STORE cycles (t<sub>STORE</sub>).  
 Note d:  $\bar{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out.  
 Note e: V<sub>CC</sub> reference levels throughout this datasheet refer to V<sub>CCX</sub> if that is where the power supply connection is made, or V<sub>CAP</sub> if V<sub>CCX</sub> is connected to ground.

## AC TEST CONDITIONS

Input Pulse Levels . . . . .	0V to 3V
Input Rise and Fall Times . . . . .	≤ 5ns
Input and Output Timing Reference Levels . . . . .	1.5V
Output Load . . . . .	See Figure 1

## CAPACITANCE<sup>f</sup> (T<sub>A</sub> = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C <sub>IN</sub>	Input Capacitance	8	pF	ΔV = 0 to 3V
C <sub>OUT</sub>	Output Capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.



Figure 1: AC Output Loading

SRAM READ CYCLES #1 & #2

(V<sub>CC</sub> = 5.0V ± 10%)<sup>e</sup>

NO.	SYMBOLS		PARAMETER	STK12C68-25		STK12C68-35		STK12C68-45		STK12C68-55		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t <sub>ELQV</sub>	t <sub>ACS</sub>	Chip Enable Access Time		25		35		45		55	ns
2	t <sub>AVAV</sub> <sup>g</sup>	t <sub>RC</sub>	Read Cycle Time	25		35		45		55		ns
3	t <sub>AVQV</sub> <sup>h</sup>	t <sub>AA</sub>	Address Access Time		25		35		45		55	ns
4	t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable to Data Valid		10		15		20		35	ns
5	t <sub>AXQX</sub> <sup>h</sup>	t <sub>OH</sub>	Output Hold after Address Change	5		5		5		5		ns
6	t <sub>ELQX</sub>	t <sub>LZ</sub>	Chip Enable to Output Active	5		5		5		5		ns
7	t <sub>EHQZ</sub> <sup>i</sup>	t <sub>HZ</sub>	Chip Disable to Output Inactive		10		10		12		12	ns
8	t <sub>GLQX</sub>	t <sub>OLZ</sub>	Output Enable to Output Active	0		0		0		0		ns
9	t <sub>GHQZ</sub> <sup>i</sup>	t <sub>OHZ</sub>	Output Disable to Output Inactive		10		10		12		12	ns
10	t <sub>ELICCH</sub> <sup>f</sup>	t <sub>PA</sub>	Chip Enable to Power Active	0		0		0		0		ns
11	t <sub>EHICCL</sub> <sup>f</sup>	t <sub>PS</sub>	Chip Disable to Power Standby		25		35		45		55	ns

Note g:  $\overline{W}$  and  $\overline{HSB}$  must be high during SRAM READ cycles.  
 Note h: Device is continuously selected with  $\overline{E}$  and  $\overline{G}$  both low.  
 Note i: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled<sup>g, h</sup>



SRAM READ CYCLE #2:  $\overline{E}$  Controlled<sup>g</sup>



# STK12C68

## SRAM WRITE CYCLES #1 & #2

( $V_{CC} = 5.0V \pm 10\%$ )<sup>e</sup>

NO.	SYMBOLS			PARAMETER	STK12C68-25		STK12C68-35		STK12C68-45		STK12C68-55		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{AVAV}$	$t_{AVAV}$	$t_{WC}$	Write Cycle Time	25		35		45		55		ns
13	$t_{WLWH}$	$t_{WLEH}$	$t_{WP}$	Write Pulse Width	20		25		30		45		ns
14	$t_{ELWH}$	$t_{ELEH}$	$t_{CW}$	Chip Enable to End of Write	20		25		30		45		ns
15	$t_{DVWH}$	$t_{DVEH}$	$t_{DW}$	Data Set-up to End of Write	10		12		15		25		ns
16	$t_{WHDX}$	$t_{EHDX}$	$t_{DH}$	Data Hold after End of Write	0		0		0		0		ns
17	$t_{AVWH}$	$t_{AVEH}$	$t_{AW}$	Address Set-up to End of Write	20		25		30		45		ns
18	$t_{AVWL}$	$t_{AVEL}$	$t_{AS}$	Address Set-up to Start of Write	0		0		0		0		ns
19	$t_{WHAX}$	$t_{EHAX}$	$t_{WR}$	Address Hold after End of Write	0		0		0		0		ns
20	$t_{WLOZ}^{i,j}$		$t_{WZ}$	Write Enable to Output Disable		10		13		14		15	ns
21	$t_{WHQX}$		$t_{OW}$	Output Active after End of Write	5		5		5		5		ns

Note j: If  $\bar{W}$  is low when  $\bar{E}$  goes low, the outputs remain in the high-impedance state.

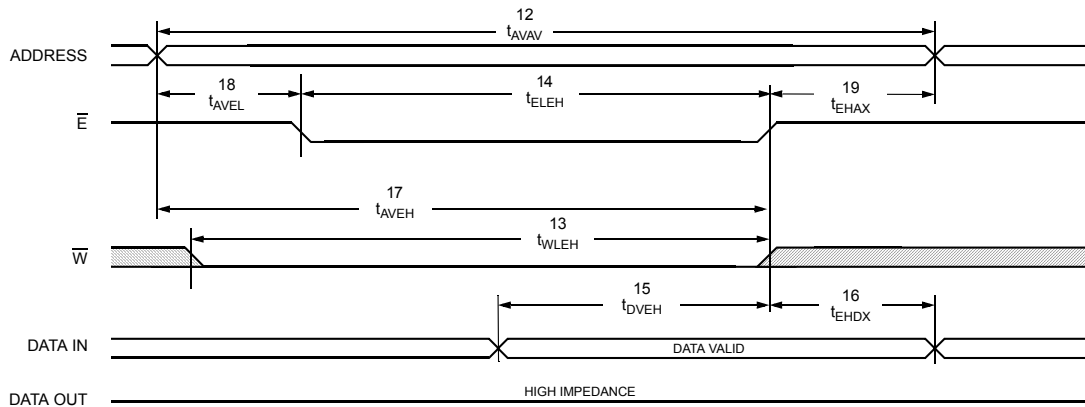
Note k:  $\bar{E}$  or  $\bar{W}$  must be  $\geq V_{IH}$  during address transitions.

Note l: HSB must be high during SRAM WRITE cycles.

### SRAM WRITE CYCLE #1: $\bar{W}$ Controlled<sup>k, l</sup>



### SRAM WRITE CYCLE #2: $\bar{E}$ Controlled<sup>k, l</sup>



**HARDWARE MODE SELECTION**

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A <sub>12</sub> - A <sub>0</sub> (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	o
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile <i>STORE</i>	Output High Z	I <sub>CC2</sub>	m
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile <i>STORE</i>	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I <sub>CC2</sub>	n, o
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile <i>RECALL</i>	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	n, o

Note m:  $\overline{HSB}$  *STORE* operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the *STORE* (if any) completes, the part will go into standby mode, inhibiting all operations until  $\overline{HSB}$  rises.

Note n: The six consecutive addresses must be in the order listed.  $\overline{W}$  must be high during all six consecutive cycles to enable a nonvolatile cycle.

Note o: I/O state assumes  $\overline{G} \leq V_{IL}$ . Activation of nonvolatile cycles does not depend on state of  $\overline{G}$ .

**HARDWARE STORE CYCLE**

(V<sub>CC</sub> = 5.0V ± 10%)<sup>e</sup>

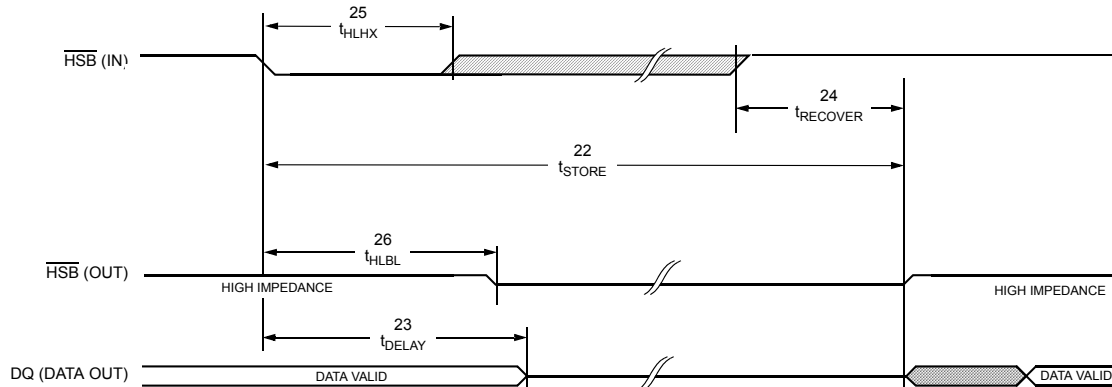
NO.	SYMBOLS		PARAMETER	STK12C68		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t <sub>STORE</sub>	t <sub>HLHZ</sub>	<i>STORE</i> Cycle Duration		10	ms	i, p
23	t <sub>DELAY</sub>	t <sub>HLQZ</sub>	Time Allowed to Complete SRAM Cycle	1		μs	i, q
24	t <sub>RECOVER</sub>	t <sub>HHQX</sub>	Hardware <i>STORE</i> High to Inhibit Off		700	ns	p, r
25	t <sub>HLHX</sub>		Hardware <i>STORE</i> Pulse Width	15		ns	
26	t <sub>HLBL</sub>		Hardware <i>STORE</i> Low to Store Busy		300	ns	

Note p:  $\overline{E}$  and  $\overline{G}$  low for output behavior.

Note q:  $\overline{E}$  and  $\overline{G}$  low and  $\overline{W}$  high for output behavior.

Note r: t<sub>RECOVER</sub> is only applicable after t<sub>STORE</sub> is complete.

**HARDWARE STORE CYCLE**



# STK12C68

## AutoStore™/POWER-UP RECALL

( $V_{CC} = 5.0V \pm 10\%$ )<sup>e</sup>

NO.	SYMBOLS		PARAMETER	STK12C68		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
27	$t_{RESTORE}$		Power-up <i>RECALL</i> Duration		550	$\mu$ s	s
28	$t_{STORE}$	$t_{HLHZ}$	<i>STORE</i> Cycle Duration		10	ms	p, q, t
29	$t_{VSBL}$		Low Voltage Trigger ( $V_{SWITCH}$ ) to $\overline{HSB}$ Low		300	ns	l
30	$t_{DELAY}$	$t_{BLQZ}$	Time Allowed to Complete SRAM Cycle	1		$\mu$ s	p
31	$V_{SWITCH}$		Low Voltage Trigger Level	4.0	4.5	V	
32	$V_{RESET}$		Low Voltage Reset Level		3.9	V	

Note s:  $t_{RESTORE}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .

Note t:  $\overline{HSB}$  is asserted low for  $1\mu$ s when  $V_{CAP}$  drops through  $V_{SWITCH}$ . If an SRAM WRITE has not taken place since the last nonvolatile cycle,  $\overline{HSB}$  will be released and no *STORE* will take place.

## AutoStore™/POWER-UP RECALL



**SOFTWARE-CONTROLLED STORE/RECALL CYCLE<sup>V</sup>**

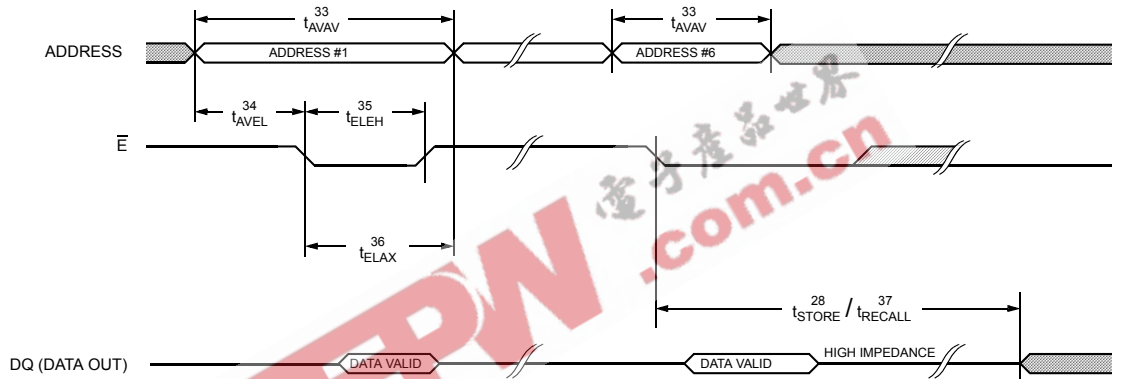
( $V_{CC} = 5.0V \pm 10\%$ )<sup>e</sup>

NO.	SYMBOLS		PARAMETER	STK12C68-25		STK12C68-35		STK12C68-45		STK12C68-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
33	$t_{AVAV}$	$t_{RC}$	STORE/RECALL Initiation Cycle Time	25		35		45		55		ns	p
34	$t_{AVEL}$	$t_{AS}$	Address Set-up Time	0		0		0		0		ns	u
35	$t_{ELEH}$	$t_{CW}$	Clock Pulse Width	20		25		30		30		ns	u
36	$t_{ELAX}$		Address Hold Time	20		20		20		20		ns	u
37	$t_{RECALL}$		RECALL Duration		20		20		20		20	$\mu$ s	

Note u: The software sequence is clocked with  $\bar{E}$  controlled READs.

Note v: The six consecutive addresses must be in the order listed in the Hardware Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle.  $\bar{W}$  must be high during all six consecutive cycles.

**SOFTWARE STORE/RECALL CYCLE:  $\bar{E}$  Controlled<sup>V</sup>**



## DEVICE OPERATION

The STK12C68 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to Nonvolatile Elements (the *STORE* operation) or from Nonvolatile Elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

### NOISE CONSIDERATIONS

The STK12C68 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 $\mu$ F connected between  $V_{CAP}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

### SRAM READ

The STK12C68 performs a READ cycle whenever  $\bar{E}$  and  $\bar{G}$  are low and  $\bar{W}$  and  $\overline{HSB}$  are high. The address specified on pins  $A_{0-12}$  determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{AVQV}$  (READ cycle #1). If the READ is initiated by  $\bar{E}$  or  $\bar{G}$ , the outputs will be valid at  $t_{ELQV}$  or at  $t_{GLQV}$ , whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the  $t_{AVQV}$  access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\bar{E}$  or  $\bar{G}$  is brought high, or  $\bar{W}$  or  $\overline{HSB}$  is brought low.

### SRAM WRITE

A WRITE cycle is performed whenever  $\bar{E}$  and  $\bar{W}$  are low and  $\overline{HSB}$  is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\bar{E}$  or  $\bar{W}$  goes high at the end of the cycle. The data on the common I/O pins  $DQ_{0-7}$  will be written into the memory if it is valid  $t_{DVWH}$  before the end of a  $\bar{W}$  controlled WRITE or  $t_{DVEH}$  before the end of an  $\bar{E}$  controlled WRITE.

It is recommended that  $\bar{G}$  be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If  $\bar{G}$  is left low, internal circuitry will turn off the output buffers  $t_{WLQZ}$  after  $\bar{W}$  goes low.

### POWER-UP RECALL

During power up, or after any low-power condition ( $V_{CAP} < V_{RESET}$ ), an internal *RECALL* request will be latched. When  $V_{CAP}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a *RECALL* cycle will automatically be initiated and will take  $t_{RESTORE}$  to complete.

If the STK12C68 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between  $\bar{W}$  and system  $V_{CC}$  or between  $\bar{E}$  and system  $V_{CC}$ .

### SOFTWARE NONVOLATILE STORE

The STK12C68 software *STORE* cycle is initiated by executing sequential  $\bar{E}$  controlled READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

- |                 |            |                             |
|-----------------|------------|-----------------------------|
| 1. Read address | 0000 (hex) | Valid READ                  |
| 2. Read address | 1555 (hex) | Valid READ                  |
| 3. Read address | 0AAA (hex) | Valid READ                  |
| 4. Read address | 1FFF (hex) | Valid READ                  |
| 5. Read address | 10F0 (hex) | Valid READ                  |
| 6. Read address | 0F0F (hex) | Initiate <i>STORE</i> cycle |

The software sequence must be clocked with  $\bar{E}$  controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that  $\bar{G}$  be low for the sequence to be valid. After the  $t_{STORE}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.



**SOFTWARE NONVOLATILE RECALL**

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of  $\bar{E}$  controlled READ operations must be performed:

- |                 |            |                              |
|-----------------|------------|------------------------------|
| 1. Read address | 0000 (hex) | Valid READ                   |
| 2. Read address | 1555 (hex) | Valid READ                   |
| 3. Read address | 0AAA (hex) | Valid READ                   |
| 4. Read address | 1FFF (hex) | Valid READ                   |
| 5. Read address | 10F0 (hex) | Valid READ                   |
| 6. Read address | 0F0E (hex) | Initiate <i>RECALL</i> cycle |

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the Nonvolatile Elements. The nonvolatile data can be recalled an unlimited number of times.

**AutoStore™ OPERATION**

The STK12C68 can be powered in one of three modes.

During normal *AutoStore™* operation, the STK12C68 will draw current from  $V_{CCX}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the  $V_{CAP}$  pin drops below  $V_{SWITCH1}$ , the part will automatically disconnect the  $V_{CAP}$  pin from  $V_{CCX}$  and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 68 $\mu$ F and 220 $\mu$ F ( $\pm 20\%$ ) rated at 6V should be provided.

In system power mode (Figure 3), both  $V_{CCX}$  and  $V_{CAP}$  are connected to the +5V power supply without the 68 $\mu$ F capacitor. In this mode the *AutoStore™* function of the STK12C68 will operate on the stored system charge as power goes down. The user must, however, guarantee that  $V_{CCX}$  does not drop below 3.6V during the 10ms *STORE* cycle.

If an automatic *STORE* on power loss is not required, then  $V_{CCX}$  can be tied to ground and +5V applied to  $V_{CAP}$  (Figure 4). This is the *AutoStore™* Inhibit mode, in which the *AutoStore™* function is disabled. If the STK12C68 is operated in this configuration, references to  $V_{CCX}$  should be changed to  $V_{CAP}$  throughout this data sheet. In this mode, *STORE* operations may be triggered through software control or the  $\overline{HSB}$  pin. It is not permissible to change between these three options “on the fly”.

In order to prevent unneeded *STORE* operations, automatic *STORES* as well as those initiated by externally driving  $\overline{HSB}$  low will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software-initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place. An optional pull-up resistor is shown connected to  $\overline{HSB}$ . This can be used to signal the system that the *AutoStore™* cycle is in progress.

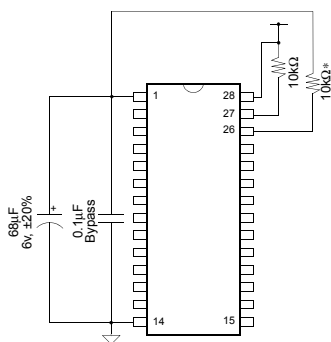


Figure 2: *AutoStore™* Mode



Figure 3: System Power Mode

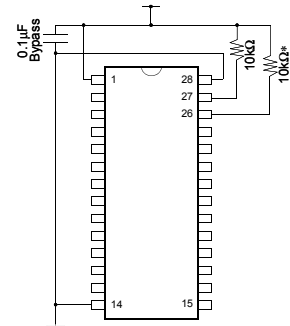


Figure 4: *AutoStore™* Inhibit Mode

\*If  $\overline{HSB}$  is not used, it should be left unconnected.

### HSB OPERATION

The STK12C68 provides the  $\overline{\text{HSB}}$  pin for controlling and acknowledging the *STORE* operations. The  $\overline{\text{HSB}}$  pin is used to request a hardware *STORE* cycle. When the  $\overline{\text{HSB}}$  pin is driven low, the STK12C68 will conditionally initiate a *STORE* operation after  $t_{\text{DELAY}}$ ; an actual *STORE* cycle will only begin if a *WRITE* to the SRAM took place since the last *STORE* or *RECALL* cycle. The  $\overline{\text{HSB}}$  pin acts as an open drain driver that is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress.

SRAM READ and *WRITE* operations that are in progress when  $\overline{\text{HSB}}$  is driven low by any means are given time to complete before the *STORE* operation is initiated. After  $\overline{\text{HSB}}$  goes low, the STK12C68 will continue SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM READ operations may take place. If a *WRITE* is in progress when  $\overline{\text{HSB}}$  is pulled low it will be allowed a time,  $t_{\text{DELAY}}$ , to complete. However, any SRAM *WRITE* cycles requested after  $\overline{\text{HSB}}$  goes low will be inhibited until  $\overline{\text{HSB}}$  returns high.

The  $\overline{\text{HSB}}$  pin can be used to synchronize multiple STK12C68s while using a single larger capacitor. To operate in this mode the  $\overline{\text{HSB}}$  pin should be connected together to the  $\overline{\text{HSB}}$  pins from the other STK12C68s. An external pull-up resistor to +5V is required since  $\overline{\text{HSB}}$  acts as an open drain pull down. The  $V_{\text{CAP}}$  pins from the other STK12C68 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK12C68s detects a power loss and asserts  $\overline{\text{HSB}}$ , the common  $\overline{\text{HSB}}$  pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK12C68s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK12C68 will continue to drive the  $\overline{\text{HSB}}$  pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK12C68 will remain disabled until the  $\overline{\text{HSB}}$  pin returns high.

If  $\overline{\text{HSB}}$  is not used, it should be left unconnected.

### PREVENTING STORES

The *STORE* function can be disabled on the fly by holding  $\overline{\text{HSB}}$  high with a driver capable of sourcing 30mA at a  $V_{\text{OH}}$  of at least 2.2V, as it will have to overpower the internal pull-down device that drives  $\overline{\text{HSB}}$  low for 20 $\mu$ s at the onset of a *STORE*. When the STK12C68 is connected for *AutoStore*<sup>TM</sup> operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CCX}}$  and a 68 $\mu$ F capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH}}$  on the way down, the STK12C68 will attempt to pull  $\overline{\text{HSB}}$  low; if  $\overline{\text{HSB}}$  doesn't actually get below  $V_{\text{IL}}$ , the part will stop trying to pull  $\overline{\text{HSB}}$  low and abort the *STORE* attempt.

### HARDWARE PROTECT

The STK12C68 offers hardware protection against inadvertent *STORE* operation and SRAM *WRITES* during low-voltage conditions. When  $V_{\text{CAP}} < V_{\text{SWITCH}}$ , all externally initiated *STORE* operations and SRAM *WRITES* are inhibited.

*AutoStore*<sup>TM</sup> can be completely disabled by tying  $V_{\text{CCX}}$  to ground and applying +5V to  $V_{\text{CAP}}$ . This is the *AutoStore*<sup>TM</sup> Inhibit mode; in this mode, *STORE*s are only initiated by explicit request using either the software sequence or the  $\overline{\text{HSB}}$  pin.

### LOW AVERAGE ACTIVE POWER

The STK12C68 draws significantly less current when it is cycled at times longer than 50ns. Figure 5 shows the relationship between  $I_{\text{CC}}$  and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{\text{CC}} = 5.5\text{V}$ , 100% duty cycle on chip enable). Figure 6 shows the same relationship for *WRITE* cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK12C68 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of *READS* to *WRITES*; 5) the operating temperature; 6) the  $V_{\text{CC}}$  level; and 7) I/O loading.



Figure 5:  $I_{cc}$  (max) Reads



Figure 6:  $I_{cc}$  (max) Writes

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**ORDERING INFORMATION**

**STK12C68 - 5 P F 45 I**

**Temperature Range**  
Blank = Commercial (0 to 70°C)  
I = Industrial (-40 to 85°C)  
M = Military (-55 to 125°C)

**Access Time**  
25 = 25ns  
35 = 35ns  
45 = 45ns  
55 = 55ns

**Lead Finish (Plastic only)**  
Blank = 85%Sn/15%Pb  
F = 100% Sn (Matte Tin)

**Package**  
P = Plastic 28-pin 300 mil DIP  
W = Plastic 28-pin 600 mil DIP  
S = Plastic 28-pin 350 mil SOIC  
C = Ceramic 28-pin 300 mil DIP (gold lead finish)  
K = Ceramic 28-pin 300 mil DIP (solder dip finish)  
L = Ceramic 28 pin LCC

**Retention / Endurance**  
Blank = Comm/Ind (100 years/10<sup>6</sup>cycles)  
5 = Military (10 years/10<sup>5</sup>cycles)

**5962-94599 01 MX X**

**Lead Finish**  
A = Solder DIP lead finish  
C = Gold lead DIP finish  
X = Lead finish "A" or "C" is acceptable

**Package**  
MX = Ceramic 28 pin 300-mil DIP  
MY = Ceramic 28 pin LCC

**Access Time**  
01 = 55ns  
02 = 45ns  
03 = 35ns

**Document Revision History**

Revision	Date	Summary
0.0	December 2002	Combined commercial, industrial and military datasheets. Removed 20 nsec device.
0.1	January 2003	Added 35 nsec SMD to order information
0.2	July 2003	Added "28 - SOIC" label to page 1 pinout drawing
0.3	September 2003	Added lead-free lead finish
0.4	October 2003	Restored "W" 600 mil DIP package to ordering information

