STK17TA8

nvTime™ Event Data Recorder

128K x 8 *AutoStore*™ nvSRAM with Real-Time Clock

Product Preview

FEATURES

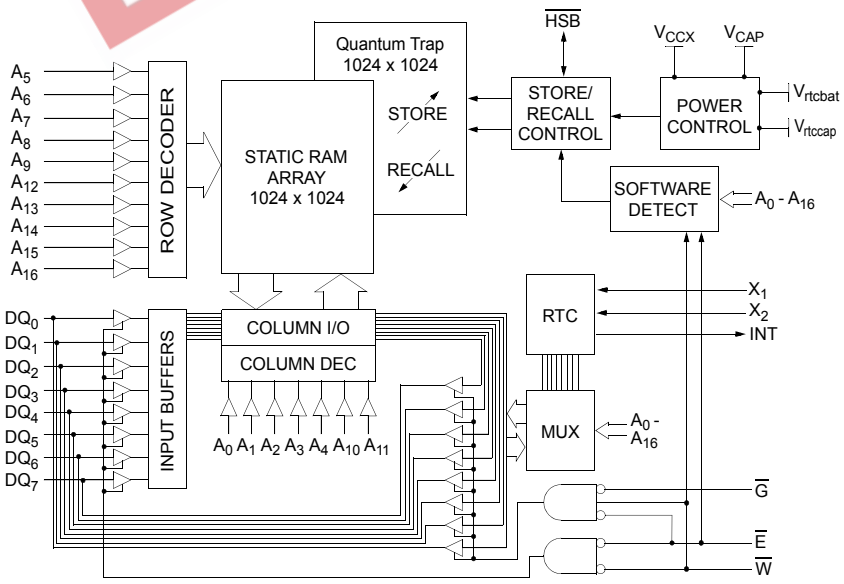
- **Data Integrity of Simtek nvSRAM Combined with Full-Featured Real-Time Clock**
- **25ns, 35ns and 45ns Access Times**
- **Software or *AutoStore*™ *STORE* to *QuantumTrap*™ Nonvolatile Elements**
- ***RECALL* to SRAM Initiated by Software or Power Restore**
- **Unlimited READ, WRITE and *RECALL* Cycles**
- **100-Year Data Retention**
- **Watchdog Timer**
- **Clock Alarm with programmable Interrupts**
- **Capacitor or battery backup for RTC**
- **Single 3V +20%, -10% Operation**
- **Commercial and Industrial Temperatures**
- **Packages: 48 pin SSOP, 40 pin DIP**

DESCRIPTION

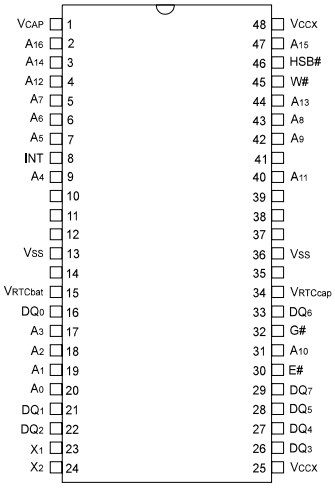
The Simtek STK17TA8 combines a 1 Mbit nonvolatile static RAM with a full-featured real-time clock in a reliable, monolithic integrated circuit. The embedded nonvolatile elements incorporate Simtek's *QuantumTrap*™ technology producing the world's most reliable nonvolatile memory. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in the nonvolatile elements.

The Real-Time Clock function provides an accurate clock with leap year tracking and a programmable, high accuracy oscillator. The Alarm function is programmable for one-time alarms or periodic seconds, minutes, hours, or days. There is also a programmable Watchdog Timer for process control.

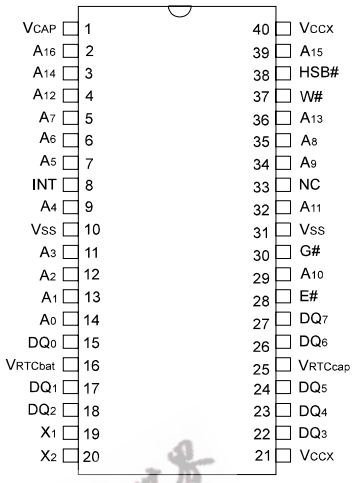
BLOCK DIAGRAM



PACKAGES



48 Pin 300 mil SSOP



40 Pin 600 mil DIP

(not to scale)

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_0 - A_{16}	Input	Address: The 17 address inputs select one of 131,072 bytes in the nvSRAM array or one of 16 bytes in the clock register map.
DQ_0 -DQ_7	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM array and clock.
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device.
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the adddress location latched by the falling edge of $\overline{E}$.
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. Deasserting $\overline{G}$ high causes the DQ pins to tri-state.
X_1, X_2	Input	Crystal: Connections for 32.768 kHz crystal.
V_{rtccap}	Power Supply	Capacitor supplied backup RTC supply voltage.
V_{rtcbat}	Power Supply	Battery supplied backup RTC supply voltage.
V_{CCX}	Power Supply	Power (+ 3V)
$\overline{HSB}$	I/O	Hardware Store Busy (I/O)
INT	Output	Interrupt Output: Can be programmed to respond to the clock alarm, the watchdog timer and the power monitor. Programmable to either active high (push/pull) or active low (open-drain).
V_{CAP}	Power Supply	Autostore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
V_{SS}	Power Supply	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Power Supply Voltage . . . . . .–0.5V to +3.9V
Voltage on Input Relative to V_{SS} . . . . . –0.5V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature. . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS(V_{CC} = 3.0V +20%, -10%)[e]

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		70 60 55		75 65 60	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[c]	Average V_{CC} Current during *STORE*		1		1	mA	All Inputs Don't Care, V_{CC} = max
I_{CC_3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 3V, 25°C, Typical		5		5	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{CC_4}[c]	Average V_{CAP} Current during *AutoStore*™ Cycle		0.5		0.5	mA	All Inputs Don't Care
I_{SB}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		0.3		0.3	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
I_{BAK}	RTC Backup Current		200		300	nA	
V_{BAK}	RTC Backup Voltage	1.6		1.6		V	
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + .3	2.0	V_{CC} + .3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC_2} and I_{CC_4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.
Note e: V_{CC} reference levels throughout this datasheet refer to V_{CCX}.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0V to 3V
Input Rise and Fall Times . . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

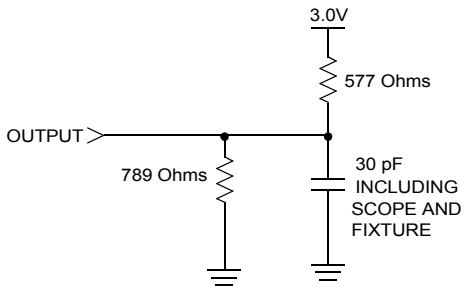


Figure 1: AC Output Loading

CAPACITANCE[f] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

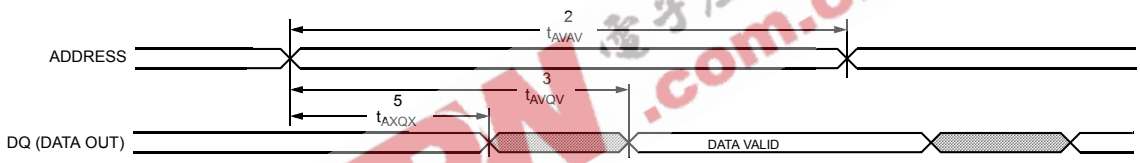
SRAM READ CYCLES #1 & #2

(V_{CC} = 3.0V +20%, -10%)[e]

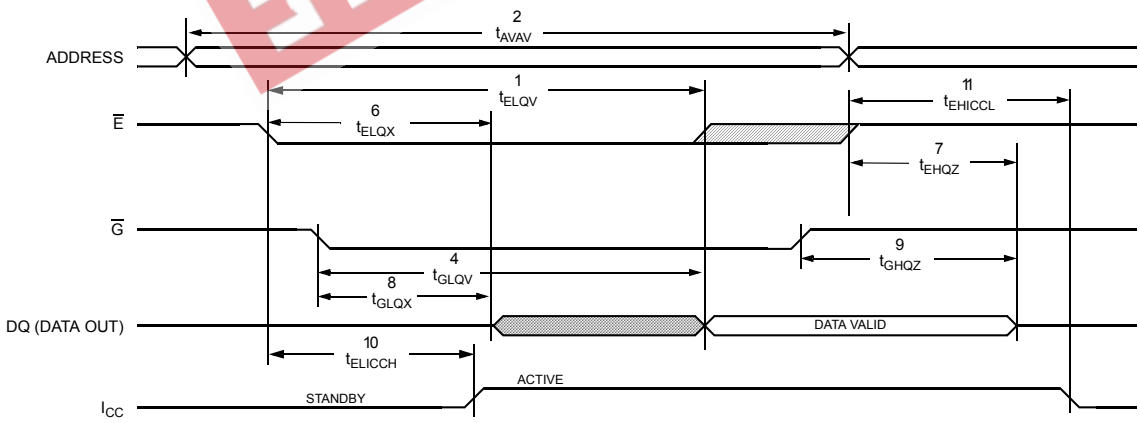
NO.	SYMBOLS		PARAMETER	STK17TA8-25		STK17TA8-35		STK17TA8-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[g]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[h]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}[h]	t_{OH}	Output Hold after Address Change	3		3		3		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
7	t_{EHQZ}[i]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[i]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}[f]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[f]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note g: $\overline{W}$ must be high during SRAM READ cycles.
Note h: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low.
Note i: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[g, h]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[g]



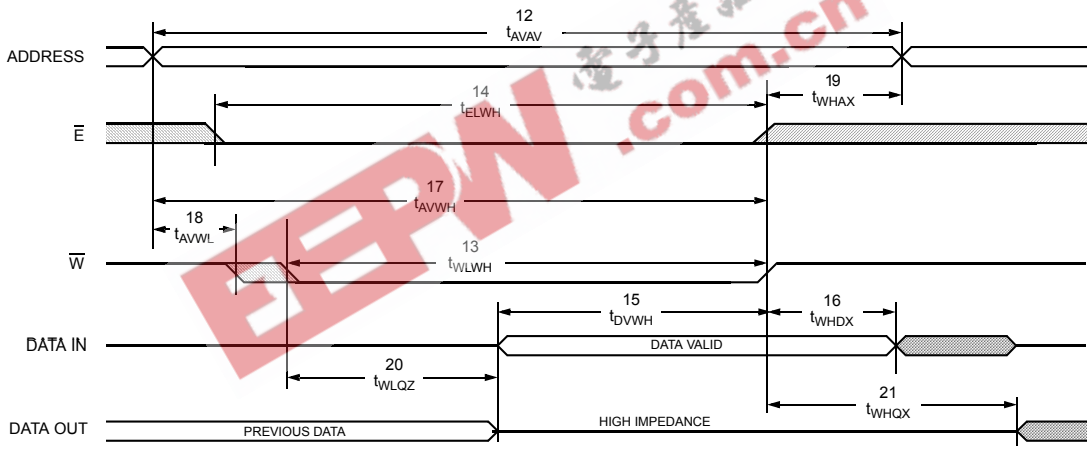
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 3.0V +20%, -10%)[e]

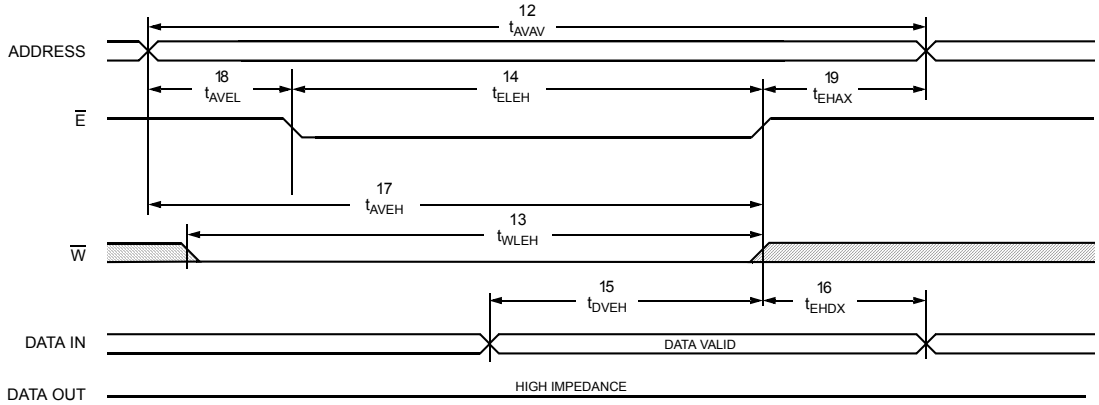
NO.	SYMBOLS			PARAMETER	STK17TA8-25		STK17TA8-35		STK17TA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[i, j]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	3		3		3		ns

Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note l: $\overline{HSB}$ must be high during SRAM write cycles.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[k, l]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[k, l]



MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{15} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	4E38 B1C7 83E0 7C1F 703F 8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore Inhibit	Output Data Output Data Output Data Output Data Output Data Output Data	Active	m, n, o
L	H	L	4E38 B1C7 83E0 7C1F 703F 4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore inhibit off	Output Data Output Data Output Data Output Data Output Data Output Data	Active	m, n, o
L	H	L	4E38 B1C7 83E0 7C1F 703F 8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC_2}	m, n, o
L	H	L	4E38 B1C7 83E0 7C1F 703F 4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	m, n, o

Note m: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
Note n: While there are 17 addresses on the STK17TA8, only the lower 16 are used to control software modes.
Note o: I/O state depends on the state of $\overline{G}$. The I/O table shown assumes $\overline{G}$ low.

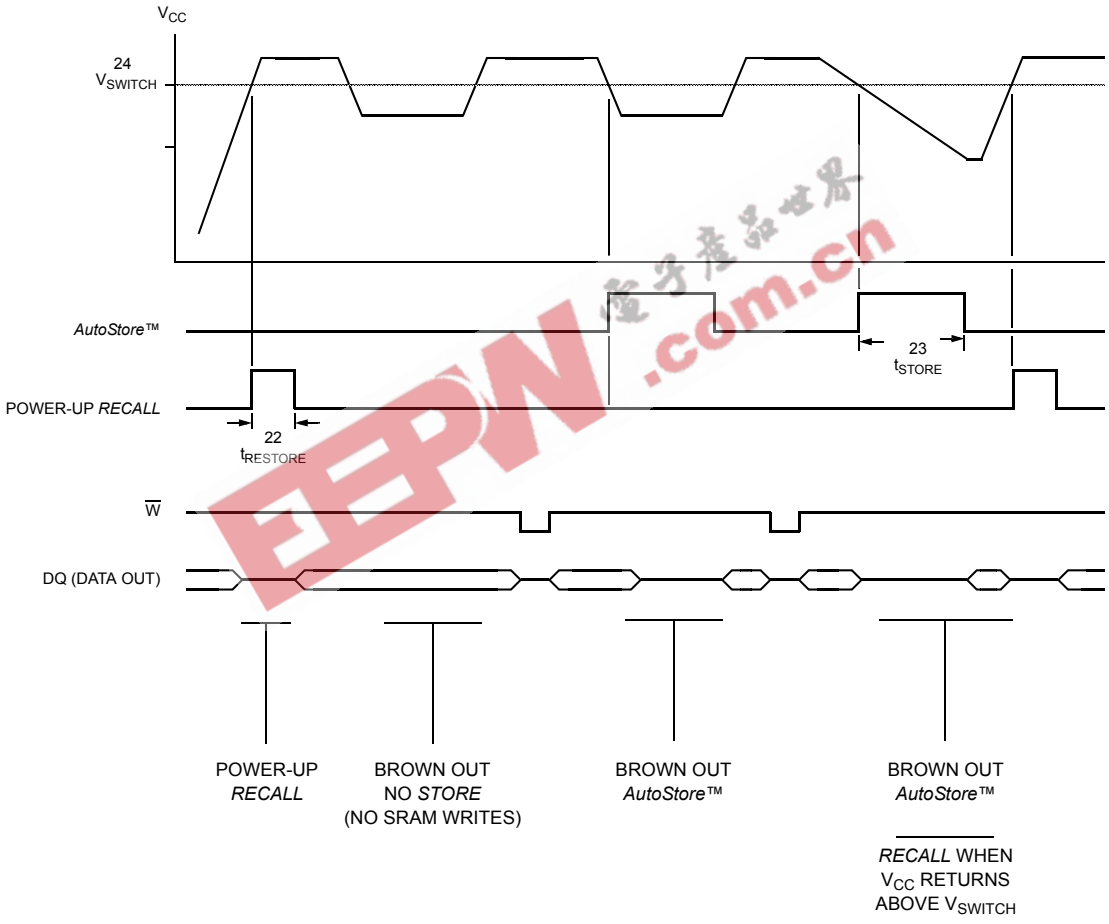
AutoStore™/POWER-UP *RECALL*

(V_{CC} = 3.0V +20%, -10%)[e]

NO.	SYMBOLS		PARAMETER	STK17TA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	$t_{RESTORE}$		Power-up *RECALL* Duration		5	ms	p
23	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	q
24	V_{SWITCH}		Low Voltage Trigger Level	2.55	2.65	V	

Note p: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note q: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place.

AutoStore™/POWER-UP *RECALL*

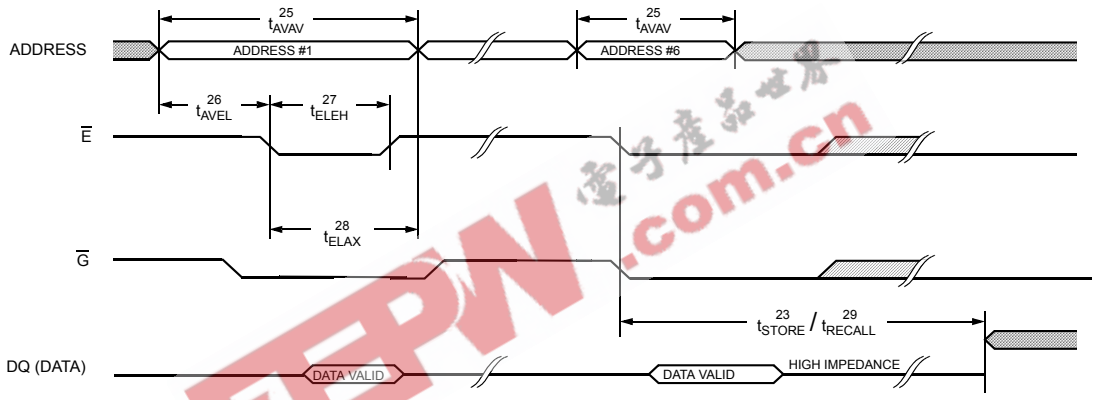


SOFTWARE-CONTROLLED *STORE*/*RECALL* CYCLE[s] (V_{CC} = 3.0V +20%, -10%)[e]

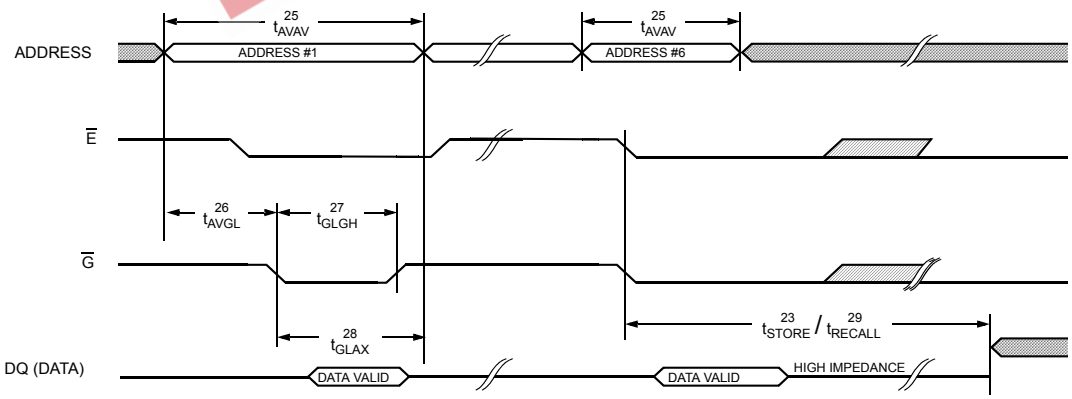
NO.	SYMBOLS			PARAMETER	STK17TA8-25		STK17TA8-35		STK17TA8-45		UNITS	NOTES
	$\overline{E}$ cont	$\overline{G}$ cont	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
25	t_{AVAV}	t_{AVAV}	t_{RC}	*STORE*/*RECALL* Initiation Cycle Time	25		35		45		ns	s
26	t_{AVEL}	t_{AVGL}	t_{AS}	Address Set-up Time	0		0		0		ns	
27	t_{ELEH}	t_{GLGH}	t_{CW}	Clock Pulse Width	20		25		30		ns	
28	t_{ELAX}	t_{GLAX}		Address Hold Time	20		20		20		ns	
29	t_{RECALL}	t_{RECALL}		*RECALL* Duration		20		20		20	µs	

Note r: The software sequence is clocked with $\overline{E}$ controlled READs or $\overline{G}$ controlled READs.
Note s: The six consecutive addresses must be in the order listed in the Hardware Mode Selection Table: (4E38, B1C7, 83E0, 7C1F, 703F, 8FC0) for a *STORE* cycle or (4E38, B1C7, 83E0, 7C1F, 703F, 4C63) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{E}$ CONTROLLED[s]



SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{G}$ CONTROLLED[s]

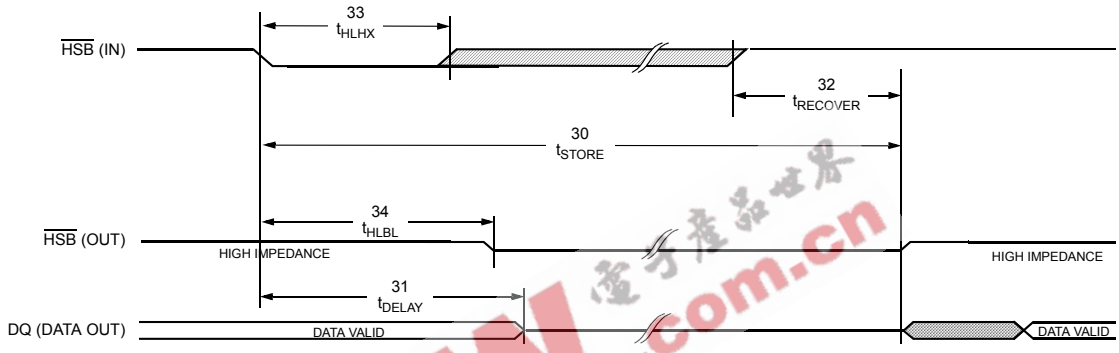


HARDWARE *STORE* CYCLE[t] (V_{CC} = 3.0V +20%, -10%)[e]

NO.	SYMBOLS		PARAMETER	STK17TA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
30	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	i
31	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	i
32	$t_{RECOVER}$	t_{HHQX}	Hardware *STORE* High to Inhibit Off		100	ns	t
33	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
34	t_{HLBL}		Hardware *STORE* Low to *STORE* Busy		300	ns	

Note t: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE *STORE* CYCLE



DEVICE OPERATION

nvSRAM

The STK17TA8 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to the nonvolatile elements (the *STORE* operation) or from the nonvolatile elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled. The STK17TA8 supports unlimited reads and writes to the SRAM, unlimited recalls from the nonvolatile elements and up to 1 million stores to the nonvolatile elements

SRAM READ

The STK17TA8 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-16} determines which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore™ OPERATION

The STK17TA8 can be powered in one of three modes.

During normal operation, the STK17TA8 will draw current from V_{CCX} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CCX} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 10μF and 100μF (±20%) rated at minimum of 5V should be provided.

In order to prevent unneeded *STORE* operations, automatic *STORE*s as well as those initiated by externally driving $\overline{HSB}$ low, will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place. $\overline{HSB}$ can be used to signal the system that the *AutoStore*™ cycle is in progress.

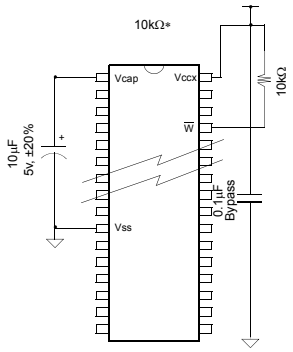


Figure 2: *AutoStore*™ Mode

If $\overline{HSB}$ is not used it should be left unconnected

$\overline{HSB}$ OPERATION

The STK17TA8 provides the $\overline{HSB}$ pin for controlling and acknowledging the *STORE* operations. The $\overline{HSB}$ pin can be used to request a hardware *STORE* cycle. When the $\overline{HSB}$ pin is driven low, the STK17TA8 will conditionally initiate a *STORE* operation after t_{DELAY}; an actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or

RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the *STORE* operation is initiated. After $\overline{HSB}$ goes low, the STK17TA8 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until $\overline{HSB}$ returns high.

The $\overline{HSB}$ pin can be used to synchronize one STK17TA8 with one or more STK14CA8 nvSRAMs to expand the memory space. To operate in this mode the $\overline{HSB}$ pins from each device should be connected together. An external pull-up resistor to +3.0V is required since $\overline{HSB}$ acts as an open drain pull down. The V_{CAP} pins from the other parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the devices detects a power loss and asserts $\overline{HSB}$, the common $\overline{HSB}$ pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those devices that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK17TA8 will continue to drive the $\overline{HSB}$ pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK17TA8 will remain disabled until the $\overline{HSB}$ pin returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

POWER-UP *RECALL*

During power up, or after any low-power condition (V_{CCX} < V_{SWITCH}), an internal *RECALL* request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK17TA8 is in a WRITE state at the end of power-up *RECALL*, the WRITE will be inhibited and $\overline{E}$ or $\overline{W}$ must be brought high and then low for a write to initiate.

SOFTWARE NONVOLATILE *STORE*

The STK17TA8 software *STORE* cycle is initiated by executing sequential $\overline{E}$ controlled READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	8FC0 (hex)	Initiate *STORE* cycle

The software sequence may be clocked with $\overline{E}$ controlled READs or $\overline{G}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of $\overline{E}$ controlled READ operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	4C63 (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile

information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements.

PREVENTING STORES

The *AutoStore*™ function can be disabled by initiating an *AutoStore Inhibit* sequence. A sequence of read operations is performed in a manner similar to the software *STORE* initiation. To initiate the *AutoStore Inihibit* sequence, the following sequence of $\overline{E}$ controlled read operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	8B45 (hex)	*AutoStore Inhibit*

The *AutoStore Inhibit* can be disabled by initiating an *AutoStore Inhibit Off* sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Inhibit Off* sequence, the following sequence of E controlled read operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	4B46 (hex)	*AutoStore Inhibit Off*

The last *AutoStore Inhibit* state is stored in nonvolatile memory and is retained through power cycling.

NOISE CONSIDERATIONS

The STK17TA8 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CAP} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

HARDWARE WRITE PROTECT

The STK17TA8 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When $V_{CCX} < V_{SWITCH}$, all externally initiated *STORE* operations and SRAM WRITEs will be inhibited.

LOW AVERAGE ACTIVE POWER

The STK17TA8 draws significantly less current when it is cycled at times longer than 50ns. Figure 3 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for commercial temperature range, V_{CC} = 3.6V, and 100% duty cycle on chip enable. Figure 4 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK17TA8 depends on the following items: 1) the duty cycle of chip enable; 2) the overall cycle rate for accesses; 3) the ratio of READs to WRITEs; 4) the operating temperature; 5) the V_{CC} level; and 6) I/O loading.

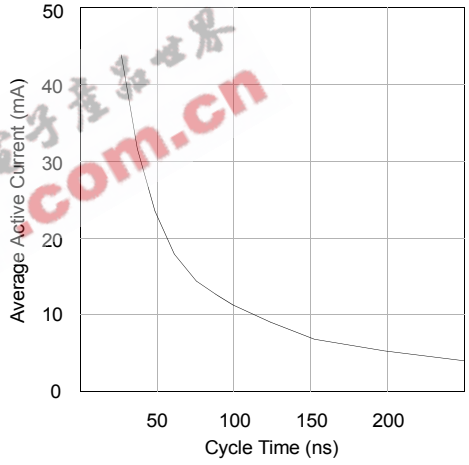


Figure 3: I_{cc} (max) Reads

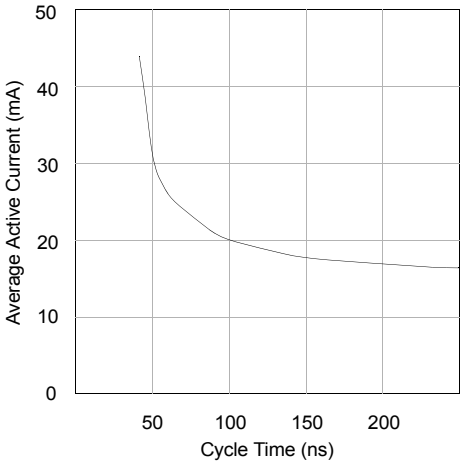


Figure 4: I_{cc} (max) Writes

nvTIME OPERATION

The STK17TA8 offers internal registers that contain Clock, Alarm, Watchdog, Interrupt, and Control functions. Internal double buffering of the clock and the clock/timer information registers prevents accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or clock accuracy of the internal clock while accessing clock data. Clock and Alarm Registers store data in BCD format.

CLOCK OPERATIONS

The clock registers maintain time up to 9,999 years in one second increments. The user can set the time to any calendar time and the clock automatically keeps track of days of the week and month, leap years and century transitions. There are eight registers dedicated to the clock functions which are used to set time with a write cycle and to read time during a read cycle. These registers contain the Time of Day in BCD format. Bits defined as "X" are currently not used and are reserved for future use by Simtek.

READING THE CLOCK

While the double-buffered RTC register structure reduces the chance of reading incorrect data from the clock, the user should halt internal updates to the STK17TA8 clock registers before reading clock data to prevent the reading of data in transition. Stopping the internal register updates does not affect clock accuracy.

The updating process is stopped by writing a "1" to the read bit (in the control register 1FFF0h), and will not restart until a "0" is written to the read bit. The RTC registers can then be read while the internal clock continues to run.

Within 10 msec after a "0" is written to the read bit, all STK17TA8 registers are simultaneously updated.

SETTING THE CLOCK

Setting the write bit (in the control register 1FFF0h) to a "1" halts updates to the STK17TA8 registers. The correct day, date and time can then be written into the registers in 24-hour BCD format. Resetting the write bit to "0" transfers those values to the actual clock counters, after which the clock resumes normal operation.

BACKUP POWER

The STK17TA8 is intended for permanently powered operation, but when primary power, Vcc, fails and drops below Vswitch the device will switch to backup power from either Vbakcap or Vbakbat, depending on whether a capacitor or battery is chosen for the application.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of clock operation with the primary source removed, the data stored in vSRAM is secure, having been stored in the nonvolatile elements as power was lost. Factors to be considered when choosing a backup power source include: the expected duration of power outages and the cost tradeoff of using a battery versus a capacitor.

During backup operation the STK17TA8 consumes a maximum of 300 nanoamps at 2 volts. Capacitor or battery values should be chosen according to the application. Backup time values based on maximum current specs are shown below. Nominal times are approximately 3 times longer.

Capacitor Value	Backup Time
0.1 F	72 hours
0.47 F	14 days
1.0 F	30 days

Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up.

If a battery is used a 3V lithium is recommended and the STK17TA8 will only source current from the battery when the primary power is removed. The battery will not, however, be recharged at any time by the STK17TA8. The battery capacity should be chosen for total anticipated cumulative down-time required over the life of the system.

STOPPING AND STARTING THE OSCILLATOR

The oscillator may be stopped at any time. This feature may be used to save battery or capacitor energy during long-term storage to increase shelf life. Setting the $\overline{\text{OSCEN}}$ bit in register 1FFF8h to 1 halts the oscillator. Setting the bit to 0 enables the oscillator. The RTC does not run until the oscillator

is enabled.

CALIBRATING THE CLOCK

The RTC is driven by a quartz controlled oscillator with a nominal frequency of 32.768 KHz. Clock accuracy will depend on the quality of the crystal, usually specified to 35 ppm limits at 25°C. This error could equate to ± 1.53 minutes per month. The STK17TA8 employs a calibration circuit that can improve the accuracy to + 1/-2 ppm at 25°C. The calibration circuit adds or subtracts counts from the oscillator divider circuit.

The number of times pulses are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in control register 1FFF8h. Adding counts speeds the clock up; subtracting counts slows the clock down. The Calibration bits occupy the the five lower order bits in the control register 8. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit, where a "1" indicates positive calibration and a "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary "1" is loaded into the register, only the first 2 minutes of the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles. That is +4.068 or -2.034 ppm of adjustment per calibration step in the calibration register.

In order to determine how to set the calibration one may set the CAL bit in register 1FFF0h to 1, which causes the INT pin to toggle at a nominal 512 Hz. Any deviation measured from the 512 Hz will indicate the degree and direction of the required correction. For example, a reading of 512.010124 Hz would indicate a +20 ppm error, requiring a -10 (001010) to be loaded into the Calibration register. Note that setting or changing the calibration register does not affect the frequency test output frequency.

ALARM

The alarm function compares user-programmed values to the corresponding time-of-day values. When a match occurs, the alarm event occurs. The alarm drives an internal flag, AF, and may drive the INT pin if desired.

There are four alarm match fields. They are date, hours, minutes and seconds. Each of these fields also has a Match bit that is used to determine if the field is used in the alarm match logic. Setting the Match bit to "0" indicates that the corresponding field will be used in the match process.

Depending on the Match bits, the alarm can occur as specifically as one particular second on one day of the month, or as frequently as once per second continuously. The MSB of each alarm register is a Match bit. Selecting none of the Match bits (all 1's) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to "0" causes the logic to match the seconds alarm value to the current time of day. Since a match will occur for only one value per minute, the alarm occurs once per minute. Likewise, setting the seconds and minutes Match bits causes an exact match of these values. Thus, an alarm will occur once per hour. Setting seconds, minutes and hours causes a match once per day. Lastly, selecting all match values causes an exact time and date match. Selecting other bit combinations will not produce meaningful results, however the alarm circuit should follow the functions described.

There are two ways a user can detect an alarm event, by reading the AF flag or monitoring the INT pin. The AF flag in the register 1FFF0h will indicate that a date/time match has occurred. The AF bit will be set to 1 when a match occurs. Reading the Flags/Control register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

WATCHDOG TIMER

The watchdog timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the Watchdog Timer register.

The counter consists of a loadable register and a free running counter. On power up, the watchdog timeout value in register 1FFF7h is loaded into the

counter load register. Counting begins on power up and restarts from the loadable value any time the Watchdog Strobe (WDS) bit is set to 1. The counter is compared to the terminal value of 0. If the counter reaches this value, it causes an internal flag and an optional interrupt output. The user can prevent the timeout interrupt by setting WDS bit to 1 prior to the counter reaching 0. This causes the counter to be reloaded with the watchdog timeout value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt and flag never occurs.

New timeout values can be written by setting the watchdog write bit to 0. When the WDW is 0 (from the previous operation), new writes to the watchdog timeout value bits D5-D0 allow the timeout value to be modified. When WDW is a 1, then writes to bits D5-D0 will be ignored. The WDW function allows a user to set the WDS bit without concern that the watchdog timer value will be modified. A logical diagram of the watchdog timer is shown below. Note that setting the watchdog timeout value to 0 would be otherwise meaningless and therefore disables the watchdog function.

The output of the watchdog timer is a flag bit WDF that is set if the watchdog is allowed to timeout. The flag is set upon a watchdog timeout and cleared when the Flags/Control register is read by the user. The user can also enable an optional interrupt source to drive the INT pin if the watchdog timeout occurs.

POWER MONITOR

The STK17TA8 provides a power management scheme with power-fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low-Vcc access. The power monitor is based on an internal band-gap reference circuit that compares the Vcc voltage to various thresholds.

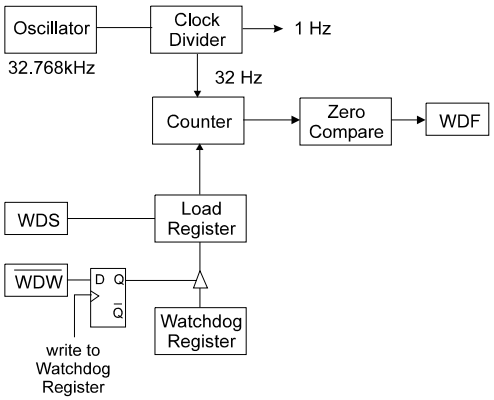


Figure 5. Watchdog Timer Block Diagram

As descibed in the *AutoStore*™ section previously, when Vswitch is reached as Vcc decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from Vccx to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source no data may be read or written and the clock functions are not available to the user. The clock continues to operate in the background. Updated clock data is available to the user 10 msec after Vcc has been restored to the device.

INTERRUPTS

The STK17TA8 provides three potential interrupt sources. They include the watchdog timer, the power monitor, and the clock/calendar alarm. Each can be individually enabled and assigned to drive the INT pin. In addition, each has an associated flag bit that the host processor can use to determine the cause of the interrupt.

Some of the sources have additional control bits that determine functional behavior. In addition, the pin driver has three bits that specify its behavior when an interrupt occurs. A functional diagram of the interrupt logic is shown below.

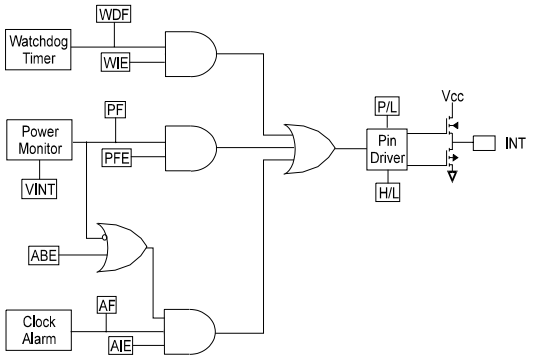


Figure 6. Interrupt Block Diagram

The three interrupts each have a source and an enable. Both the source and the enable must be active (true high) in order to generate an interrupt

output. Only one source is necessary to drive the pin. The user can identify the source by reading the Flags/Control register, which contains the flags associated with each source. All flags are cleared to 0 when the register is read. The cycle must be a complete read cycle ($\overline{WE}$ high); otherwise the flags will not be cleared. The power monitor has two programmable settings that are explained in the power monitor section.

Once an interrupt source is active, the pin driver determines the behavior of the output. It has two programmable settings as shown below. Pin driver control bits are located in the Interrupts register.

According to the programming selections, the pin can be driven in the backup mode for an alarm interrupt. In addition, the pin can be an active low (open-drain) or an active high (push-pull) driver. If programmed for operation during backup mode, it can only be active low. Lastly, the pin can provide a one-shot function so that the active condition is a pulse or a level condition. In one-shot mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In level mode, the pin goes to its active polarity until the Flags/Control register is read by the user. This mode is intended to be used as an interrupt to a host microcontroller. The control bits are summarized as follows:

Watchdog Interrupt Enable - WIE. When set to 1, the watchdog timer drives the INT pin as well as an internal flag when a watchdog timeout occurs. WhenWIE is set to 0, the watchdog timer affects only the internal flag.

Alarm Interrupt Enable - AIE. When set to 1, the alarm match drives the INT pin as well as an internal fla. When set to 0, the alarm match only affects to internal flag.

Power Fail Interrupt Enable - PFE. When set to 1, the power fail monitor drives the pin as well as an internal flag. When set to 0, the power fail monitor affects only the internal flag.

Alarm Battery-backup Enable - ABE. When set to 1, the clock alarm interrupt (as controlled by AIE) will function even in battery backup mode. When set to 0, the alarm will occur only when Vcc>Vswitch. AIE should only be set when the INT pin is programmed for active low operation. In addition, it only functions with the clock alarm, not the watchdog. If enabled, the power monitor will drive the interrupt during all normal Vcc conditions regardless of the ABE bit. The application for ABE is intended for power control, where the system powers up at a predetermined time. Depending on the application, it may require dedicating the INT pin to this function.

High/Low - H/L. When set to a 1, the INT pin is active high and the driver mode is push-pull. The INT pin can drive high only when Vcc>Vswitch. When set to a 0, the INT pin is active low and the drive mode is open-drain. Active low (open drain) is operational even in battery backup mode.

Pulse/Level - P/L. When set to a 1 and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a 0, the INT pin is driven high or low (determined by H/L) until the Flags/Control register is read.

When an enabled interrupt source activates the INT pin, as external host can read the Flags/Control register to determine the cause. Remember that all flags will be cleared when the register is read. If the INT pin is programmed for Level mode, then the condition will clear and the INT pin will return to its inactive state. If the pin is programmed for Pulse mode, then reading the flag also will clear the flag and the pin. The pulse will not complete its specified duration if the Flags/Control register is read. If the INT pin is used as a host reset, then the Flags/Control register cannot be read during a reset.

During a power-on reset with no battery, the interrupt register is automatically loaded with the value 24h. This causes power-fail interrupt to be enabled with an active-low pulse.

RTC Register Map

Register	BCD DATA								FUNCTION/RANGE
	D7	D6	D5	D4	D3	D2	D1	D0	
1FFFFh	10 Years				Years				Years: 00 - 99
1FFFEh	X	X	X	10s Months	Months				Months: 01 - 12
1FFFDh	X	X	10s Day of month		Day of Month				Day of Month:01 - 31
1FFFCh	X	X	X	X	X	Day of Week			Day of Week:01 - 07
1FFFBh	X	X	10s Hours		Hours				Hours: 00 - 23
1FFFAh	X	10s Minutes			Minutes				Minutes: 00 - 59
1FFF9h	X	10s Seconds			Seconds				Seconds: 00 - 59
1FFF8h	$\overline{OSCEN}$	X	Cal Sign	Calibration					Calibration values*
1FFF7h	WDS	$\overline{WDW}$	WDT						Watchdog*
1FFF6h	WIE	AIE	PFE	ABE	$\overline{H/L}$	$\overline{P/L}$	X	X	Interrupts*
1FFF5h	$\overline{M}$	X	10s alarm date		alarm date				Alarm, Day of the Month: 01-31
1FFF4h	M	X	10s alarm hours		alarm hours				Alarm, Hours: 00-23
1FFF3h	$\overline{M}$	10 alarm minutes			alarm minutes				Alarm, minutes: 00-59
1FFF2h	$\overline{M}$	10 alarm seconds			alarm seconds				Alarm, seconds: 00-59
1FFF1h	10s Centuries				Centuries				Centuries: 00 - 99
1FFF0h	WDF	AF	PF	X	X	CAL	W	R	Flags*

X - resevered for future use
* - not BCD values

Register Map Detail

1FFFFh	Timekeeping - Years							
	D7	D6	D5	D4	D3	D2	D1	D0
	10 Years				Years			
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99.							

1FFFEh	Timekeeping - Months							
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	10s Months	Months			
	Contains the BCD digits of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12.							

1FFFDh	Timekeeping - Date							
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	10s Day of month		Day of Month			
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31.							

1FFFCh	Timekeeping - Day							
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	Day of Week		
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meanting to the day value, as the day is not integrated with the date.							

1FFFBh	Timekeeping - Hours							
	D7	D6	D5	D4	D3	D2	D1	D0
	12/24	X	10s Hours		Hours			
	Contains the BCD value of hours in 24 hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23.							

1FFFAh	Timekeeping - Minutes							
	D7	D6	D5	D4	D3	D2	D1	D0
	X	10s Minutes			Minutes			
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59.							

1FFF9h	Timekeeping - Seconds							
	D7	D6	D5	D4	D3	D2	D1	D0
	X	10s Seconds			Seconds			
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59.							

1FFF8h	Contol/Calibration							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{\text{OSCEN}}$	X	Calibration Sign	Calibration				
$\overline{\text{OSCEN}}$	Oscillator Enable. When set to 1, the oscillator is halted. When set to 0, the oscillator runs. Disabling the oscillator saves battery/capacitor power during storage. On a no-battery power-up, this bit is set to 1. The RTC will not run until the oscillator is enabled. Set this bit to 0 to activate the RTC.							
Calibration Sign	Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base.							
Calibration	These five bits control the calibration of the clock.							

1FFF7h	Watchdog Timer							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDS	$\overline{\text{WDW}}$	WDT					
WDS	Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no affect. The bit is cleared automatically once the watchdog timer is reset. The WDS bit is write only. Reading it always will return a 0.							
$\overline{\text{WDW}}$	Watchdog Write Enable. Setting this bit to 1 masks the watchdog timeout value (WDT5-WDT0) so it cannot be written. This allows the user to strobe the watchdg without disturbing the timeout value. Setting this bit to 0 allows bits 5-0 to be witten on the next write to the Watchdog register. The new value will be loaded on the nex internal watchdog clock after the write cycle is complete. This function is explained in more detail in the watchdog timer section.							

1FFF7h	Watchdog Timer							
	D7	D6	D5	D4	D3	D2	D1	D0
WDT	Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The minimum range or timeout value is 31.25 ms (a setting of 1) and the maximum timeout is 2 seconds (setting of 3Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the $\overline{WDW}$ bit was cleared to 0 on a previous cycle.							

1FFF6h	Interrupt Status/Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	WIE	AIE	PFE	ABE	$\overline{H/L}$	$\overline{P/L}$	X	X
WIE	Watchdog Interrupt Enable. When set to 1 and a watchdog timeout occurs, the watchdog timer drives the INT pin as well as the WDF flag. When set to 0, the watchdog timeout affects only the WDF flag.							
AIE	Alarm Interrup Enable. When set to 1, the alarm match drives the INT pin as well as the AF flag. When set to 0, the alarm match only affects the AF flag.							
PFE	Power-Fail Enable. When set to 1, the alarm match drives the INT pin as well as the AF flag. When set to 0, the power-fail monitor affects only the PF flag.							
ABE	Alarm Battery-backup Enable. When set to 1, the alarm interrupt (as controlled by AIE) will function even in battery backup mode. When set to 0, the alarm will occur only when Vcc>Vswitch.							
$\overline{H/L}$	High/Low. When set to a 1, the INT pin is driven active high. When set to 0, the INT pin is open drain, active low.							
$\overline{P/L}$	Pulse/Level. When set to a 1, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to a 0, the INT pin is driven to an active level (as set by H/L) until the Flags/Control register is read.							

1FFF5h	Alarm - Day							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{M}$	0	10s alarm date		alarm date			
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
$\overline{M}$	Match. Setting this bit to 0 causes the date value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.							

1FFF4h	Alarm - Hours							
	D7	D6	D5	D4	D3	D2	D1	D0
	M	0	10s alarm hours		alarm hours			
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
$\overline{M}$	Match. Setting this bit to 0 causes the hours value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the hours value.							

1FFF3h	Alarm - Minutes							
	D7	D6	D5	D4	D3	D2	D1	D0
	M	10s alarm minutes			alarm minutes			
	Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value							
$\overline{M}$	Match. Setting this bit to 0 causes the minutes value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the minutes value.							

1FFF2h	Alarm - Seconds							
	D7	D6	D5	D4	D3	D2	D1	D0
	M	10s alarm seconds			alarm seconds			
	Contains the alarm value for the seconds and the mask bit to select or deselect the seconds value							

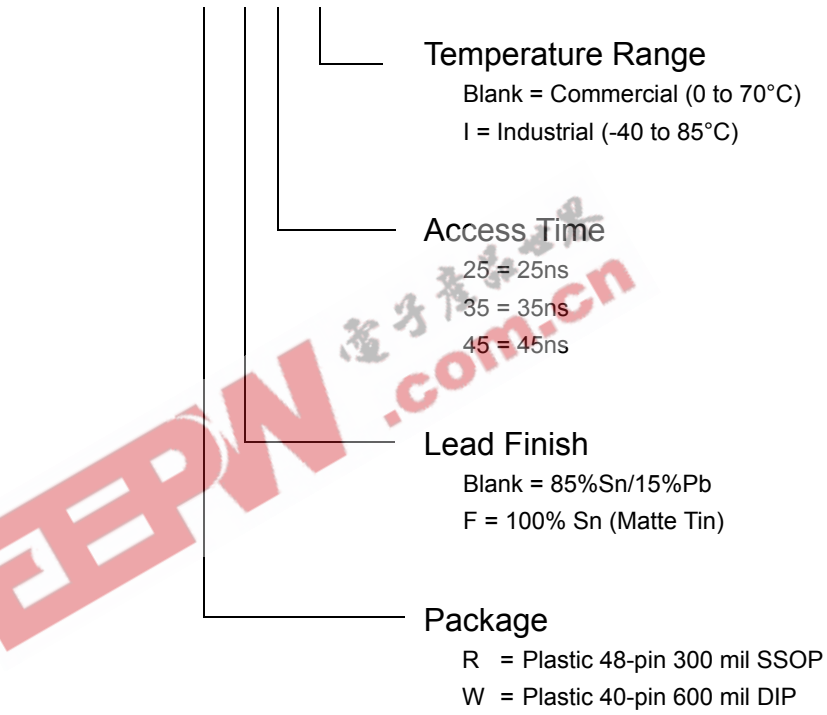
1FFF2h	Alarm - Seconds							
	D7	D6	D5	D4	D3	D2	D1	D0
$\overline{M}$	Match. Setting this bit to 0 causes the seconds value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the seconds value.							

1FFF1h	Timekeeping - Centuries							
	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	10s Centuries		Centuries			

1FFF0h	Flags							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDF	AF	PF	X	X	CAL	W	R
WDF	Watchdog Timer Flag. This read-only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags/Control register is read.							
AF	Alarm Flag. This read-only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags/Control register is read.							
PF	Power-fail Flag. This read-only bit is set to 1 when power falls below the power-fail threshold Vswitch. It is cleared to 0 when the Flags/Control register is read.							
CAL	Calibration Mode. When set to 1, the clock enters calibration mode. When set to 0, the clock operates normally.							
W	Write Time. Setting the W bit to 1 freezes updates of the timekeeping registers. The user can then write them with updated values. Setting the W bit to 0 causes the contents of the time registers to be transferred to the timekeeping counters.							
R	Read Time. Setting the R bit to 1 copies a static image of the timekeeping registers and places them in a holding register. The user can then read them without concerns over changing values causing system errors. The R bit going from 0 to 1 causes the timekeeping capture, so the bit must be returned to 0 prior to reading again.							

ORDERING INFORMATION

STK17TA8 - R F 45 I



Document Revision History

Revision	Date	Summary
0.0	February 2003	Publish new datasheet
0.1	March 2003	Remove 525 mil SOIC, Add 48 Pin SSOP and 40 Pin DIP packages; Modified Block Diagram in AutoStore description section
0.2	June 2003	Modify 600 mil DIP pinout (switch pins 32 and 33), Update Power-up Recall specs, Update Software Controlled Store/Recall Cycle, Added Hardware Store Description, Modified Mode Selection Table, Updated Vswitch, Updated t_{store}, Modify I_{BAK} and V_{BAK}
0.3	February 2004	Change part number from STK17CA8 to STK17TA8; Add lead-free finish option