Winbond Electronics Corp.

128K × 8 CMOS STATIC RAM

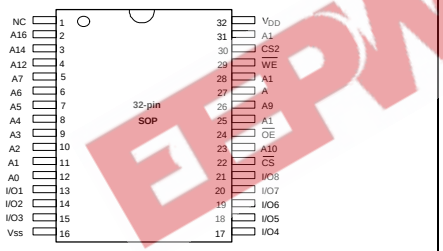
GENERAL DESCRIPTION

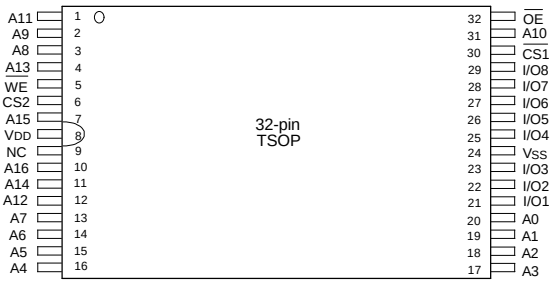
The W24L01 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a wide voltage range from 2.7V to 3.6V power supply. The W24L01 family, W24L01-LE and W24L01-LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

FEATURES

- Low power consumption
- Access time: 55 nS /70 nS
- 2.7V to 3.6V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 1.5V (min.)
- Packaged in 32-pin 450 mil SOP, standard type one TSOP (8 mm × 20 mm), small type one TSOP (8 mm × 13.4 mm) and 48-pin CSP

PIN CONFIGURATIONS

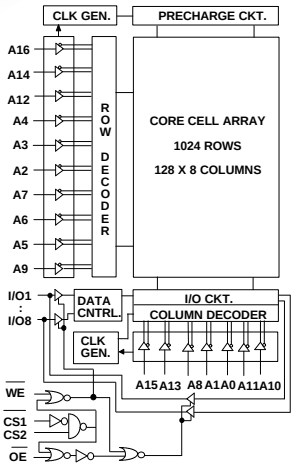




48-pin CSP TOP VIEW

	1	2	3	4	5	6
A	A0	A1	CS2	A3	A6	A8
B	I/O5	A2	WE	A4	A7	I/O1
C	I/O6		NC	A5		I/O2
D	VSS					VCC
E	VCC					VSS
F	I/O7		NC	NC		I/O3
G	I/O8	OE	CS1	A16	A15	I/O4
H	A9	A10	A11	A12	A13	A14

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A16	Address Inputs
I/O1 – I/O8	Data Inputs/Outputs
$\overline{CS}$, CS2	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	I/O1 - I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to VSS Potential		-0.5 to +4.6	V
Input/Output to VSS Potential		-0.5 to VDD +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	LL	0 to 70	°C
	LE	-20 to 85	
	LI	-40 to 85	

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VSS = 0V; TA (°C) = 0 to 70 for LL, -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	W24L01			UNIT
			MIN.	TYP.*	MAX.	
Input Low Voltage	VIL	-	-0.2	-	+0.4	V
Input High Voltage	VIH	-	+2.2	-	VDD +0.3	V
Input Leakage Current	ILI	VIN = VSS to VDD	-1	-	+1	µA
Output Leakage Current	ILO	VI/O = VSS to VDD, $\overline{CS1}$ = VIH (min.) or CS2 = VIL (max.) or $\overline{OE}$ = VIH (min.) or $\overline{WE}$ = VIL (max.)	-1	-	+1	µA
Output Low Voltage	VOL	IOL = +2.1 mA	-	-	0.4	V
Output Low Voltage	VOH	IOH = -1.0 mA	2.2	-	-	V

Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS		W24L01 MIN.	W24L01 TYP.*	W24L01 MAX.	UNIT
Operating Power Supply Current	I_{DD}	$\overline{CS1}$ = V_{IL} (max.) and CS2 = V_{IH} (min.) , I/O = 0 mA, Cycle = min. Duty = 100%		-	25 (3V) 30 (3.3V)	40 (70 nS) 55 (55 nS)	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} (min.) or CS2 = V_{IL} (max.), Cycle = min. Duty = 100%		-	-	0.3	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{DD} -0.2V or CS2 ≤ 0.2V	LL	-	2	5	µA
			LE/LI			7	

Note: Typical parameter is measured under ambient temperature T_A = 25° C

CAPACITANCE

(T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	10	pF

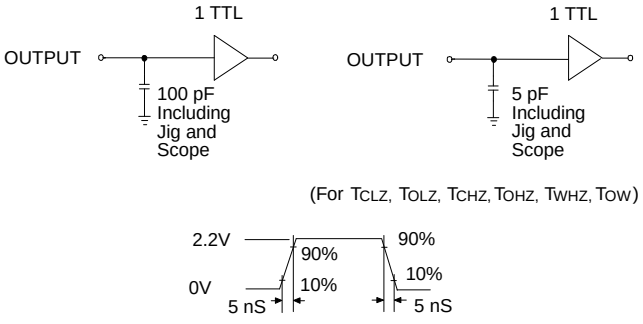
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 2.2V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V, V_{DD} = 3.0V
Output Load	See the drawing below

AC Test Loads and Waveform



AC Characteristics, continued

(V_{SS} = 0V; T_A (°C) = 0 to 70 for LL, -20 to 85 for LE, -40 to 85 for LI)

Read Cycle

PARAMETER	SYM.	MIN.	MAX.	MIN.	MAX.	UNIT
Read Cycle Time	T_{RC}	55	-	70	-	nS
Address Access Time	T_{AA}	-	55	-	70	nS
Chip Select Access Time	T_{ACS}	-	55	-	70	nS
Output Enable to Output Valid	T_{AOE}	-	30	-	35	nS
Chip Selection to Output in Low Z	T_{CLZ}*	10	-	10	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	25	-	30	nS
Output Disable to Output in High Z	T_{OHZ}*	-	25	-	30	nS
Output Hold from Address Change	T_{OH}	5	-	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

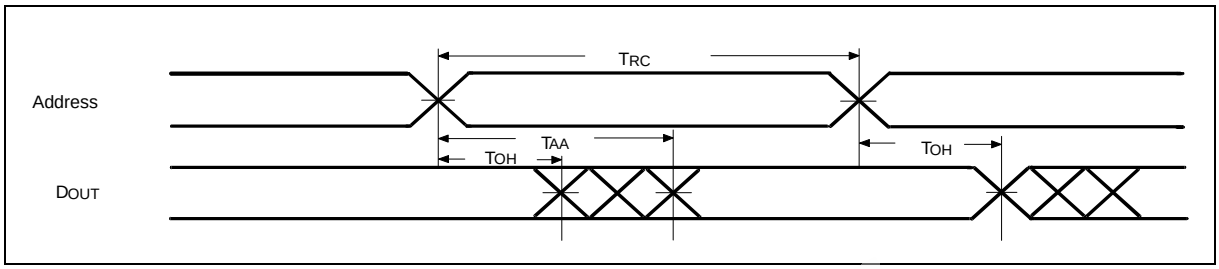
PARAMETER		SYM.	MIN.	MAX.	MIN.	MAX.	UNIT
Write Cycle Time		T_{WC}	55	-	70	-	nS
Chip Selection to End of Write		T_{CW}	50	-	60	-	nS
Address Valid to End of Write		T_{AW}	50	-	60	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	40	-	55	-	nS
Write Recovery Time	$\overline{CS1}$, CS2, $\overline{WE}$	T_{WR}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	30	-	30	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	20	-	25	nS
Output Disable to Output in High Z		T_{OHZ}*	-	20	-	25	nS
Output Active from End of Write		T_{OW}	5	-	5	-	nS

* These parameters are sampled but not 100% tested

TIMING WAVEFORMS

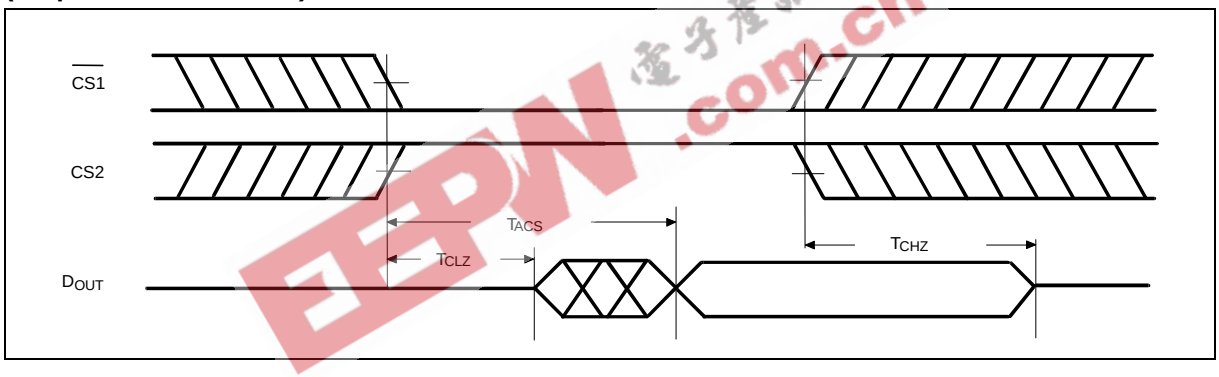
Read Cycle 1

(Address Controlled)



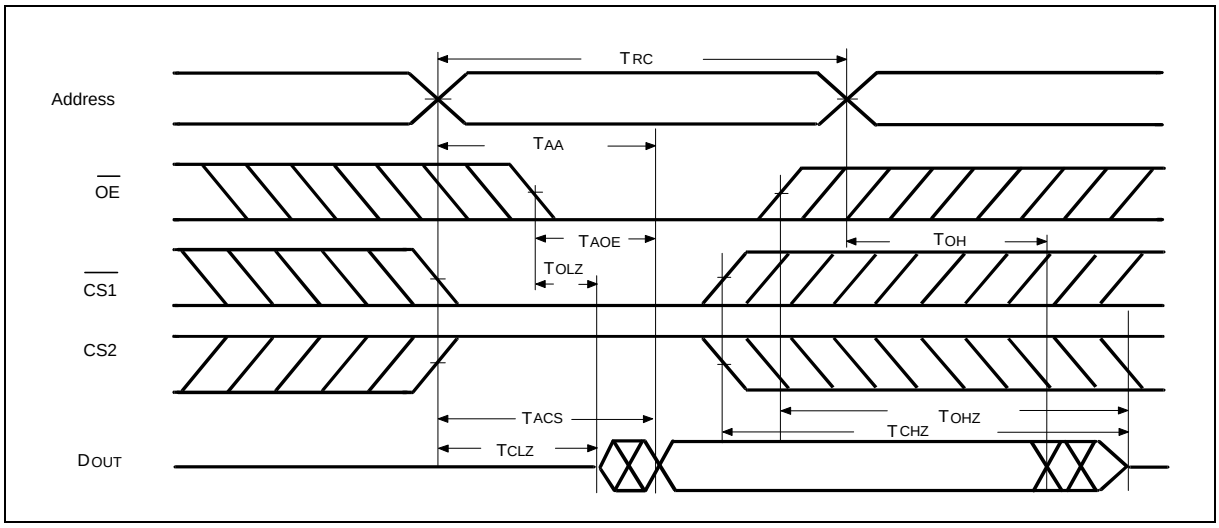
Read Cycle 2

(Chip Select Controlled)



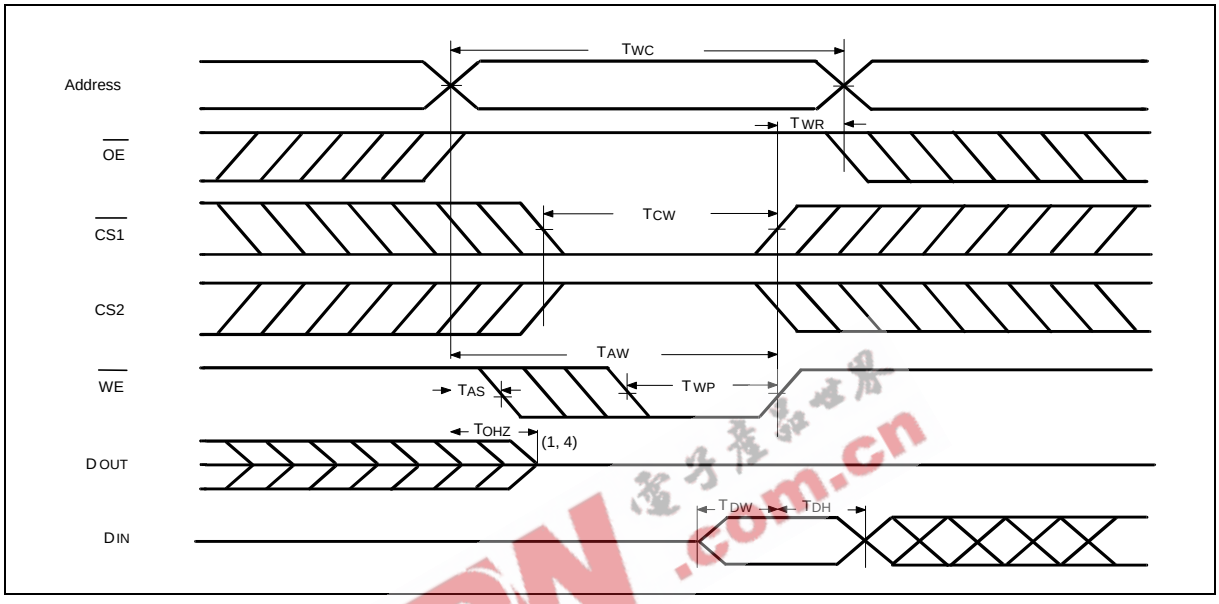
Read Cycle 3

(Output Enable Controlled)



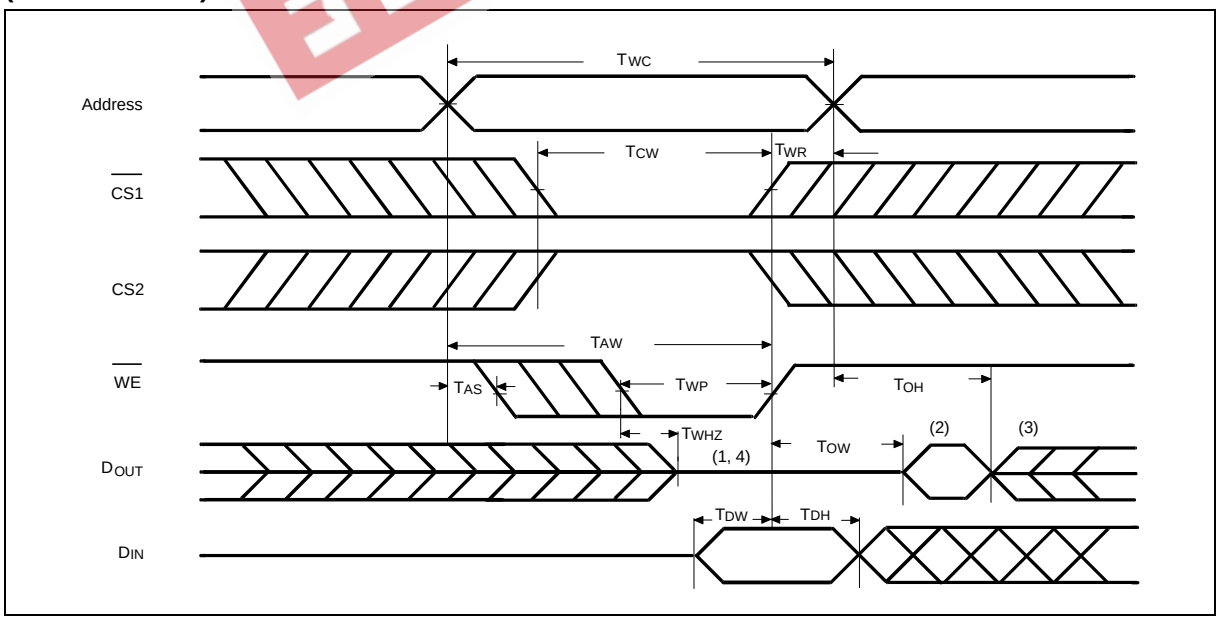
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:
1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

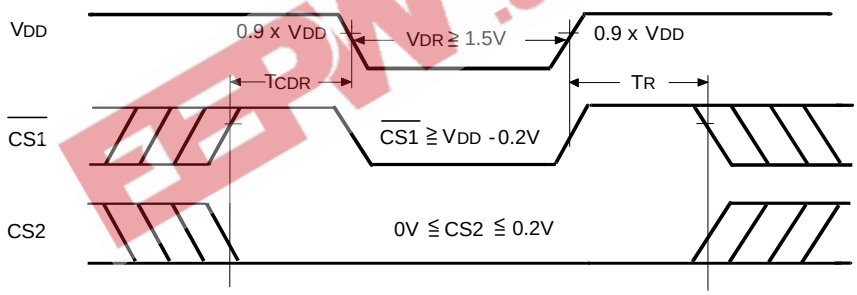
DATA RETENTION CHARACTERISTICS

(T_A (°C) = 0 to 70 for LL, -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{DD}$ -0.2V or CS2 ≤ 0.2V	1.5	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS1} \geq V_{DD}$ -0.2V or CS2 ≤ 0.2V, V_{DD} = 3V	-	-	5	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T_R		T_{RC}*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

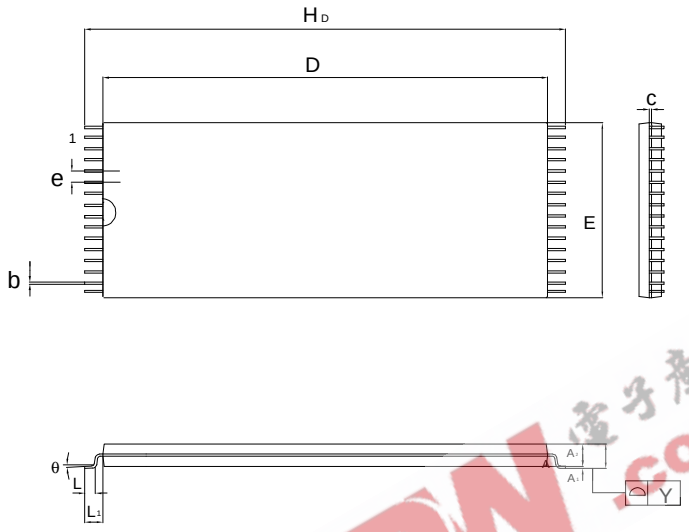
PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	PACKAGE
W24L01B-55LL	55	2.7V – 3.6V	0 to 70	CSP
W24L01Q-55LL	55	2.7V – 3.6V	0 to 70	Small type one TSOP
W24L01S-55LL	55	2.7V – 3.6V	0 to 70	450 mil SOP
W24L01T-55LL	55	2.7V – 3.6V	0 to 70	Standard type one TSOP
W24L01B-55LE	55	2.7V – 3.6V	-20 to 85	CSP
W24L01Q-55LE	55	2.7V – 3.6V	-20 to 85	Small type one TSOP
W24L01S-55LE	55	2.7V – 3.6V	-20 to 85	450 mil SOP
W24L01T-55LE	55	2.7V – 3.6V	-20 to 85	Standard type one TSOP
W24L01B-55LI	55	2.7V – 3.6V	-40 to 85	CSP
W24L01Q-55LI	55	2.7V – 3.6V	-40 to 85	Small type one TSOP
W24L01S-55LI	55	2.7V – 3.6V	-40 to 85	450 mil SOP
W24L01T-55LI	55	2.7V – 3.6V	-40 to 85	Standard type one TSOP
W24L01B-70LL	70	2.7V – 3.6V	0 to 70	CSP
W24L01Q-70LL	70	2.7V – 3.6V	0 to 70	Small type one TSOP
W24L01S-70LL	70	2.7V – 3.6V	0 to 70	450 mil SOP
W24L01T-70LL	70	2.7V – 3.6V	0 to 70	Standard type one TSOP
W24L01B-70LE	70	2.7V – 3.6V	-20 to 85	CSP
W24L01Q-70LE	70	2.7V – 3.6V	-20 to 85	Small type one TSOP
W24L01S-70LE	70	2.7V – 3.6V	-20 to 85	450 mil SOP
W24L01T-70LE	70	2.7V – 3.6V	-20 to 85	Standard type one TSOP
W24L01B-70LI	70	2.7V – 3.6V	-40 to 85	CSP
W24L01Q-70LI	70	2.7V – 3.6V	-40 to 85	Small type one TSOP
W24L01S-70LI	70	2.7V – 3.6V	-40 to 85	450 mil SOP
W24L01T-70LI	70	2.7V – 3.6V	-40 to 85	Standard type one TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

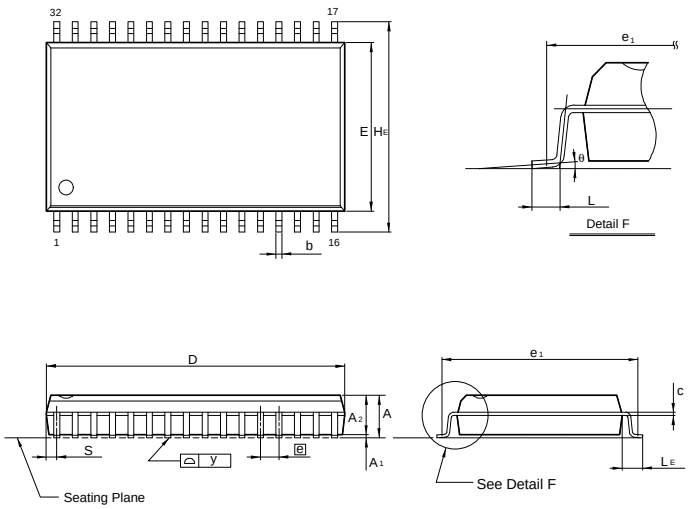
32-pin Small Type One TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.049	—	—	1.25
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.27
c	0.0056	0.0059	0.0062	0.14	0.15	0.16
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.520	0.528	0.536	13.20	13.40	13.60
e	—	0.020	—	—	0.50	—
L	0.012	0.020	0.028	0.30	0.50	0.70
L_1	0.027	—	—	0.675	—	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

32-pin SOP Wide Body

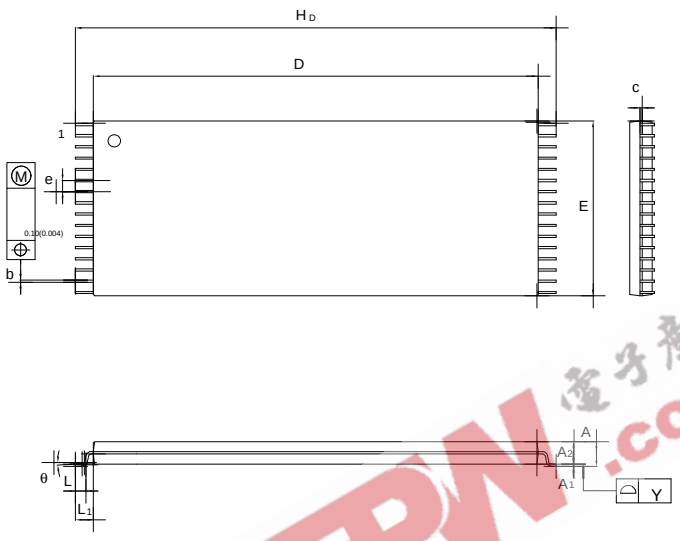


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.118	—	—	3.00
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	—	0.805	0.817	—	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.556	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	—	—	0.036	—	—	0.91
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches
5. General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

32-pin Standard Type One TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	DESCRIPTION
A1	Feb. 1998	Initial Issued
A2	Apr. 1998	Add standby power supply current (I_{SB1}) typical parameter when operation temperature T_A = 25° C
A3	June 1998	Change supply voltage range from (2.7V to 3.6V) to (2.3V to 3.3V)
A4	Oct. 1998	Add SOP package type
A5	Jan. 1999	Add SOP package pin configuration
A6	Jan. 2, 2002	Change supply voltage range from (2.3V – 3.3V) to (2.7V – 3.6V). Add 55 nS spec. Add LL grade.

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