# WCFS4008V1C

## 512K x 8 Static RAM

### Features

- **High speed**
  - **— $t_{AA}$ = 12 ns**
- **2.0V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

### Functional Description

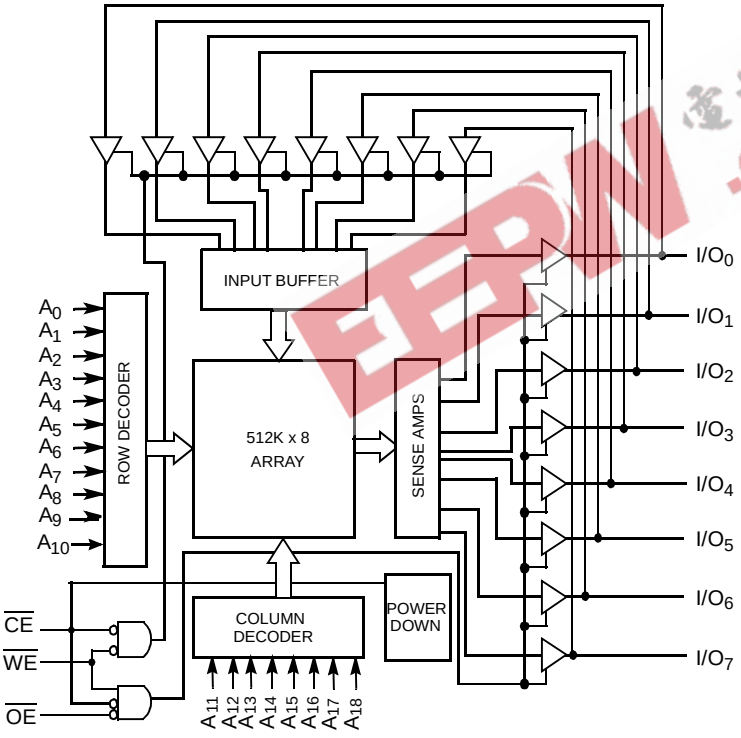
The WCFS4008V1C is a high-performance CMOS Static RAM organized as 524K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins ($I/O_0$ through $I/O_7$) is then written into the location specified on the address pins ($A_0$ through $A_{18}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

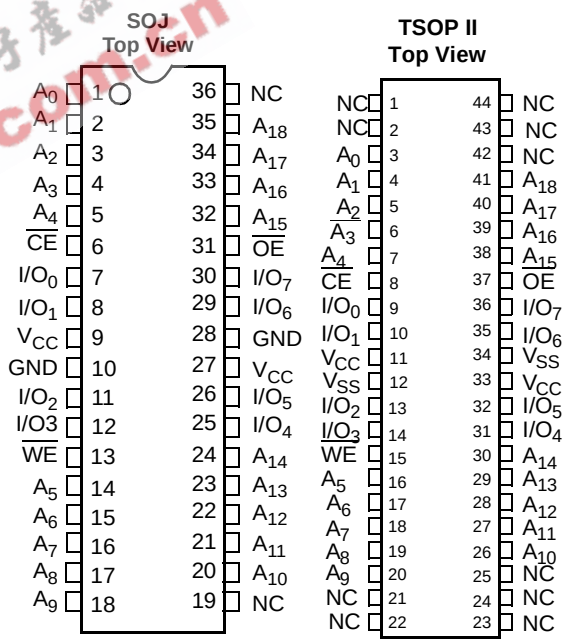
The eight input/output pins ($I/O_0$ through $I/O_7$) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The WCFS4008V1C is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground pinout.

### Logic Block Diagram




### Pin Configuration




### Selection Guide

| | | WCFS4008V1C 12ns |
|---|---|---|
| Maximum Access Time (ns) | | 12 |
| Maximum Operating Current (mA) | Comm'l | 85 |
| Maximum CMOS Standby Current (mA) | Comm'l | 10 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65×C to +150×C

Ambient Temperature with Power Applied.....–55×C to +125×C

Supply Voltage on $V_{CC}$ to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1] .....–0.5V to $V_{CC}$ + 0.5V

DC Input Voltage[1] ..... –0.5V to $V_{CC}$ + 0.5V

Current into Outputs (LOW) ..... 20 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 0.3V |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | WCFS4008V1C 12ns | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4.0 mA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | | –0.3 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output Disabled | | –1 | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., f = $f_{MAX}$ = $1/t_{RC}$ | Comm'l | | 85 | mA |
| $I_{SB1}$ | Automatic CE Power-Down Current —TTL Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$ $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | | | 40 | mA |
| $I_{SB2}$ | Automatic CE Power-Down Current —CMOS Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{CC}$ – 0.3V, $V_{IN}$ ≥ $V_{CC}$ – 0.3V, or $V_{IN}$ ≤ 0.3V, f = 0 | Comm'll | | 10 | mA |

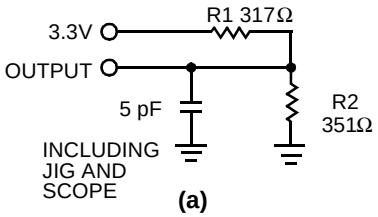
## Capacitance[2]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 8 | pF |
| $C_{OUT}$ | I/O Capacitance | | 8 | pF |

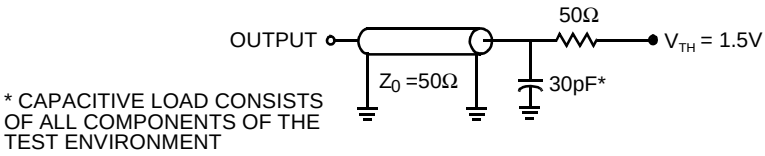
**Note:**

1. $V_{IL}$ (min.) = –2.0V for pulse durations of less than 20 ns
2. Tested initially and after any design or process changes that may affect these parameters.

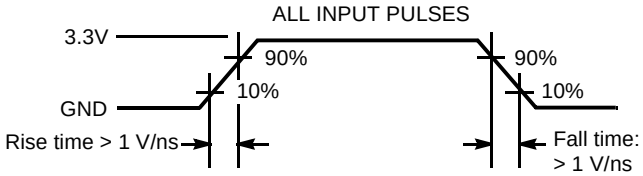
## AC Test Loads and Waveforms




(a)




(b)




(c)

## AC Switching Characteristics[3] Over the Operating Range

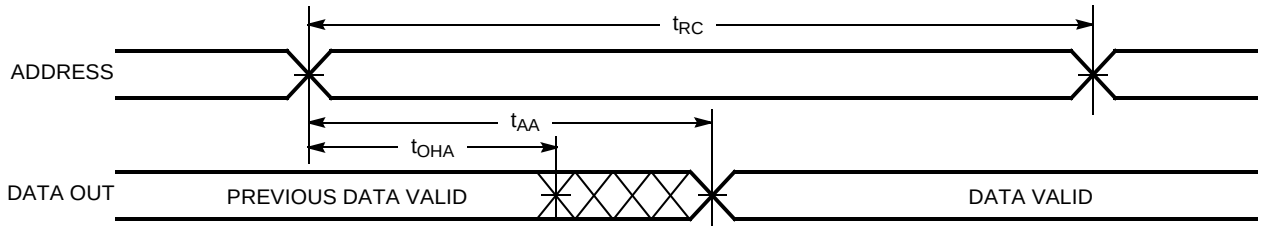
| Parameter | Description | WCFS4008V1C 12ns | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **READ CYCLE** | | | | |
| $t_{power}$[4] | $V_{CC}$(typical) to the first access | 1 | | ns |
| $t_{RC}$ | Read Cycle Time | 12 | | ns |
| $t_{AA}$ | Address to Data Valid | | 12 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 3 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 12 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 6 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 0 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[5, 6] | | 6 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z[6] | 3 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z[5, 6] | | 6 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power-Up | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power-Down | | 12 | ns |
| **WRITE CYCLE**[7, 8] | | | | |
| $t_{WC}$ | Write Cycle Time | 12 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 8 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 8 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 8 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 6 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[6] | 3 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[5, 6] | | 6 | ns |

**Notes:**

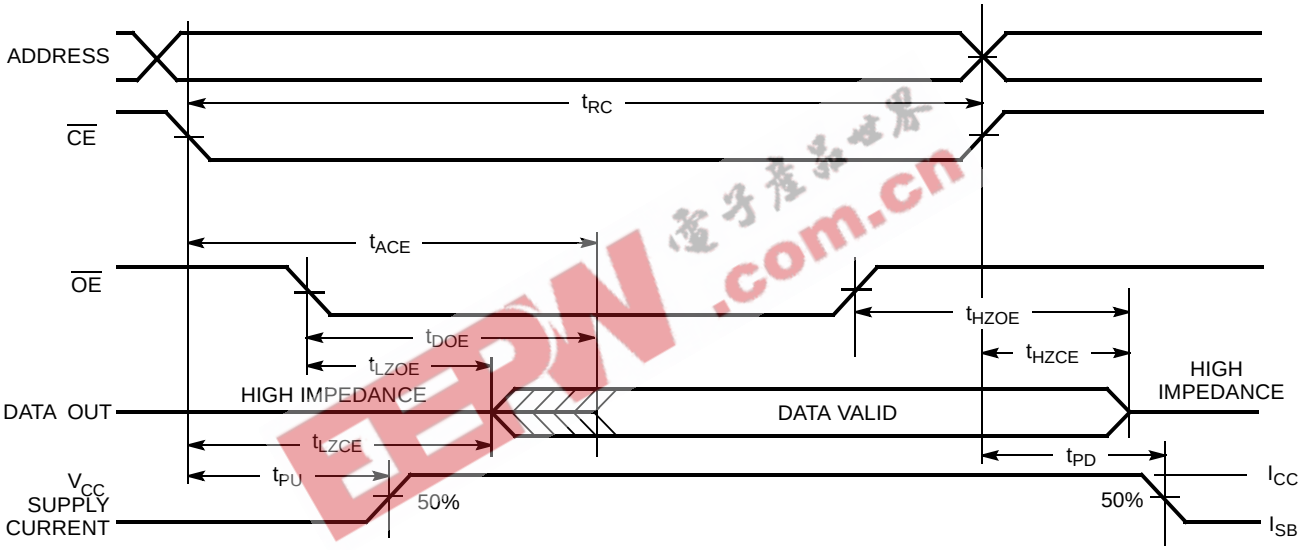
3. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
4. $t_{POWER}$ gives the minimum amount of time that the power supply should be at stable, typical Vcc values until the first memory access can be performed.
5. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
7. The internal write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

### Read Cycle No. 1[9, 10]




### Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]

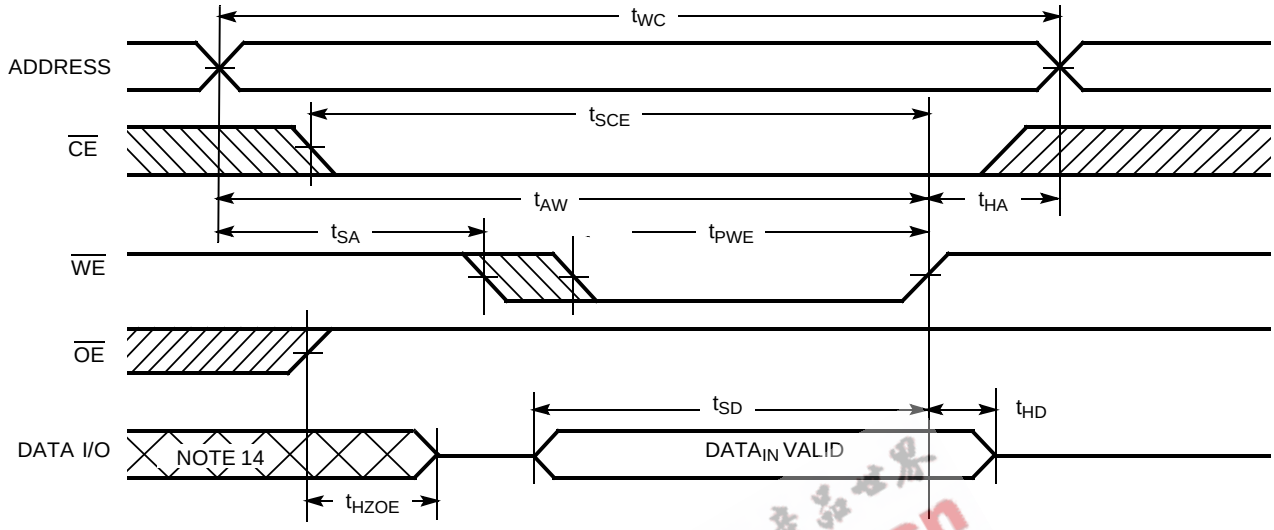



**Notes:**

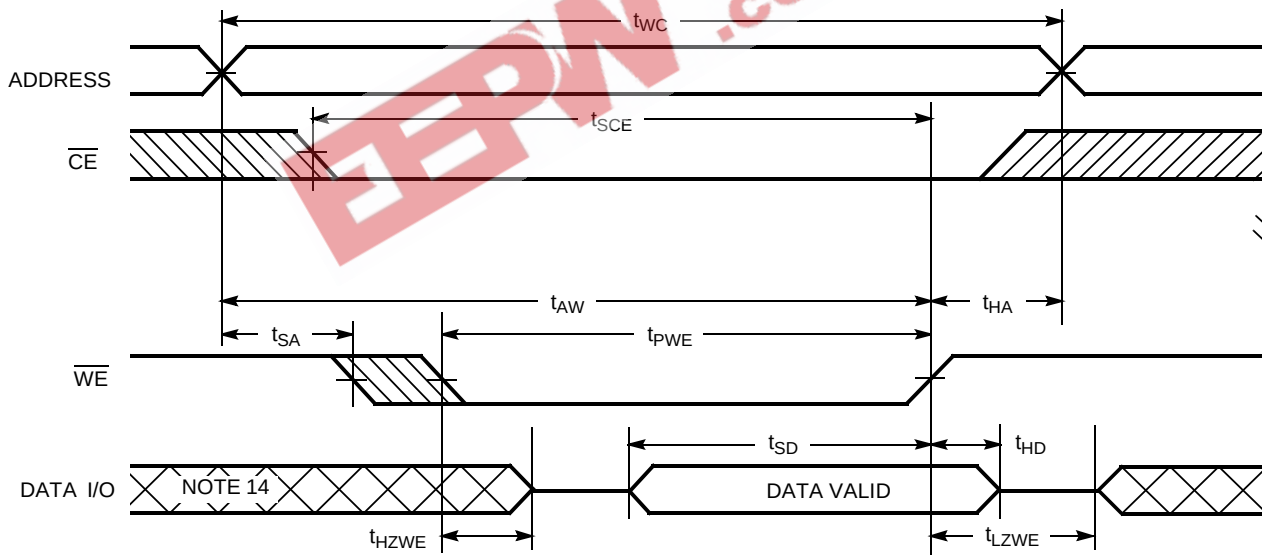
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1(WE Controlled, OE HIGH During Write)[12, 13]




### Write Cycle No. 2 (WE Controlled, OE LOW)[13]




## Truth Table

| CE | OE | WE | $I/O_0 - I/O_7$ | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Power-Down | Standby ($I_{SB}$) |
| L | L | H | Data Out | Read | Active ($I_{CC}$) |
| L | X | L | Data In | Write | Active ($I_{CC}$) |
| L | H | H | High Z | Selected, Outputs Disabled | Active ($I_{CC}$) |

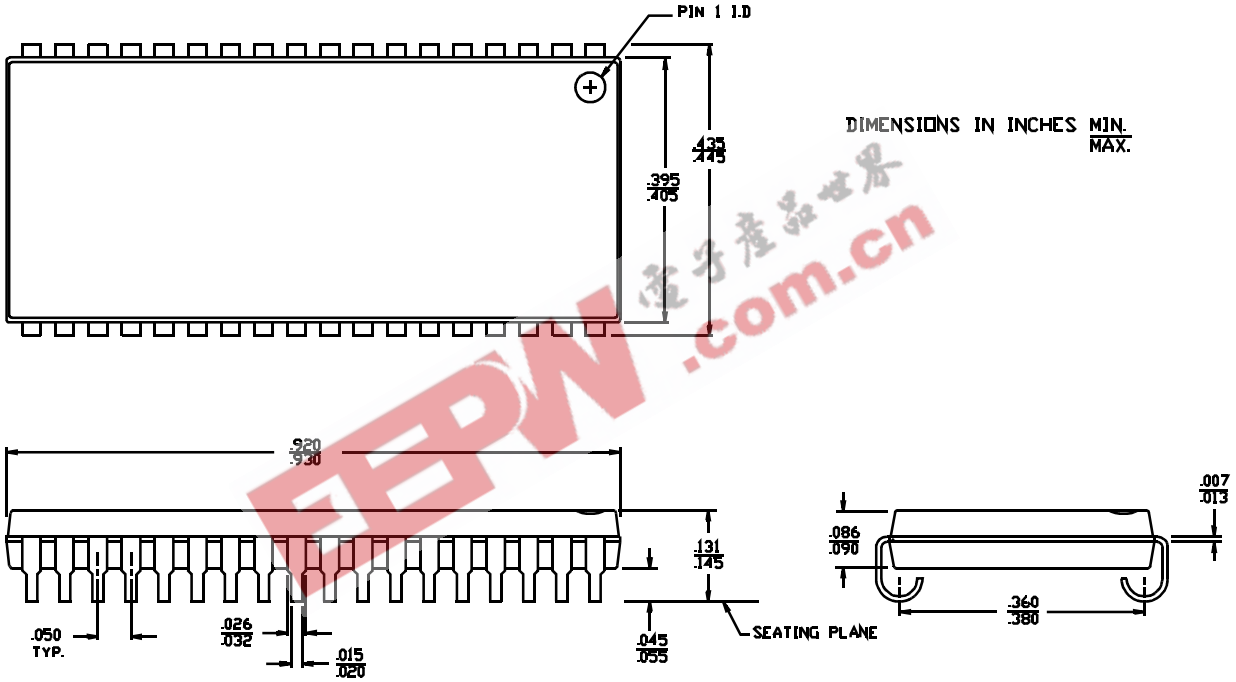
**Notes:**
12. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 12 | WCFS4008V1C-JC12 | J | 36-Lead (400-Mil) Molded SOJ | Commercial |
| | WCFS4008V1C-TC12 | T | 44-pin TSOP II | |

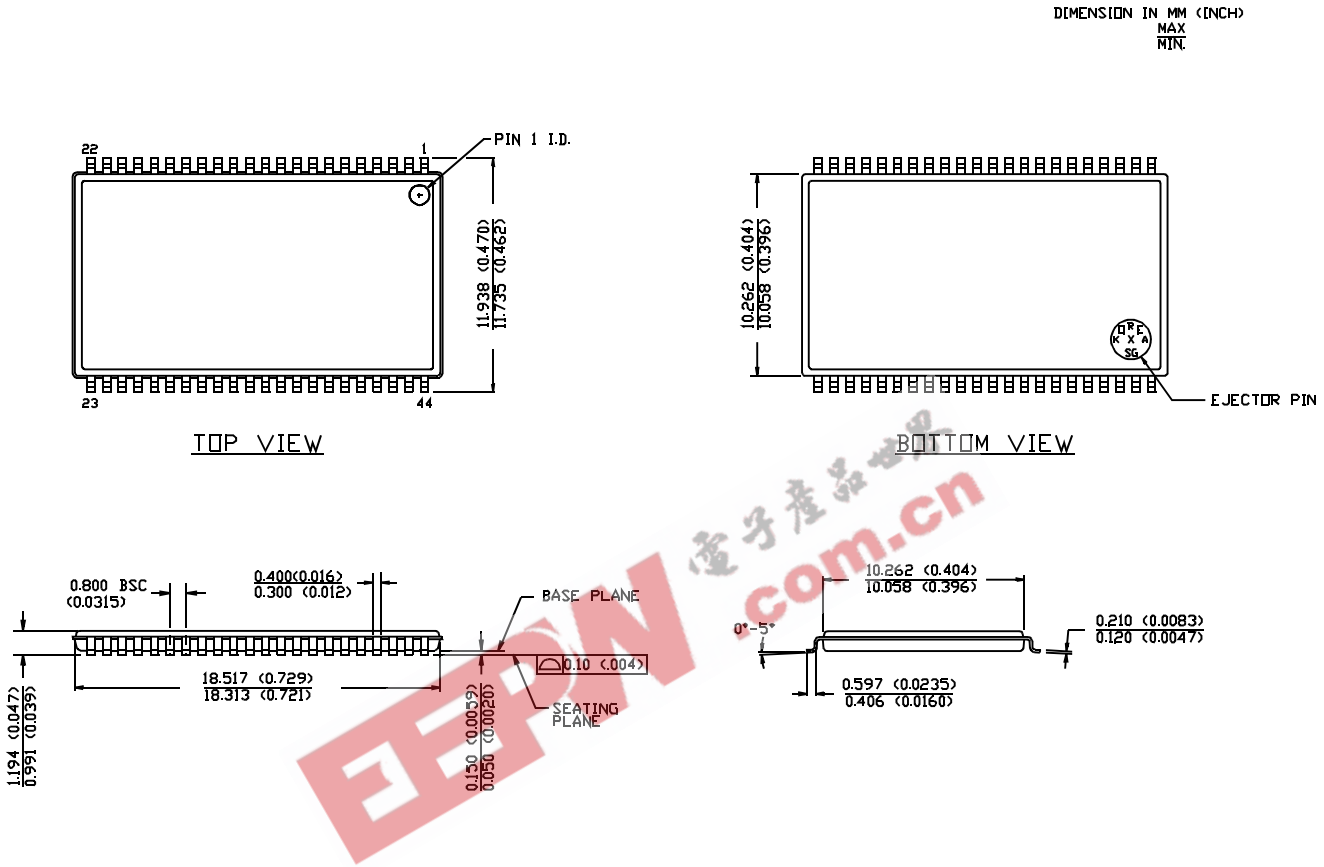
## Package Diagrams

**36-Lead (400-Mil) Molded SOJ J**



## Package Diagrams (continued)

**44-Pin TSOP II T**



# 512K x 8 Static RAM

## Revision History

| Document Title: WCFS4008V1C 32K x 8 3.3V Static RAM | | | |
|---|---|---|---|
| **REV.** | **ISSUE DATE** | **ORIG. OF CHANGE** | **DESCRIPTION OF CHANGE** |
| ** | 4/12/2002 | XFL | New Datasheet |