

Preliminary W24100



128K × 8 CMOS STATIC RAM

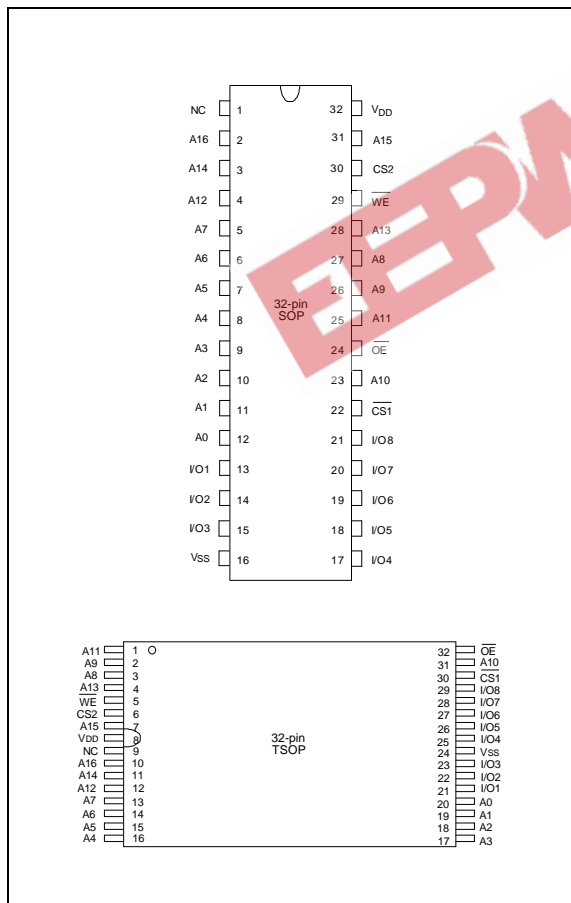
GENERAL DESCRIPTION

The W24100 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

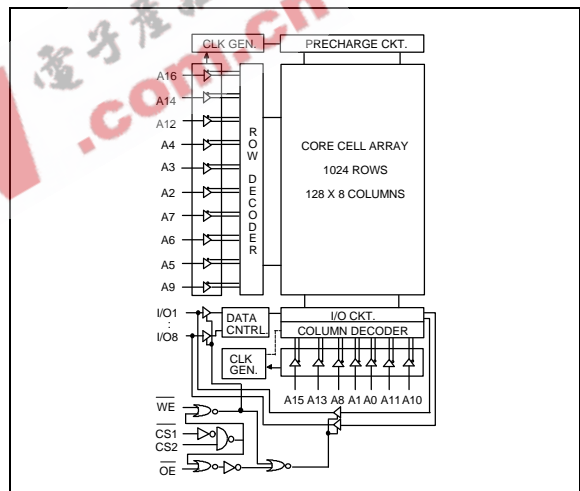
FEATURES

- Low power consumption:
 - Active: 385 mW (max.)
- Access time: 70 nS
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 32-pin 600 mil DIP, 450 mil SOP, standard type one TSOP (8 mm × 20 mm) and small type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

Preliminary W24100



TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to VSS Potential	-0.5 to +7.0	V
Input/Output to VSS Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to 70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VDD = 5V ±10%; VSS = 0V; TA = 0° C to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.*	MAX.	UNIT
Input Low Voltage	VIL	-	-0.5	-	+0.8	V
Input High Voltage	VIH	-	+2.2	-	VDD+0.5	V
Input Leakage Current	ILI	VIN = VSS to VDD	-1	-	+1	μA
Output Leakage Current	ILO	VIO = VSS to VDD, CS1 = VIH (min.) or OE = VIH (min.) or WE = VIL (max.)	-1	-	+1	μA
Output Low Voltage	VOL	IOL = +2.1 mA	-	-	0.4	V
Output High Voltage	VOH	IOH = -1.0 mA	2.4	-	-	V
Operating Power Supply Current	IDD	CS1 = VIL (max.) and CS2 = VIH (min.), I/O = 0 mA Cycle = min., Duty = 100%	-	-	70	mA
Standby Power Supply Current	ISB	CS = VIH (min.), Cycle = min. Duty = 100%	-	-	3	mA
	ISB1	CS1 ≥ VDD -0.2V or CS2 ≤ 0.2V	LL	-	-	50
L			-	-	100	μA

Note: Typical parameter is measured under ambient temperature TA = 25° C and VDD = 5V.

Preliminary W24100



CAPACITANCE

(V_{DD} = 5 V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

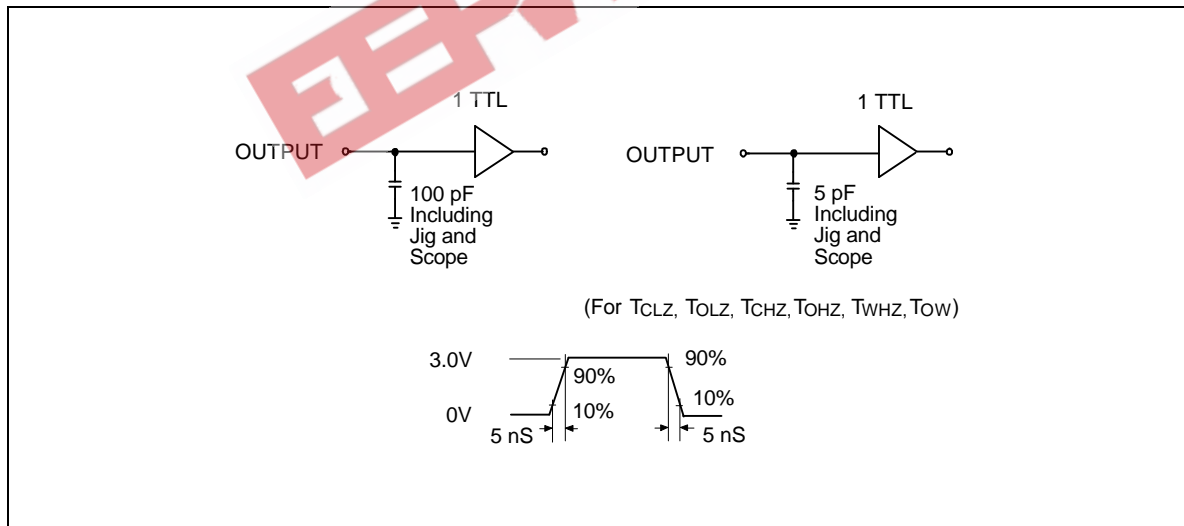
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



Preliminary W24100



AC Characteristics, continued

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = 0° C to 70° C)

Read Cycle

PARAMETER	SYM.	W24100-70L		W24100-70LL		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	70	-	70	-	nS
Address Access Time	TAA	-	70	-	70	nS
Chip Select Access Time	TACS	-	70	-	70	nS
Output Enable to Output Valid	TAOE	-	35	-	35	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	30	-	30	nS
Output Hold from Address Change	TOH	10	-	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

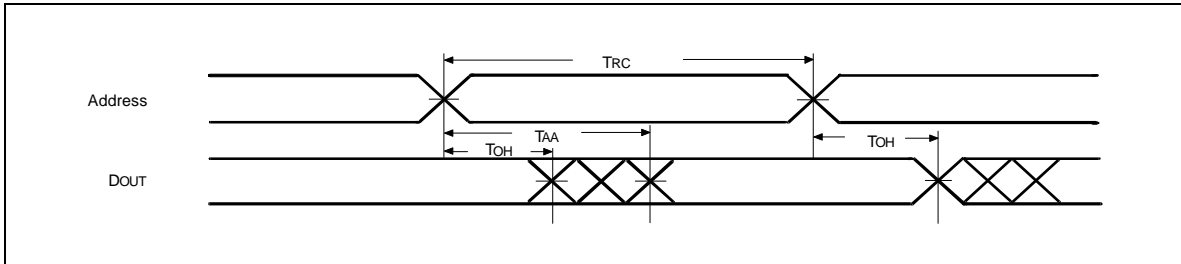
PARAMETER	SYM.	W24100-70L		W24100-70LL		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	TWC	70	-	70	-	nS
Chip Selection to End of Write	TCW	50	-	50	-	nS
Address Valid to End of Write	TAW	50	-	50	-	nS
Address Setup Time	TAS	0	-	0	-	nS
Write Pulse Width	TWP	50	-	50	-	nS
Write Recovery Time	TWR	0	-	0	-	nS
	$\overline{CS1}$, $\overline{CS2}$, \overline{WE}					
Data Valid to End of Write	TDW	30	-	30	-	nS
Data Hold from End of Write	TDH	0	-	0	-	nS
Write to Output in High Z	TWHZ*	-	25	-	25	nS
Output Disable to Output in High Z	TOHZ*	-	25	-	25	nS
Output Active from End of Write	TOW	5	-	5	-	nS

* These parameters are sampled but not 100% tested

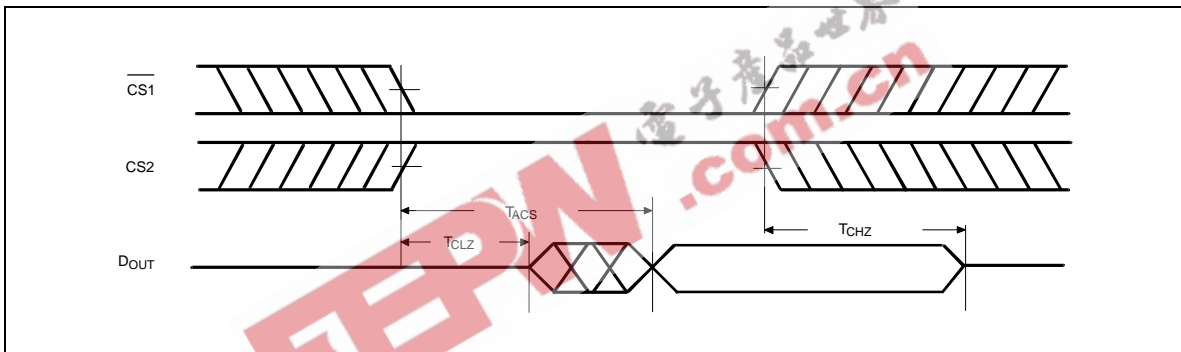


TIMING WAVEFORMS

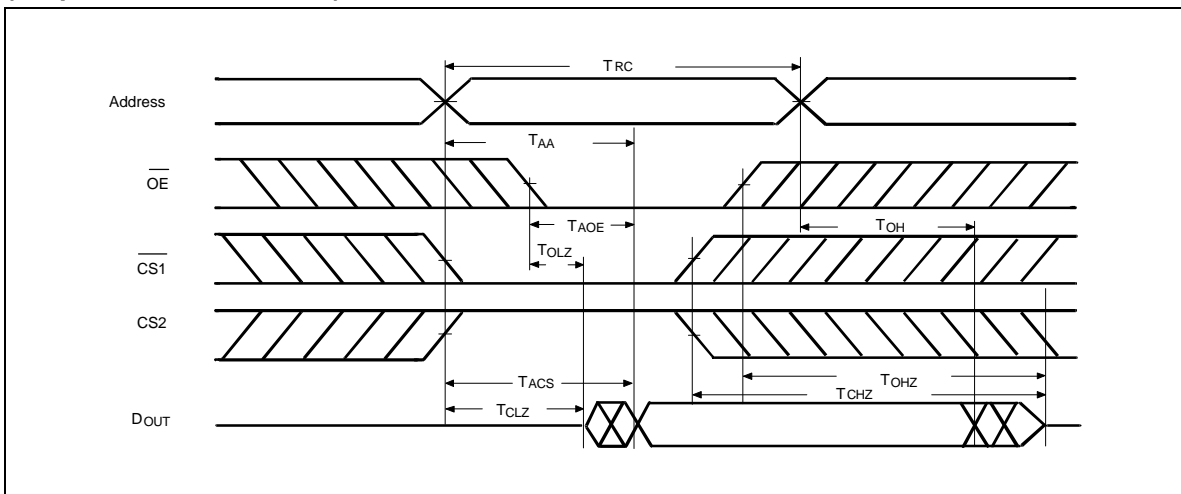
**Read Cycle 1
(Address Controlled)**



**Read Cycle 2
(Chip Select Controlled)**



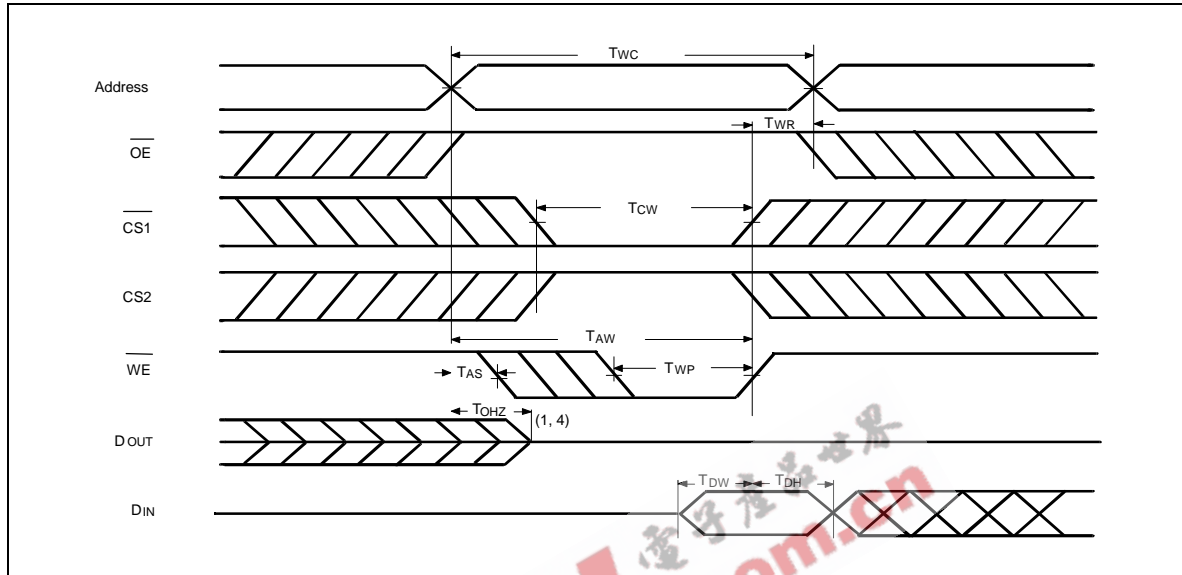
**Read Cycle 3
(Output Enable Controlled)**





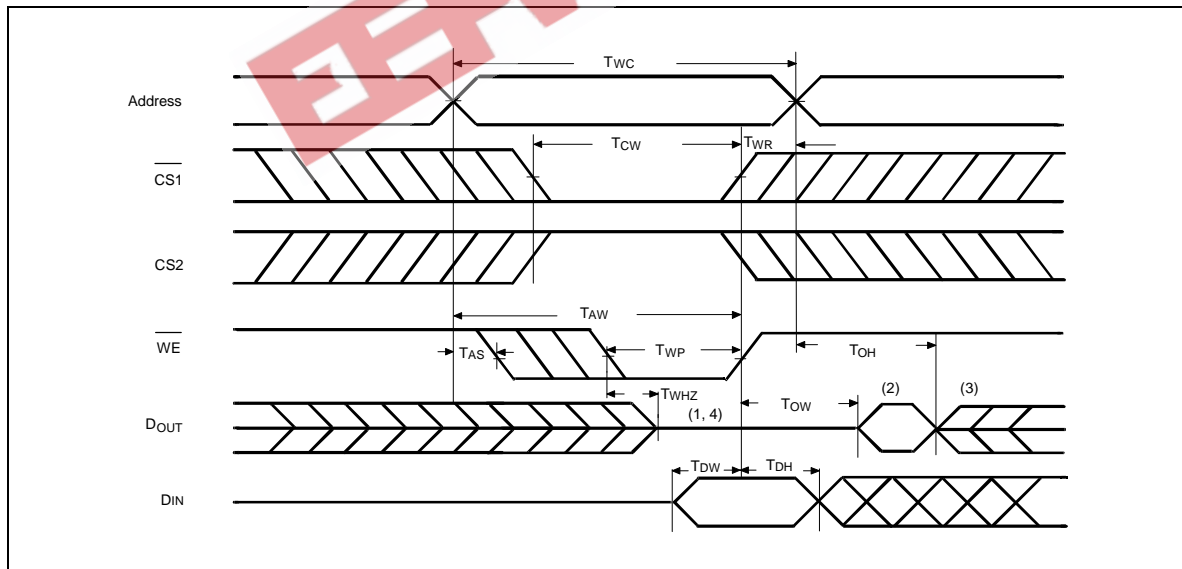
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.



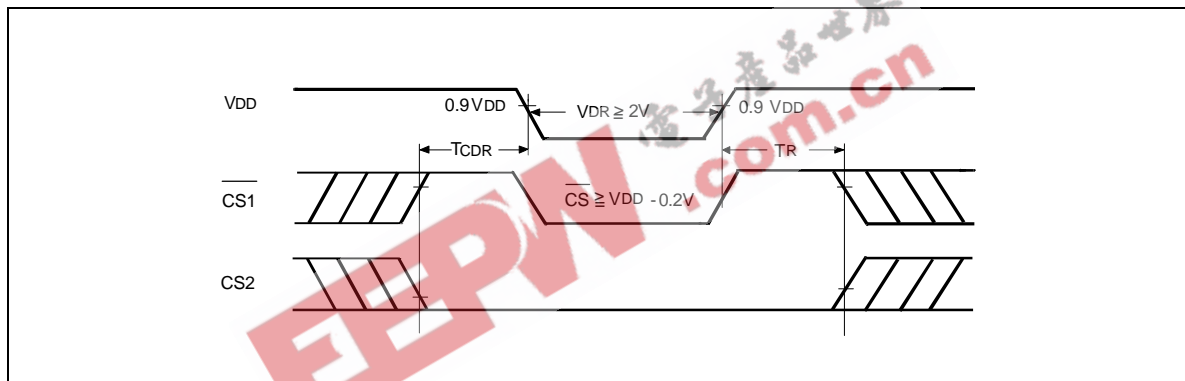
DATA RETENTION CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to 70°C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{\text{CS}} \geq V_{\text{DD}} - 0.2\text{V}$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{\text{CS}} \geq V_{\text{DD}} - 0.2\text{V}$, $V_{\text{DD}} = 3\text{V}$	-	-	50	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	TR		TRC*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



Preliminary W24100

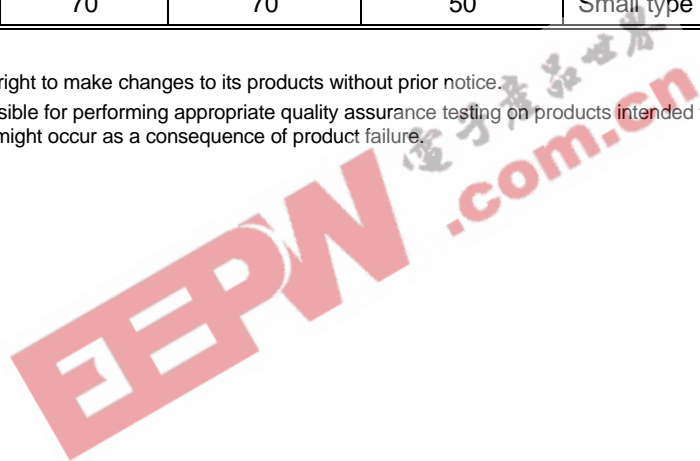


ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24100-70L	70	70	100	600 mil DIP
W24100-70LL	70	70	50	600 mil DIP
W24100S-70L	70	70	100	450 mil SOP
W24100S-70LL	70	70	50	450 mil SOP
W24100T-70L	70	70	100	Standard type one TSOP
W24100T-70LL	70	70	50	Standard type one TSOP
W24100Q-70L	70	70	100	Small type one TSOP
W24100Q-70LL	70	70	50	Small type one TSOP

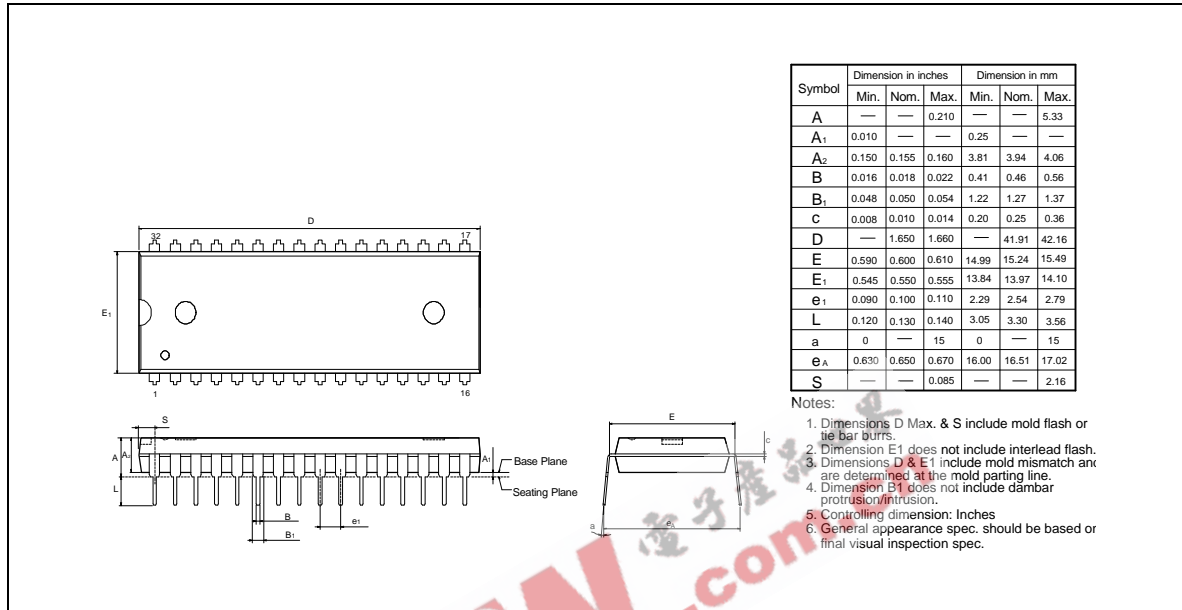
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

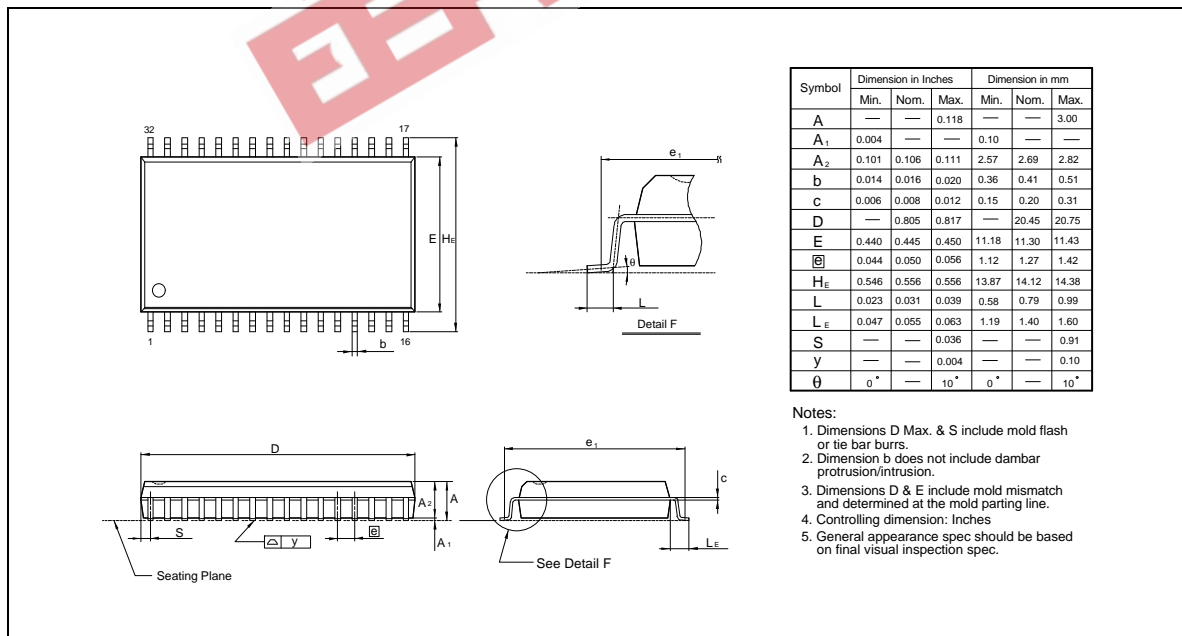


PACKAGE DIMENSIONS

32-pin P-DIP

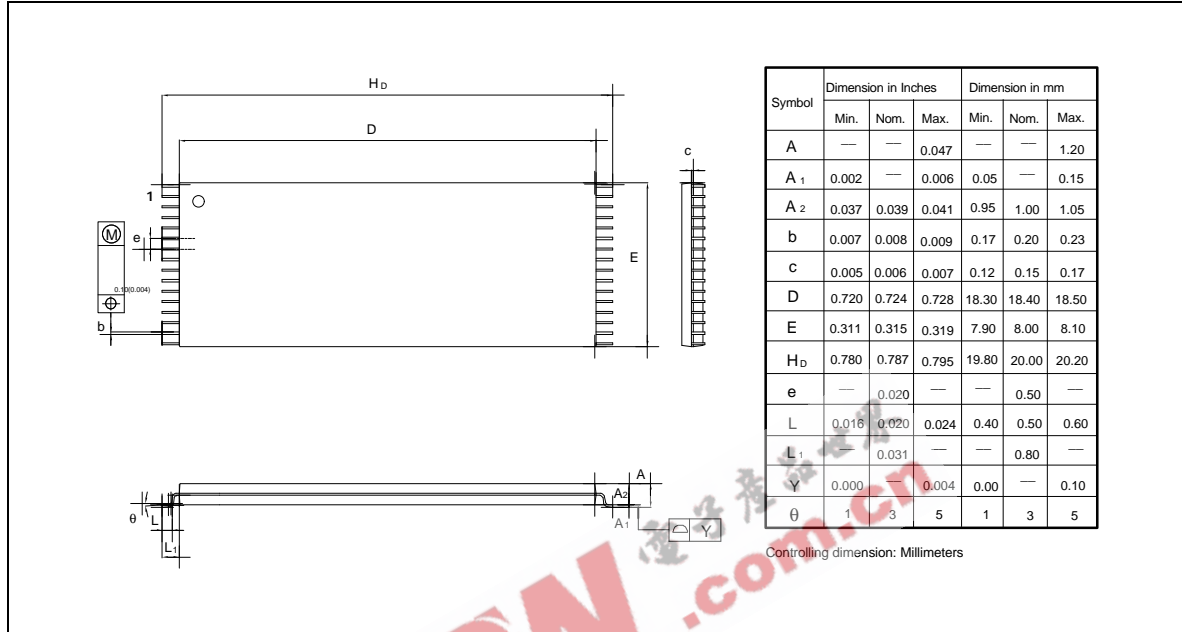


32-pin SOP Wide Body

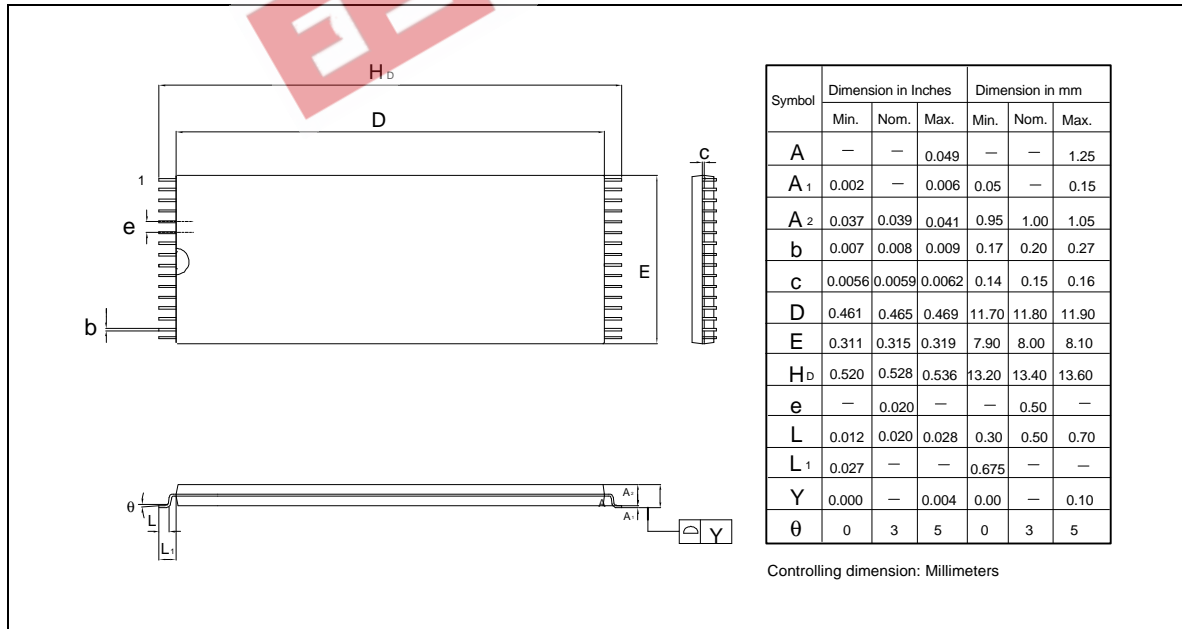


Package Dimensions, continued

32-pin Standard Type One TSOP



32-pin Small Type One TSOP



Preliminary W24100



VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 1999	-	Initial Issued

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Note: All data and specifications are subject to change without notice.