



WM5620L, WM5620

Production Data
Sept. 1996 Rev 2

3 & 5V Quad 8-Bit Voltage Output DAC with Serial Interface

Description

WM5620L and WM5620 are quad 8-bit digital to analogue converters (DAC) controlled via a serial interface. Each DAC's output voltage range is programmable for either x1 or x2 its reference input voltage, allowing near rail to rail operation for the x2 output range. Separate high impedance buffered voltage reference inputs are provided for each DAC. WM5620L operates on a single supply voltage of 3 V while WM5620 operates on 5 V.

WM5620/L interfaces to all popular microcontrollers and microprocessors via a three wire serial interface with CMOS compatible, schmitt trigger, digital inputs. An 11 bit command word comprises 2 DAC select bits, an output range selection bit and 8-bits of data.

Individual or all DAC outputs are changed using WM5620/L's double buffered DAC registers and the separate LOAD and LDAC inputs. DAC outputs are updated simultaneously by writing a complete set of new values and then pulsing the LDAC input.

The DAC outputs are optimised for single supply operation and driving ground referenced loads.

An internal power-on-reset function sets the DAC's input codes to zero at power up.

Ideal in space critical applications WM5620/L is available in small outline and DIP packages for commercial (0°C to 70°C) and industrial (-40°C to 85°C) temperature ranges.

Features

- Four 8-bit voltage output DAC's
- Three wire serial interface
- Programmable x1 or x2 output range.
- Power-on-reset sets outputs to zero
- Buffered voltage reference inputs
- Simultaneous DAC output update
- 14 pin SO or DIP package

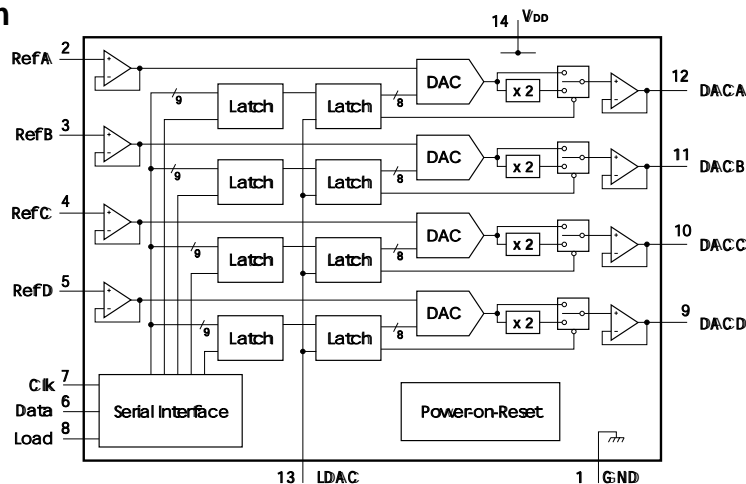
Key Specifications

- Single supply operation:
 - WM5620L : 3 V
 - WM5620 : 5 V
- 0 to 4 V output (x2 output range) at 5 V VDD
- 0 to 2.5 V output (x2 output range) at 3 V VDD
- Low power: 5.1 mW at 3 V, 10 mW at 5 V max.
- Guaranteed monotonic output

Applications

- Programmable d.c. voltage sources
- Digitally controlled attenuator/amplifier
- Signal synthesis
- Mobile communications
- Automatic test equipment
- Process control

Block Diagram



Production Data data sheets contain final specifications current on publication date. Supply of products conforms to Wolfson Microelectronics standard terms and conditions

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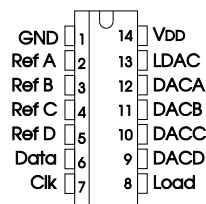
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WM5620L, WM5620

Pin Configuration

Top View N and D packages



Ordering Information

DEVICE	TEMP. RANGE	PACKAGE
WM5620CN	0°C to 70°C	14 pin plastic DIP
WM5620CD	0°C to 70°C	14 pin plastic SO
WM5620IN	-40°C to 85°C	14 pin plastic DIP
WM5620ID	-40°C to 85°C	14 pin plastic SO
WM5620LCN	0°C to 70°C	14 pin plastic DIP
WM5620LCD	0°C to 70°C	14 pin plastic SO
WM5620LIN	-40°C to 85°C	14 pin plastic DIP
WM5620LID	-40°C to 85°C	14 pin plastic SO

Absolute Maximum Ratings (note 1)

Supply Voltage (VDD - VGND) +7V
 Digital Inputs GND - 0.3 V, VDD + 0.3 V
 Reference inputs GND - 0.3 V, VDD + 0.3 V

Operating temperature range, TA TMIN to TMAX
 WM5620_C 0°C to +70°C
 WM5620_I -40°C to +85°C
 Storage Temperature -50°C to +150°C
 Lead Temperature 1.6mm (1/16 inch) from case
 (soldering, 10 sec) + 260°C

Recommended Operating Conditions

	SYMBOL	MIN	NOMINAL	MAX	UNIT
Supply voltage WM5620	VDD	4.75		5.25	V
Supply Voltage WM5620L	VDD	2.7	3.3	5.25	V
Reference input range x1 gain	VREF [A/B/C/D]			VDD - 1.5	V
DAC output load resistance to GND	RL	10			kΩ
High level digital input voltage	VIH	0.8 VDD			V
Low level digital input voltage	VIL			0.8	V
Clock frequency	FCLK			1	MHz

Electrical Characteristics: WM5620

VDD = 5 V, GND = 0 V, VREF = 2 V, RL = 10 kΩ, CL = 100 pF, TA = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
Supply current	IDD	VDD = 5V			2	mA
Static Accuracy						
Resolution			8			Bits
Monotonicity			8			Bits
Differential Nonlinearity	DNL	VREF = 2 V, Range x 2. (note 3)		± 0.1	± 0.9	LSB
Integral Nonlinearity	INL	VREF = 2 V, Range x 2. (note 4)			± 1.0	LSB
Zero-code error	ZCE	VREF = 2 V, Range x 2. (note 5)	0		30	mV
Zero-code error temperature coefficient		Input code = 00 Hex (note 6)		10		μV/°C
Zero-code error supply rejection		Input code = 00 Hex (note 7)		0.5		mV/V

WM5620L, WM5620

Electrical Characteristics: WM5620

V_{DD} = 5V ±5%, GND = 0 V, V_{REF} = 2 V, R_L = 10 kΩ, C_L = 100 pF, T_A = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full scale error	FSE	V _{REF} = 2 V, Range x 2. (note 8)			± 60	mV
Full scale error temperature coefficient		Input code = FF Hex (note 9)		± 25		μV/°C
Full scale error supply rejection		Input code= FF Hex, (note 10)		0.5		mV/V
Output sink current	I _{O(SINK)}	Each DAC output	20			μA
Output source current	I _{O(SOURCE)}		2			mA
Reference input current	I _{REF}	V _{DD} =5V, V _{REF} =2V			± 10	μA

Electrical Characteristics: WM5620L

V_{DD} = 3V, GND = 0 V, V_{REF} = 1.25 V, R_L = 10 kΩ, C_L = 100 pF, T_A = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
Supply current	I _{DD}	V _{DD} = 3.3V			2	mA
Static Accuracy						
Resolution			8			Bits
Monotonicity			8			Bits
Differential Nonlinearity	DNL	V _{REF} = 1.25 V, Range x 2. (note 3)			± 0.9	LSB
Integral Nonlinearity	INL	V _{REF} = 1.25 V, Range x 2. (note 4)			± 1.0	LSB
Zero-code error	ZCE	V _{REF} = 1.25 V, Range x 2. (note 5)	0		30	mV
Zero-code error temperature coefficient		Input code = 00 Hex (note 6)		10		μV/°C
Full scale error	FSE	V _{REF} = 1.25 V, Range x 2. (note 8)			± 60	mV
Full scale error temperature coefficient		Input code = FF Hex (note 9)		± 25		μV/°C
Output sink current	I _{O(SINK)}	Each DAC output	20			μA
Output source current	I _{O(SOURCE)}		1			mA
Ref. input current	I _{REF}	V _{DD} = 3.3V; V _{ref} = 1.5V			±10	μA

Electrical Characteristics: WM5620 & WM5620L

V_{DD} = 2.7V to 5.5V, GND = 0 V, R_L = 10 kΩ, C_L = 100 pF, T_A = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
High level input current	I _{IH}	V _I = V _{DD}			±10	μA
Low level input current	I _{IL}	V _I = 0V			±10	μA
Input capacitance	C _I			15		pF
Timing Parameters						
Data input setup time	t _{SD}		50			ns
Data input hold time	t _{HD}		50			ns
CLK ↓ to Load ↓	t _{HL}		50			ns
Load ↑ to CLK ↓	t _{SL}		50			ns
Load duration	t _{WL}		250			ns
LDAC duration	t _{WD}		250			ns
Load ↓ to LDAC ↓	t _{LD}		0			ns

WM5620L, WM5620

Electrical Characteristics: WM5620 & WM5620L

$V_{DD} = 2.7V$ to $5.5V$, $GND = 0V$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_A =$ full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Inputs						
Reference input voltage	V_{REF}	A, B, C, D, inputs	GND		$V_{DD} - 1.5$	V
Reference input capacitance		A, B, C, D, inputs		15		pF
Reference feedthrough		A, B, C, D, inputs (note 11)		-60		dB
Channel to channel isolation		A, B, C, D, inputs (note 12)		-60		dB
Dynamic Performance						
Output settling time		To 1/2 LSB, $V_{DD} = 3V$ & $5V$ (note 13)		10		μs
Output slew rate				1		$V/\mu\text{s}$
Input bandwidth		(note 14)		100		kHz
Large Signal Bandwidth		Measured at -3dB point		100		kHz
Digital Crosstalk		Clk = 1MHz sq wave measured at DACA - DACD		-50		dB

Electrical Characteristics: WM5620 & WM5620L (continued)

Notes:

- Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating range limits are given under Recommended Operating Conditions. Guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.
- Total Unadjusted Error is the sum of integral linearity error, zero code error and full scale error over the input code range.
- Differential Nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
- Integral Nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
- Zero code error is the deviation from zero voltage output when the digital input code is zero.
- Zero code error temperature coefficient is given by:

$$ZCETC = (ZCE(T_{max}) - ZCE(T_{min})) / V_{REF} \times 10^6 / (T_{max} - T_{min})$$
- Zero-code Error Rejection Ratio (ZCE-RR) is measured by varying the V_{DD} voltage, from 4.5 to 5.5 V d.c., and measuring the proportion of this signal imposed on the zero-code output voltage.
- Full-scale error is the deviation from the ideal full-scale output ($V_{REF} - 1\text{ LSB}$) with an output load of $10\text{ k}\Omega$
- Full-Scale Temperature Coefficient is given by:

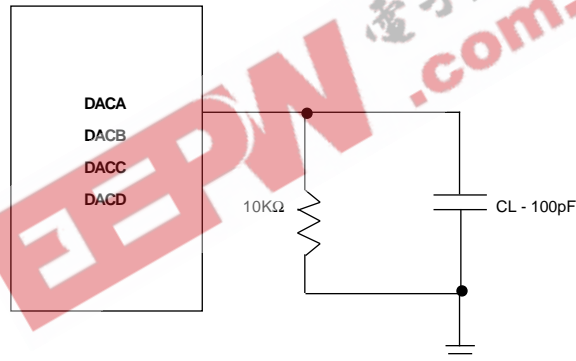
$$FSETC = (FSE(T_{max}) - FSE(T_{min})) / V_{REF} \times 10^6 / (T_{max} - T_{min})$$
- Full Scale Error Rejection Ratio (FSE-RR) is measured by varying the V_{DD} voltage, from 4.5 to 5.5 V d.c., and measuring the proportion of this signal imposed on the full-scale output voltage.

WM5620L, WM5620

Electrical Characteristics: WM5620 & WM5620L (continued)

- 11 Reference feedthrough is measured at a DAC output with an input code = 00 Hex with a VREF input = $1 V_{dc} + 1 V_{pp}$ at 10kHz
- 12 Channel to channel isolation is measured at a DAC output with an input code of one DAC to FF Hex and the code on all other DACs to 00 Hex with a VREF input = $1 V_{dc} + 1 V_{pp}$ at 10kHz
- 13 Setting time is the time for the output signal to remain within ± 0.5 LSB of the final measurement value for a digital input code change of 00 Hex to FF Hex. For WM5620: $V_{DD} = 5V$, $V_{REF} = 2V$ and range = x 2. For WM5620L: $V_{DD} = 3V$, $V_{REF} = 1.25V$ and range = x 2.
- 14 Reference bandwidth is the -3dB bandwidth with an input at $V_{REF} = 1.25 V_{dc} \pm 2 V_{pp}$ with a digital input code of full-scale

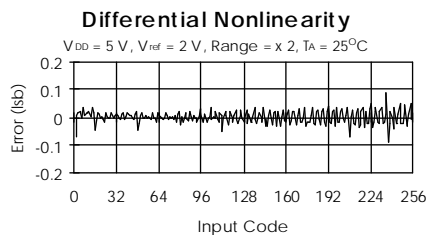
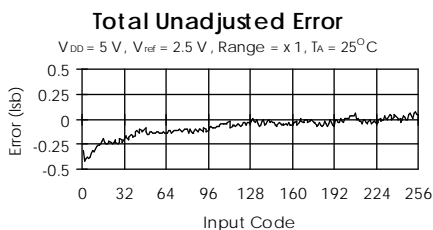
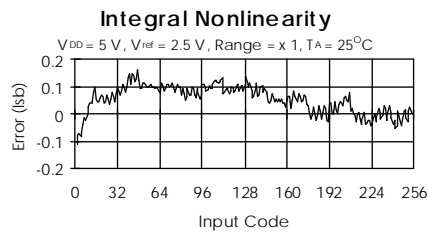
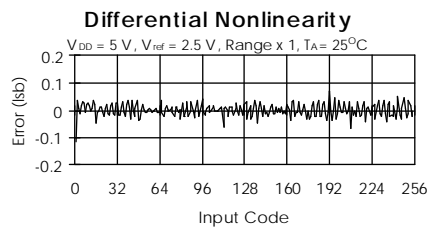
Parameter Measurement Information



Slewing Settling Time and Linearity Measurements

Typical Performance Characteristics

Typical DNL, INL and TUE * at $V_{DD} = 5V$

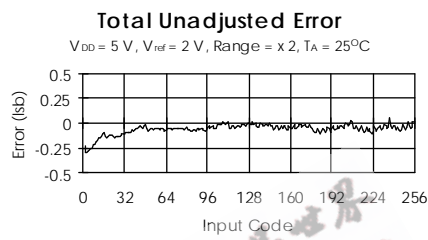
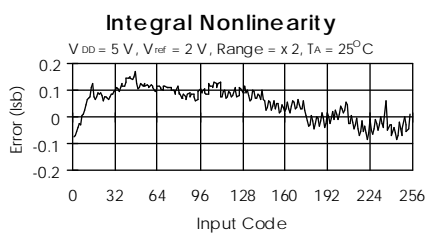


* see note 2

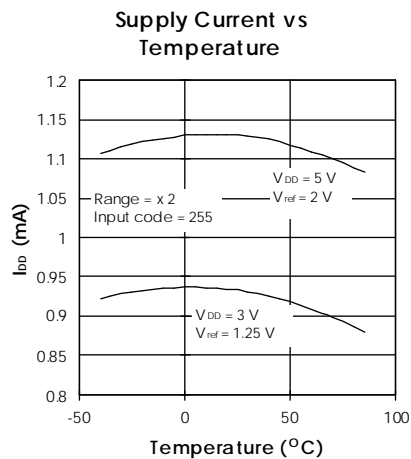
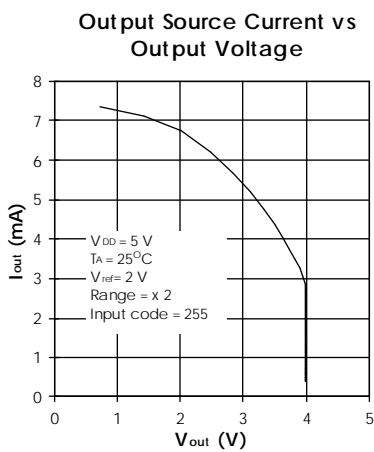
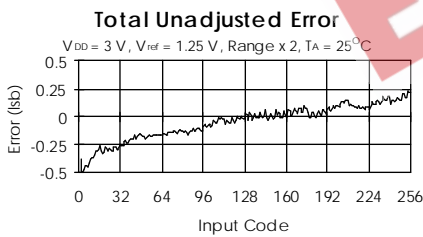
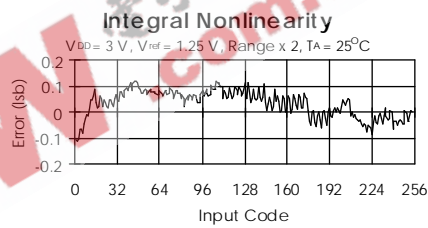
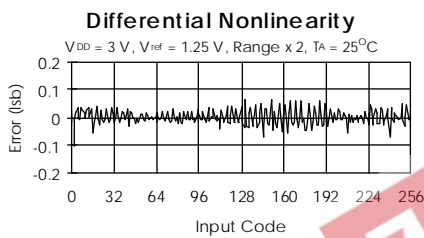
WM5620L, WM5620

Typical Performance Characteristics (Continued)

Typical DNL, INL and TUE * at $V_{DD} = 5\text{ V}$



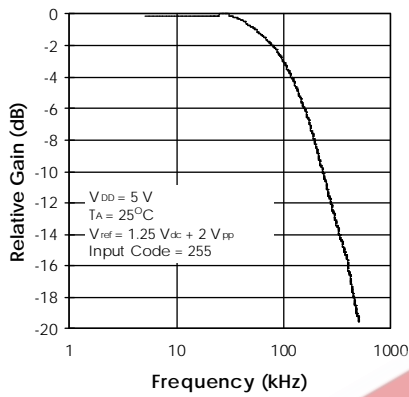
Typical DNL, INL and TUE at $V_{DD} = 3\text{ V}$



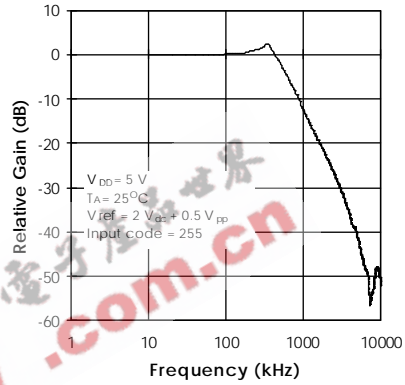
WM5620L, WM5620

Typical Performance Characteristics (Continued)

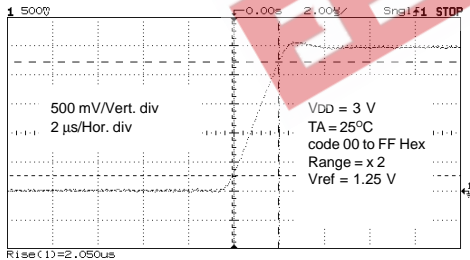
Large Signal Frequency Response



Small Signal Frequency Response

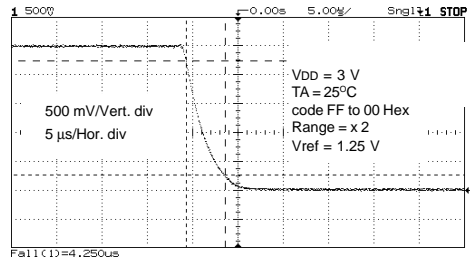


Positive Rise and Settling Time $V_{DD} = 3\text{ V}$



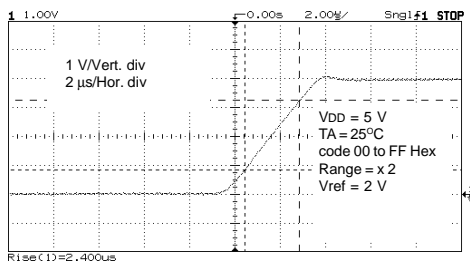
Rise time = 2.05 μs , Positive slew rate = 0.96 μs
Settling time = 4.5 μs

Negative Fall and Settling Time $V_{DD} = 3\text{ V}$



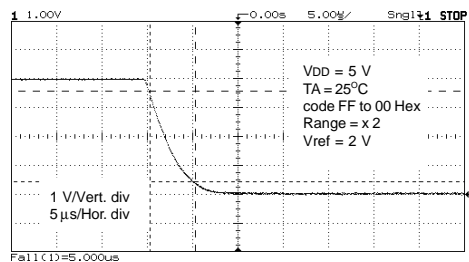
Fall time = 4.25 μs , Negative slew rate = 0.46 μs
Settling time = 8.5 μs

Positive Rise and Settling Time $V_{DD} = 5\text{ V}$



Rise time = 2.4 μs , Positive slew rate = 1.0 μs
Settling time = 5.8 μs

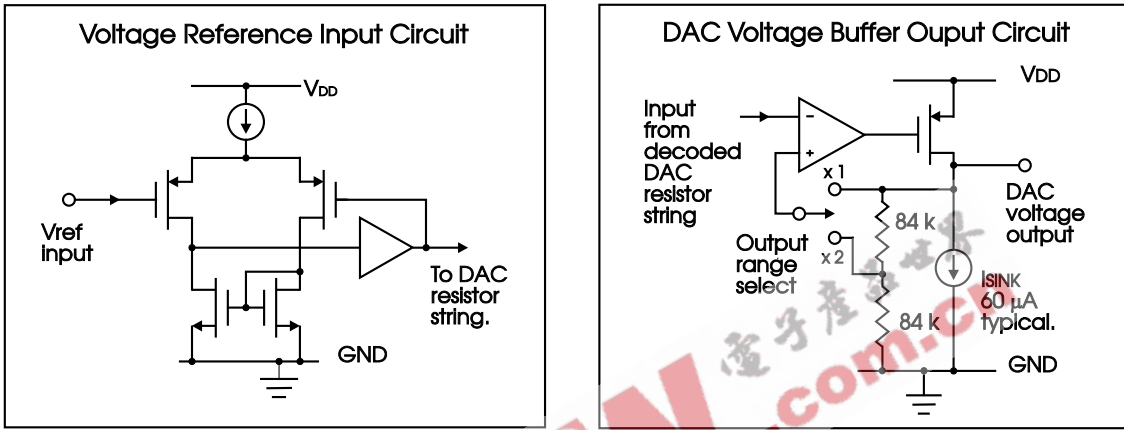
Negative Fall and Settling Time $V_{DD} = 5\text{ V}$



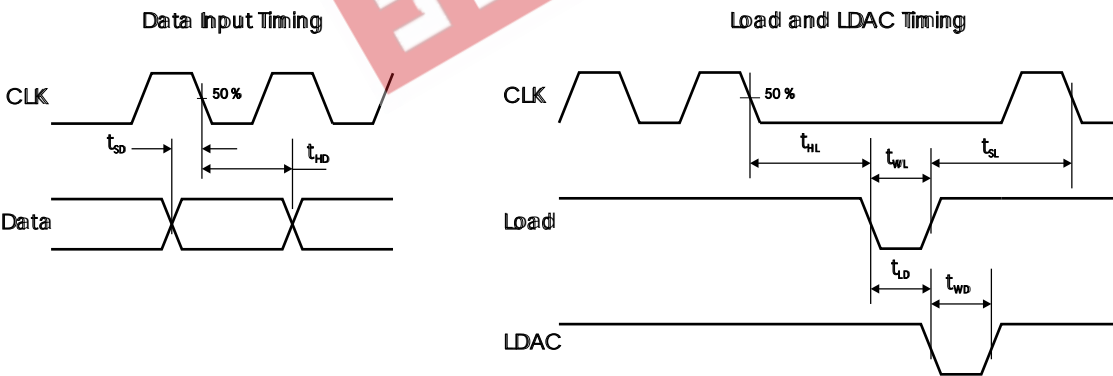
Fall time = 5.0 μs , Negative slew rate = 0.63 μs
Settling time = 9.5 μs

WM5620L, WM5620

Equivalent Input and Output Circuits



Timing Waveforms



Timing Diagrams

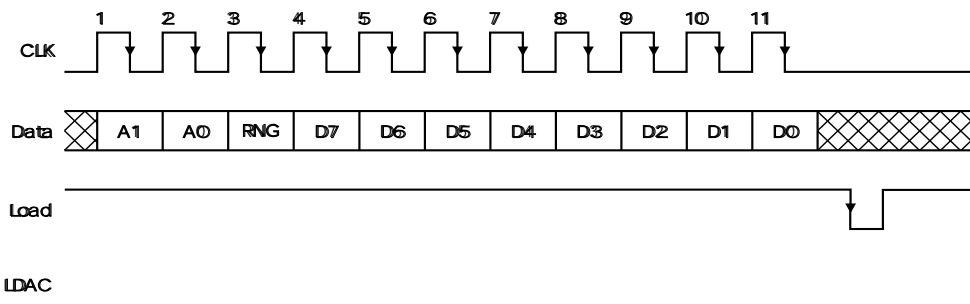


Figure 1. Load controlled update (LDAC = 0)

Timing Diagrams

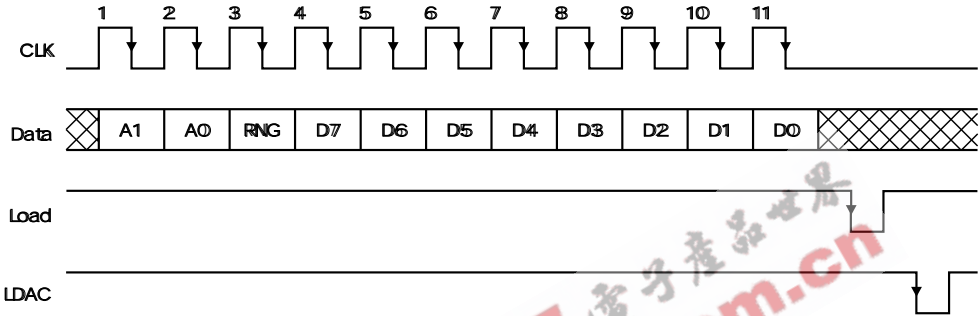


Figure 2. LDAC controlled update

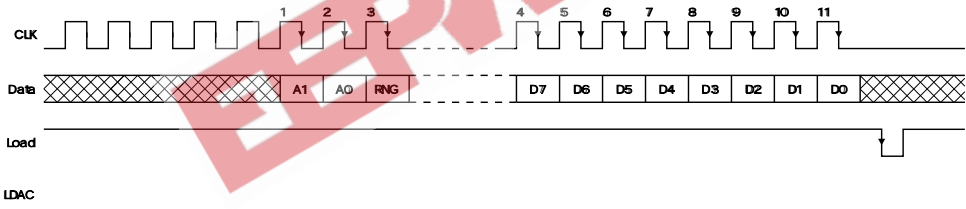


Figure 3. Load controlled update (LDAC = 0) using 8-bit serial word.

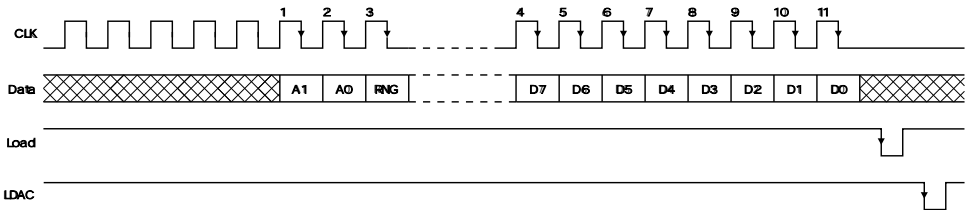


Figure 4. LDAC controlled update using 8-bit serial word.

WM5620L, WM5620

Pin Descriptions

Pin	Name	Type	Function
1	GND	Supply	Ground return and reference terminal
2	RefA	Analogue input	Reference voltage input to DACA
3	RefB	Analogue input	Reference voltage input to DACB
4	RefC	Analogue input	Reference voltage input to DACC
5	RefD	Analogue input	Reference voltage input to DACD
6	Data	Digital input	Serial interface data
7	Clk	Digital input	Serial interface clock, negative edge sensitive
8	Load	Digital input	Serial interface load
9	DACD	Analogue output	DAC D output
10	DACC	Analogue output	DAC C output
11	DACB	Analogue output	DAC B output
12	DACA	Analogue output	DAC A output
13	LDAC	Digital input	DAC update latch control
14	VDD	Supply	positive supply voltage

Functional Description

DAC operation

Each of WM5620/L's four digital to analogue converters (DACs) are implemented using a single resistor string with 256 taps corresponding to each of the input 8-bit codes. One end of a resistor string is connected to the GND pin and the other end is driven from the output of a reference input buffer. The use of a resistor string guarantees monotonicity of the DAC's output voltage. Linearity depends upon the matching of the resistor string's individual elements and the performance of the output buffer. The reference input buffers present a high impedance to reference sources.

Each DAC has a voltage output amplifier which is programmable for gains of x1 or x2 through the serial interface. The DAC output amplifiers feature rail to rail output stages, allowing outputs over the full supply voltage range to be achieved with a x2 gain setting and a VDD/2 reference voltage input. Used in this way a slight degradation in linearity will occur as the output voltage approaches VDD.

A power-on-reset activates at power up resetting the DACs inputs to code 0. Each output voltage is given by:

$$V_{out} = V_{ref} \times \text{CODE}/256 \times (1 + \text{RNG})$$

Where: RNG controls the output gains of x1 and x2
CODE is the range 0 to 255

Data interface

WM5620/L's four double buffered DAC inputs allow several ways of controlling the update of each DAC's output.

Serial data is input, MSB first, into the DATA input pin using CLK, LOAD and LDAC control inputs and comprises 2 DAC address bits, an output range (RNG) bit and 8 DAC input bits.

With the LOAD pin high data is clocked into the DATA pin on each falling edge of CLK. Any number of data bits may be clocked in, only the last 11 bits are used. When all data bits have been clocked in, a falling edge at the LOAD pin latches the data and RNG bits into the correct 9 bit input latch using the 2 bit DAC address.

If the LDAC input pin is low, the second latch at the DAC input is transparent, and the DAC input and RNG bit will be updated on the falling edge of LOAD simultaneously with the input latch, as shown in figure 1. If the LDAC input is high during serial data input, as shown in figure 2, the falling edge of the LOAD input stores the data in the addressed input latch. The falling edge of LDAC updates the second latches from the input latches and hence the DAC outputs.

WM5620L, WM5620

Functional Description (Continued)

Using these inputs individual DACs can be updated using one 11 bit serial input word and the LOAD pin. Using both LOAD and LDAC, all or selected DACs can be updated after an appropriate number of data words have been inputted. Figures 3 & 4 illustrate operation with the 8 clock pulses available from some microprocessors. If the data input is interrupted in this way the clock input must be held low during the break in clock pulses.

The RNG bit controls the DAC output range. When RNG = 0 the output is between $V_{ref}(A,B,C,D)$ and GND and when RNG = 1 the range is between $2 \times V_{ref}(A,B,C,D)$ and GND.

Serial Input Decode

A1	A0	DAC
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

D7	D6	D5	D4	D3	D2	D1	D0	Output Voltage
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{Ref} (1 + \text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{Ref} (1 + \text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{Ref} (1 + \text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{Ref} (1 + \text{RNG})$

WM5620L, WM5620

Applications Information

Linearity, offset, and gain error using single end supplies

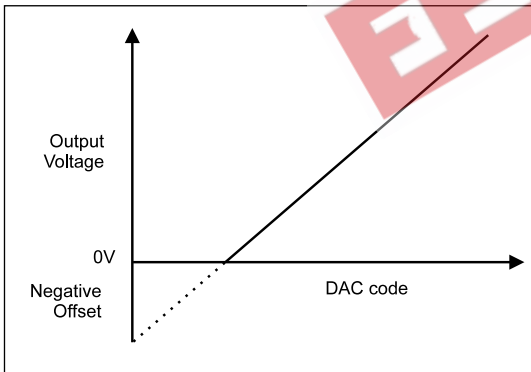
When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is GND, the output cannot drive to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at ZERO volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown below.

This negative offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive to a negative voltage.

For a DAC, linearity is measured between ZERO input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full scale code and the lowest code which produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.



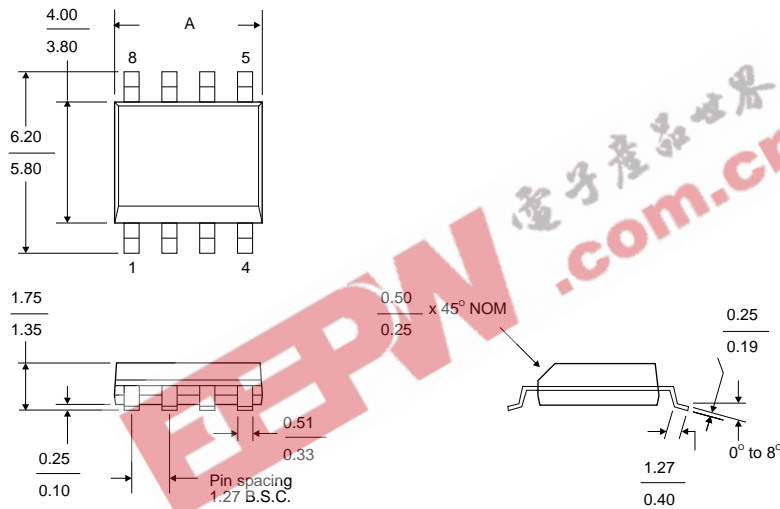
Effect of negative offset (single supply)

WM5620L, WM5620

Package Descriptions

Plastic Small-Outline Package

D - 8 pins shown



Dimension 'A' Variations

N	Min	Max
8	4.80	5.00
14	8.55	8.75
16	9.80	10.00

Notes:

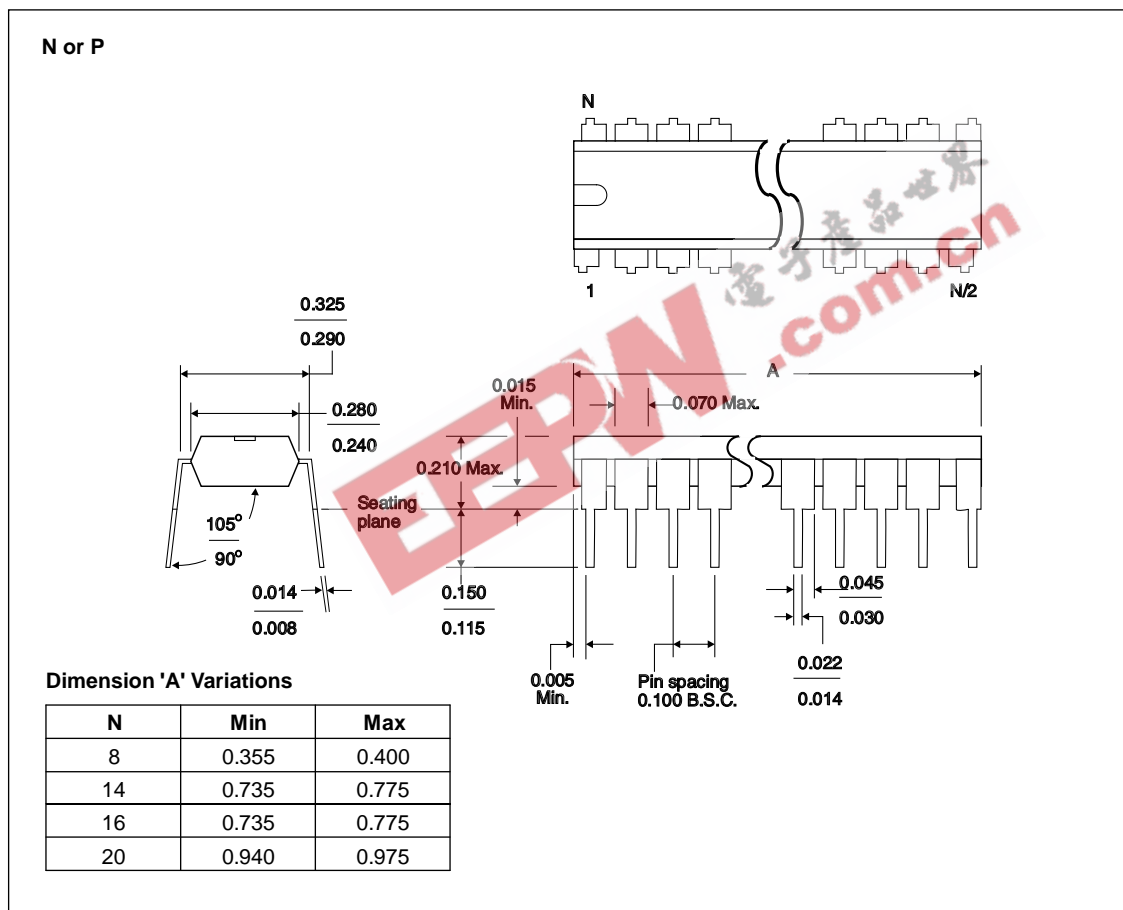
- Dimensions in millimeters.
- Complies with Jedec standard MS-012.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion.
- Dimension A, mould flash or protrusion shall not exceed 0.15mm. Body width, interlead flash or protrusions shall not exceed 0.25mm.

Rev. 1 November 96

WM5620L, WM5620

Package Descriptions

Dual-In-Line Package



Notes:

- A. Dimensions are in inches
- B. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001)
- C. N is the maximum number of terminals
- D. All end pins are partial width pins as shown, except the 14 pin package which is full width.