Winbond Electronics Corp.

8-BIT EMULATION MICROCONTROLLER

GENERAL DESCRIPTION

The W78958B is an 8-bit emulation microcontroller that supports emulation for the Winbond W78C51 family of products, including the W78C31, W78C32, W78C51, W78C52, W78C154*, W78C58, W78C438, and W78C458. It is designed to support real-time (up to 40 MHz) emulation tools, such as in-circuit emulators (ICEs).

The W78958B is packaged in a 100-pin PQFP and is available in two different types, standard and advanced. The standard type supports the functions of the W78C31, W78C32, W78C51, W78C52, W78C154*, and W78C58. The advanced type supports the functions of the W78C438 and W78C458. Both types can be operated in two modes, normal and emulation. In normal mode, the W78958B runs freely, like the W78C51 family of products. In emulation mode, which is entered by driving the ICESET pin high asynchronously, the W78958B stays in the S2 state of the next instruction. In this mode, the W78958B allows direct access (read/write) to the special function registers (SFRs), the program counter (PC), and the internal RAM. Also, it allows ICE makers to access the external program and data memory easily, thereby eliminating the need for glue logic. Moreover, it provides several signals to facilitate ICE design, including $\overline{IPME}$ (Internal Program Memory Enable), for switching between "internal" and external ROM, $\overline{ESEL}$ (Emulation address space Select), for combining the emulation program and data memory in a 128 KB SRAM, and CLKS1 (internal S1 state clock timing signal), for creating the emulation control signals. Once the ICESET pin goes low, the W78958B will release its internal clock and return to its normal operating mode.

For detailed specifications concerning the W78C31, W78C32, W78C51, W78C52, W78C154*, W78C58, W78C438, and W78C458, refer to the Functional Description below or to the Winbond product specifications.

Notes for all W78C154*:

1. W78958B will emulate W78C154 except port1.6 & port1.7 as output mode:

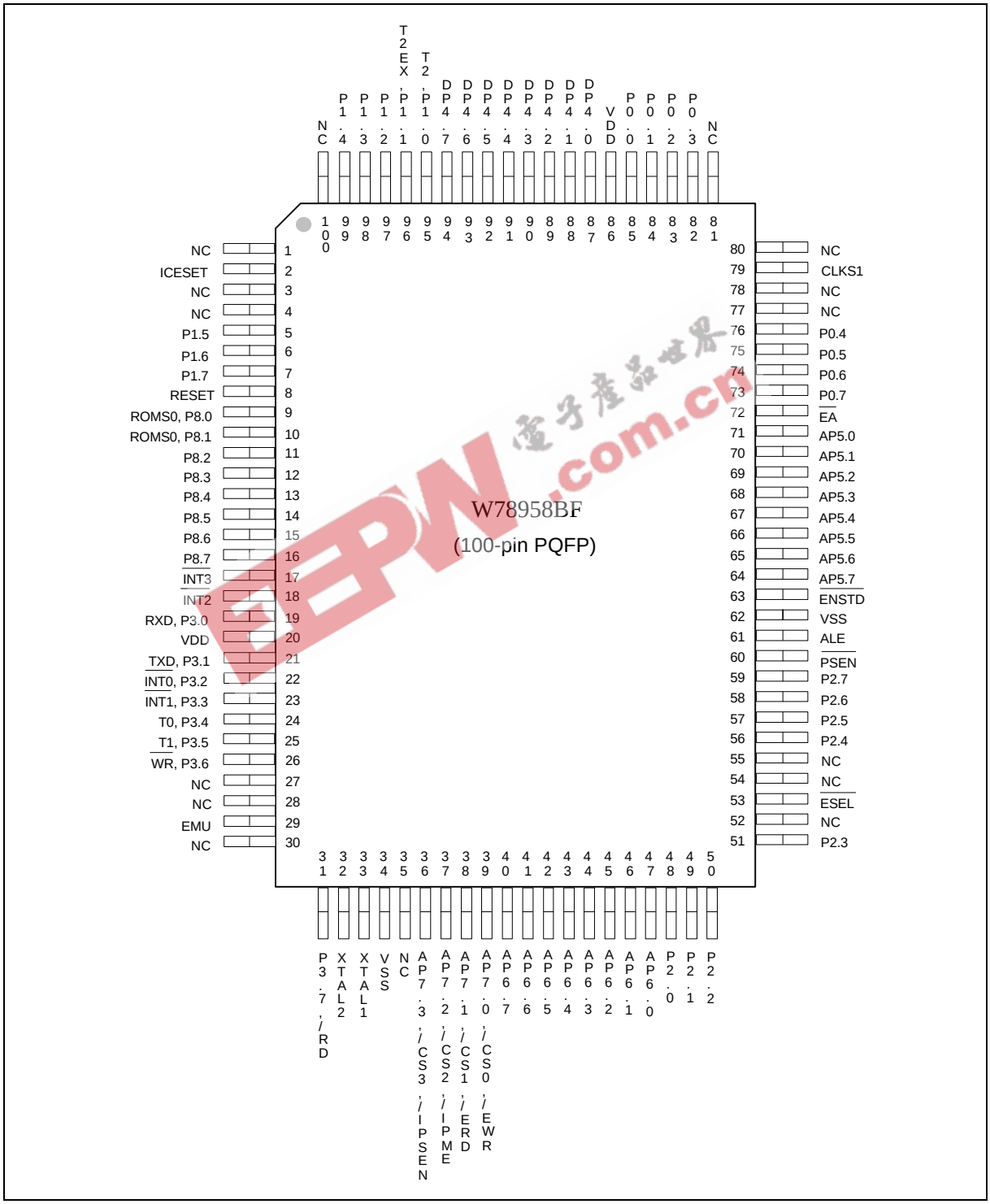
W78958B	port1.6 & port1.7	pull-ups
W78C154	port1.6 & port1.7	open drain

2. The specification of W78C154 is exclusive, therefore, the DC characteristics is not fully compatible with W78958B, however the emulation function is still the same as W78958B.

FEATURES

- 8-bit CMOS emulation microcontroller
- Real-time emulation at up to 40 MHz
- Convenient emulation chip for ICE market
- Two types: standard type and advanced type
- Standard type supports emulation for the W78C31, W78C32, W78C51, W78C52, W78C154*, and W78C58
- Advanced type supports emulation for the W78C438, and W78C458
- In emulation mode, allows direct access to SFRs/PC and internal RAM
- Allows ICE makers to access external program/data memory easily
- Supports switching signals between "internal" and external ROM
- Supports combined emulation program and data memory in a 128 KB SRAM
- Provides internal S1 state clock timing signal for easy creation of the emulation control signals
- Fully static design
- 256-byte on-chip scratchpad RAM
- 64 KB program memory address space in standard type; 1 MB extended program memory address space in advanced type
- 64 KB data memory address space in standard type; 1 MB extended data memory address space in advanced type
- Boolean processor
- Six-source, two-level interrupt capability in standard type; eight-source, two-level interrupt capability in advanced type
- Three 16-bit timer/counters
- One full duplex serial channel
- Built-in power management
- Four 8-bit bidirectional and bit-addressable I/O ports in standard type; four 8-bit bidirectional and bit- addressable I/O ports and one 8-bit bidirectional but parallel I/O port in advanced type
- Packaged in 100-pin PQFP
  - W78958BF-40

PIN CONFIGURATION



PIN DESCRIPTION

$\overline{\text{ENSTD}}$ Enable Standard Type, Input, Active Low

TYPE	MODE	DESCRIPTION
Advanced	-	Default status is pulled high by internal pull-up resistor.
Standard	-	A low on this pin enables the standard type.

Note: "-" in "Mode" column means that the function description is valid in both modes, normal and emulation.

$\overline{\text{EA}}$ External Address, Input

TYPE	MODE	DESCRIPTION
Advanced	-	Functions same as in W78C438.
Standard	-	Functions same as in W78C51, W78C52, W78C154* or W78C58.

$\overline{\text{PSEN}}$

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions same as in W78C438.
	Emulation	In high impedance state.
Standard	Normal	Pins ROMS1 and ROMS0 determine the function of $\overline{\text{PSEN}}$. For details, see Table D1 below.
	Emulation	In high impedance state.

ROMS1	ROMS0	FUNCTION of $\overline{\text{PSEN}}$, PORT 0, AND PORT 2
0	0	Same as in the W78C51 (verify 4K ROM).
0	1	Same as in the W78C52 (verify 8K ROM).
1	0	Same as in the W78C154* (verify 16K ROM).
1	1	Same as in the W78C58 (verify 32K ROM).

Table D1.

ALE

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions same as in W78C32.
	Emulation	In high impedance state.
Standard	Normal	Functions same as in W78C52.
	Emulation	In high impedance state.

RST, XTAL1, XTAL2

TYPE	MODE	DESCRIPTION
Advanced	-	Functions same as in W78C32.
Standard	-	Functions same as in W78C52.

P0.7–P0.0 Port 0, Bits 7–0

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions are the same as those in the W78C32, except that a multiplexed address/data bus is not provided during accesses to external memory.
	Emulation	Frozen in the original state.
Standard	Normal	Pins ROMS1 (P8.1) and ROMS0 (P8.0) determine functions of P0.7–P0.0. For details, see Table D1.
	Emulation	When $\overline{\text{ESEL}}$ is held at "H" level, P0.7–P0.0 are floating.

P1.7–P1.0 Port 1, Bits 7–0

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions are the same as those in the W78C32.
	Emulation	Frozen in the original state.
Standard	Normal	Functions are the same as those in the W78C52.
	Emulation	Frozen in the original state.

P2.7–P2.0 Port 2, Bits 7–0

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions are the same as those in the W78C32, except that a high-byte address bus is not provided during accesses to external memory.
	Emulation	Frozen in the original state.
Standard	Normal	Pins ROMS1 and ROMS0 determine functions of P2.7–P2.0. For details, see Table D1.
	Emulation	When $\overline{\text{ESEL}}$ is held at "H" level, the states of P2.7–P2.0 depend on the MP2 (Mask Port 2) register. At this time, if the bit content of MP2 is 0, the corresponding pin of Port 2 maintains in the original state; otherwise, the corresponding pin of Port 2 is in high impedance state.

P3.7–P3.0 Port 3, Bits 7–0

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions are the same as those in the W78C32.
	Emulation	Frozen in the original state.
Standard	Normal	Functions are the same as those in the W78C52.
	Emulation	Frozen in the original state.

DP4.7–DP4.0 Address/Data Bus, Bits 7–0

TYPE	MODE	DESCRIPTION
Advanced	Normal	DP4 provides a multiplexed low-byte address/data bus during accesses to external memory.
	Emulation	When $\overline{\text{ESEL}}$ is held at "L" level, DP4 is the data input/output of the SFR/PC and internal RAM. When $\overline{\text{ESEL}}$ is held at "H" level, DP4 is in high impedance state.
Standard	Normal	Pins ROMS1 and ROMS0 determine functions of DP4. For details, see Table D2.
	Emulation	Same as in the advanced type.

ROMS1	ROMS0	FUNCTIONS OF DP4
0	0	Provides a multiplexed low-byte address/data bus during accesses to external 4 KB EPROM.
0	1	Provides a multiplexed low-byte address/data bus during accesses to external 8 KB EPROM.
1	0	Provides a multiplexed low-byte address/data bus during accesses to external 16 KB EPROM.
1	1	Provides a multiplexed low-byte address/data bus during accesses to external 32 KB EPROM.

Table D2.

AP5.7–AP5.0 Address Bus, Bits 7–0

TYPE	MODE	DESCRIPTION
Advanced	Normal	AP5<7:0> output the <7:0> address of the external ROM multiplexed with the <7:0> address of the external data RAM.
	Emulation	When $\overline{\text{ESEL}}$ is held at "L" level, AP5 is the low-byte address input for the SFR/PC and internal RAM. When $\overline{\text{ESEL}}$ is held at "H" level, AP5 is in high impedance state.
Standard	Normal	Pins ROMS1 and ROMS0 determine functions of AP5. For details, see Table D3.
	Emulation	Same as in the advanced type.

ROMS1	ROMS0	FUNCTIONS of AP5
0	0	AP5 output the <7:0> address of the external 4K EPROM.
0	1	AP5 output the <7:0> address of the external 8K EPROM.
1	0	AP5 output the <7:0> address of the external 16K EPROM.
1	1	AP5 output the <7:0> address of the external 32K EPROM.

Table D3.

AP6.7–AP6.0 Address Bus, Bit 15–8

TYPE	MODE	DESCRIPTION
Advanced	Normal	AP6<7:0> output the <15:8> address of the external ROM multiplexed with the <15:8> address of the external data RAM. During the execution of "MOVX @Ri," AP6's output comes from the HB register, which is the page register for the high byte address.
	Emulation	When $\overline{\text{ESEL}}$ is held at "L" level, AP6<0> is the address input for the accesses to the SFR/PC and internal RAM. At this time, if AP6<0> = 0, the SFR/PC can be accessed; if AP6<0> = 1, the internal RAM can be accessed. When $\overline{\text{ESEL}}$ is held at "H" level, AP6 is in high impedance state.
Standard	Normal	Pins ROMS1 and ROMS0 determine functions of AP6. For details, see Table D4.
	Emulation	Same as in the advanced type.

ROMS1	ROMS0	FUNCTIONS OF AP6
0	0	AP6<3:0> output the <11:8> address of the external 4K EPROM.
0	1	AP6<4:0> output the <12:8> address of the external 8K EPROM.
1	0	AP6<5:0> output the <13:8> address of the external 16K EPROM.
1	1	AP6<6:0> output the <14:8> address of the external 32K EPROM.

Table D4.

AP7.3–AP7.0 Address Bus, Bit 3–0, Input/Output, Dual-purpose

TYPE	MODE	DESCRIPTION
Advanced	Normal	Bit 7 of EPMA (Extended Program Memory Address) register determines functions of AP7<3:0>. When this bit is "0" (default value), AP7 outputs the <19:16> address of the external ROM from bits <3:0> of EPMA register during the execution of "MOVC A,@A+DPTR" to read the external ROM data, the execution of "MOVX A,@DPTR" to read the external RAM data, or the execution of "MOVX @DPTR,A" to write the external RAM data. Excluding those times, AP7<3:0> output 0H. When this bit is "1," AP7<3:0> (CS3–0) are the output pins to support memory-mapped peripheral chip select, and only one of them is active low at any time. These pins are decoded by AP6<7:6>. For details, see Table D5.
	Emulation	When $\overline{\text{ESEL}}$ is held in "L" state, AP7<0> ($\overline{\text{EWR}}$) and AP7<1> ($\overline{\text{ERD}}$) are the write and read control input signals, respectively, for the accesses to the SFR/PC and internal RAM. When $\overline{\text{ESEL}}$ is held in "H" state, AP7<3:0> are in high impedance state.
Standard	Normal	AP7<2> ($\overline{\text{IPME}}$) is the "internal" program memory enable signal. It outputs "0" to indicate that the access buses are DP4, AP5 and AP6. It outputs "1" to indicate that the access buses are Port 0 and Port 2. AP7<3> ($\overline{\text{IPSEN}}$) is the "internal" program store output enable signal. It outputs "0" to enable the "internal" program memory onto the DP4 address/data bus during fetch and MOVC operations.
	Emulation	Same as in the advanced type.

AP6.7	AP6.6	DESCRIPTION
0	0	AP7.0: low; others: high
0	1	AP7.1: low; others: high
1	0	AP7.2: low; others: high
1	1	AP7.3: low; others: high

Table D5.

P8.7–P8.0 Port 8, Bits 7–0, Input/Output

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions are the same as those of Port 1 in the W78C31, except that they are mapped by the P8 register and not bit-addressable. The P8 register is not a standard register in the W78C32. Its address is at 0A6H.
	Emulation	Frozen in the original state.
Standard	Normal	P8.1 (ROMS1, standard type ROM size Select 1) and P8.0 (ROMS0) are the input pins that determine which of four different ROM sizes is being used: 4K, 8K, 16K, or 32K bytes. For details, see Table D1–D4.
	Emulation	Frozen in the original state.

$\overline{INT2}$ and $\overline{INT3}$ External Interrupt 2 and 3, Input

TYPE	MODE	DESCRIPTION
Advanced	Normal	Functions are similar to those of external interrupt 0 and 1 in the W78C31, except that the functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. For details, see Table D6. The XICON register is bit-addressable but is not a standard register in the W78C32. Its address is at 0C0H. The interrupt vector addresses and the priority polling sequence within the same level are shown in Table D7.
	Emulation	Frozen in the original state.
Standard	-	Not supported.

BIT	ADDR.	NAME	FUNCTION
7	0C7H	PX3	High/low priority level for $\overline{INT\ 3}$ is specified when this bit is set/cleared by software.
6	0C6H	EX3	Enable/disable interrupt from $\overline{INT3}$ when this bit is set/cleared by software.
5	0C5H	IE3	If IT3 is "1," IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
4	0C4H	IT3	$\overline{INT3}$ is falling-edge/low-level triggered when this bit is set/cleared by software.
3	0C3H	PX2	High/low priority level for $\overline{INT\ 2}$ is specified when this bit is set/cleared by software.
2	0C2H	EX2	Enable/disable interrupt from $\overline{INT\ 2}$ when this bit is set/cleared by software.
1	0C1H	IE2	If IT2 is "1," IE2 is set/cleared automatically by hardware when interrupt is de0tected/serviced.
0	0C0H	IT2	$\overline{INT\ 2}$ is falling-edge/low-level triggered when this bit is set/cleared by software.

Table D6. Functions of XICON Register.

INTERRUPT SOURCE	VECTOR ADDRESS	PRIORITY SEQUENCE WITHIN LEVEL
External Interrupt 0	03H	0 (Highest)
Timer/Counter 0	0BH	1
External Interrupt 1	13H	2
Timer/Counter 1	1BH	3
Serial Port	23H	4
Timer/Counter 2	2BH	5
External Interrupt 2	33H	6
External Interrupt 3	3BH	7 (Lowest)

Table D7.

$\overline{\text{ESEL}}$ Emulation Address Space Select, Input/Output, Dual-purpose

TYPE	MODE	DESCRIPTION
Advanced	Normal	While the W78958B is accessing program memory, $\overline{\text{ESEL}}$ outputs "0." While the W78958B is accessing data memory, the $\overline{\text{ESEL}}$ outputs "1."
	Emulation	Default status is pulled low by internal pull-high resistor. $\overline{\text{ESEL}}$ is used to select two emulation address spaces. When $\overline{\text{ESEL}}$ is held in "L" state, the SFR/PC and internal RAM can be accessed, and AP7<0>($\overline{\text{EWR}}$) and AP7<1>($\overline{\text{ERD}}$) are the active low write and read control input signals, respectively. When $\overline{\text{ESEL}}$ is held in "H" state, the external ROM and RAM can be accessed (P3.6 and P3.7 are weakly pulled high by internal pull-high resistors).
Standard	Normal	Same as in the advanced type.
	Emulation	Default status is pulled low by internal pull-high resistor. $\overline{\text{ESEL}}$ is used to select two emulation address spaces. When $\overline{\text{ESEL}}$ is held in "L" state, the SFR/PC and internal RAM can be accessed, and AP7<0>($\overline{\text{EWR}}$) and AP7<1>($\overline{\text{ERD}}$) are the active low write and read control input signals, respectively. When $\overline{\text{ESEL}}$ is held in "H" state, the external ROM/RAM can be accessed (P3.6/P3.7 are weakly pulled high by internal pull-high resistors), P0.7–P0.0 are floating, and P2.7–P2.0 are in high impedance state optionally dependent on the content of register MP2.

ICESET Emulation Mode Enable, Input, Active High

This pin, which is used to facilitate ICE applications, is default low with an internal pull-low resistor. When ICESET is set active, the W78958B will enter the emulation mode. In this mode, the W78958B's internal clock and states are frozen, but the oscillator continues to run. The contents of the SFRs, PC, the 256-byte internal RAM, and the external program/data memory can then be accessed easily by ICE makers to eliminate board-level glue logic. As soon as the ICESET pin goes low again, the W78958B will release the internal clock and return to its original operating mode.

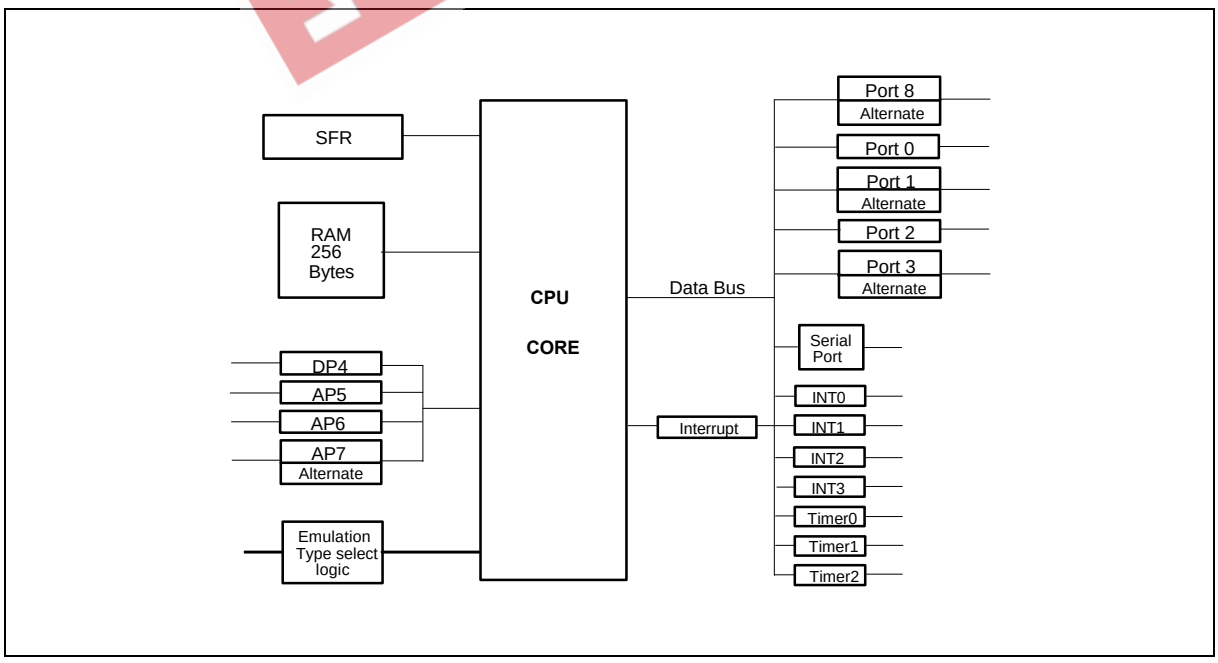
EMU Emulation Mode Active Indicator, Output, Active High

When ICESET is set to high and synchronized with the internal clock, EMU will go high at the end of the S1 state of the next instruction. This pin indicates that the W78958B has entered the emulation mode after ICESET acknowledgment. When ICESET is set to low, the W78958B clears the content of IR (00H is the opcode of instruction NOP), and then leave the emulation mode. At this time, the W78958B runs a NOP instruction to prevent improper code from being executed, because the content of PC may have been changed. After the W78958B leaves the emulation mode–i.e., the internal clock and states start to run–it takes four states to fetch the second (ignored) byte of NOP. EMU will go low until the complete NOP instruction has been finished–that is, it will go low at the end of the S4 state. EMU goes low four states after the device exits the emulation mode.

CLKS1 Machine Cycle Clock output pin

CLKS1 outputs the internal S1 state cycle clock.

BLOCK DIAGRAM



Note: AP7, Port 8, INT2 and INT3 are valid only in advanced type.

FUNCTIONAL DESCRIPTION

The W78958B is available in two types, an advanced type and a standard type, which are intended for use with different end products. The default product type is the advanced type. Both the advanced type and the standard type are also available with an emulation function. To configure the W78958B to operate as the advanced type or standard type and to enter the emulation mode, adjust the input pin settings as shown in the table below. (Note that a transition between the advanced type and standard type is not permitted after power-on.)

		Advanced → Emulation		Standard → Emulation		Notes
$\overline{\text{ENSTD}}$	I	High		Low		1
$\overline{\text{EA}}$	I	Low		High/Low		
ICESET	I	Low	High	Low	High	2
EMU	O	Low	High	Low	High	

Notes:

1. This pin is pulled high internally.
2. This pin is pulled low internally.

The type transition diagram for the advanced and standard types is shown below:

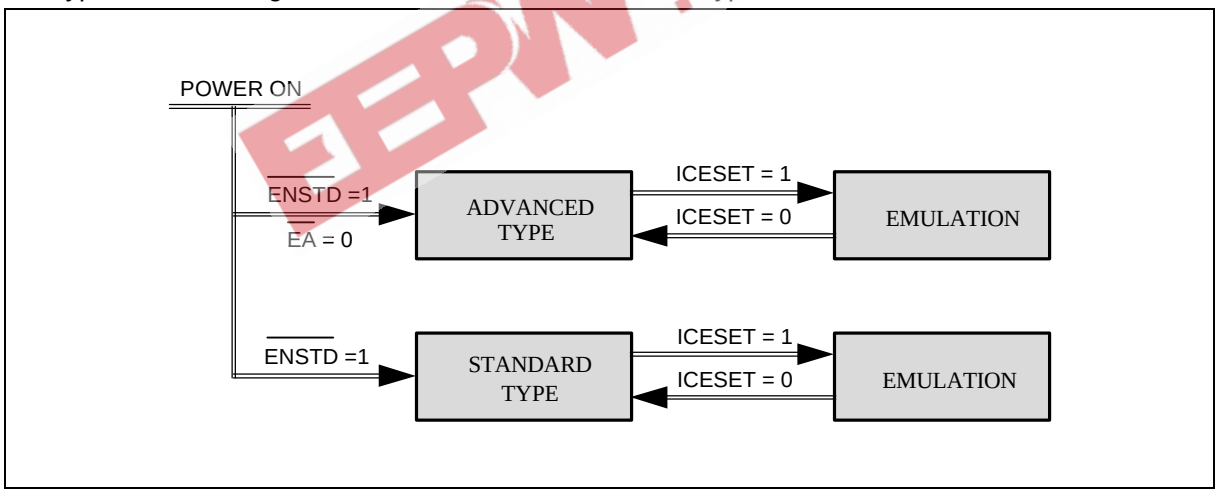


Figure E. 1

Note that a transition between the advanced type and standard type is not permitted after power-on.

Advanced Type, Normal Mode

At power-on, if $\overline{\text{ENSTD}}$ is set to high or left floating and $\overline{\text{EA}}$ is set to low, then the W78958B will operate as the advanced type. The advanced type provides four general-purpose I/O ports for W78C32 applications; the address and data bus are separated from Port 0 and Port 2 so that these ports can be used as general-purpose I/O ports. In this type, DP4 is the data bus for external program and data memory, AP5<7:0> are the low byte address, AP6<7:0> are the high byte address, $\overline{\text{PSEN}}$ enables the external program memory to DP4, and P3.6 ($\overline{\text{WR}}$) and P3.7($\overline{\text{RD}}$) are the write and read control signals for the external data memory, respectively. The external latch for multiplexing the low

byte address is no longer needed in this type. The advanced type supports 64 KB of external program memory and 64 KB of external data memory, just as a W78C32 does.

The programming of the advanced type is fully compatible with that of the W78C32 except that the external data RAM is accessed by a "MOVX @Ri" instruction. To support address paging, there is an additional 8-bit SFR "HB" (high byte), which is a nonstandard register, at address 0A1H. During the execution of "MOVX @Ri," the contents of HB are output to AP6. The page address is modified by loading the HB register with a new value before execution of the "MOVX @Ri" instruction. To read/write the HB register, one can use the "MOV direct" instruction or "read-modify-write" instructions. The HB register does not support bit-addressable instructions.

The advanced type provides four pins, AP7.3–AP7.0 (CS3–CS0), to support either 1 MB program/data memory space or memory-mapped chip select logic. Bit 7 of EPMA (Extended Program Memory Address) register determines the functions of these pins. When this bit is "0" (default value), AP7<3:0> support external program and data memory addresses up to 1 MB for applications that require additional external memory to store large amounts of data. During the execution of "MOVC A,@A+DPTR" to read the external ROM data, the execution of "MOVX @DPTR,A" to write the external RAM data, or the execution of "MOVX A,@DPTR" to read the external RAM data, AP7<3:0> output address <19:16> from bits <3:0> of the EPMA (Extended Program Memory Address) register. Excluding that time, AP7<3:0> always output 0H to ensure the instruction fetch is within the 64K program memory address. Different banks can be selected by modifying the content of the EPMA register before the execution of these instructions.

When EPMA.7 is "1," AP7<3:0> are output pins that support the memory-mapped peripheral chip select logic, which eliminates the need for glue logic. These pins are decoded by AP6<7:6>. Only one of the pins is active low at any one time. That is, they are active individually with 16 K address resolution. For example, CS0 is active low for the address range from 0000H to 3FFFH, CS1 is active low for 4000H to 7FFFH, and so forth.

The EPMA register is a nonstandard 8-bit SFR at address 0A2H in the W78C32. To read/write the EPMA register, one can use the "MOV direct" instruction or "read-modify-write" instructions. Bits <6:4> of the EPMA register are reserved bits, and their output values are 111B if they are read. The content of EPMA is 70H after RESET. The EPMA register does not support bit-addressable instructions.

The advanced type provides one parallel I/O port, Port 8. Its function is the same as that of Port 1 in the W78C31, except that the port is mapped by the P8 register and is not bit-addressable. The P8 register is not a standard register in the W78C32. Its address is at 0A6H. To read/write the P8 register, one can use the "MOV direct" instruction or "read-modify-write" instructions.

The advanced type provides two additional external interrupts, $\overline{\text{INT 2}}$ and $\overline{\text{INT 3}}$, whose functions are similar to those of external interrupt 0 and 1 in the W78C31. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. For details, see Table D6. The XICON register is bit-addressable but is not a standard register in the W78C32. Its address is at 0C0H. To set/clear the bits of the XICON register, one can use the "SETB (or CLR) bit" instruction. For example, "SETB 0C2H" sets bit EX2 of XICON. The interrupt vector addresses and the priority polling sequence within the same level are shown in Table D7.

For a description of the emulation functions of the advanced type, refer to the section below on the emulation functions.

Standard Type, Normal Mode

If $\overline{\text{ENSTD}}$ is set to low at power-on, then the W78958B will operate as the standard type. In this type, pins ROMS1 and ROMS0 are input pins that are used to select one of four different ROM sizes: 4, 8, 16, or 32 K bytes. When $\overline{\text{EA}}$ is set to high, an internal program code is fetched from the external 4, 8, 16, or 32 KB EPROM, depending on the state of ROMS1 and ROMS0. The interface pins needed are DP4<7:0>, as the data bus, and AP5<7:0> and AP6<3:0>, AP6<4:0>, AP6<5:0> or AP6<6:0>, as the address bus, again depending on the state of ROMS1 and ROMS0. When $\overline{\text{EA}}$ is set to low, the device is compatible with W78C32 operations.

For example, when pins ROMS1 and ROMS0 are held in "L" and "H" states, respectively, the functions of the standard type are fully compatible with those of the W78C52, except that the internal 8 KB ROM is replaced by an external EPROM. To reduce the size of the EPROM, one can use the W78T064, a 20-pin, 300-mil 8 KB EPROM with internal address latch. If the W78T064 is used as the EPROM, DP4<7:0> should be used as the low-byte address and data bus. And the AP7<3> ($\overline{\text{IPSEN}}$) enables the "internal" (lower-order 8 KB, for this example) program memory output onto the DP4 address/data bus during fetch and MOVC operations. For detailed specifications concerning the W78T064, refer to the W78T064 product specifications.

The $\overline{\text{IPME}}$ pin indicates the access buses for the program memory. During accesses to the "internal" program memory, it outputs "0" to indicate that the access buses are DP4, AP5, and AP6. During accesses to the "external" program memory, it outputs "1" to indicate that the access buses are Port 0 and Port 2.

For a description of the emulation functions of the standard type, refer to the next section.

Emulation Functions (Both Types)

The W78958B supports emulation functions for the standard type (emulation of the W78C31, W78C32, W78C51, W78C52, W78C154*, and W78C58) and the advanced type (emulation of the W78C438, and W78C458).

When the device is operating in the normal mode, pins $\overline{\text{ESEL}}$, CLKS1, AP7<2> ($\overline{\text{IPME}}$), ROMS1 and ROMS0 provide special functions to facilitate ICE design. When the emulation program and data memory are combined in a single chip, $\overline{\text{ESEL}}$ is used to separate the two memory spaces. $\overline{\text{ESEL}}$ outputs "0" to indicate that the W78958B is accessing program memory and "1" to indicate that the W78958B is accessing data memory. CLKS1 outputs the internal S1 state cycle clock, which can be used as a base for the necessary timing signals. When W78958B is operating as the standard type and emulates a model that includes an internal ROM, AP7<2> ($\overline{\text{IPME}}$) is used to select the "internal" or external program memory. When the W78958B fetches the "internal" program, $\overline{\text{IPME}}$ outputs "0" to indicate that the access buses are DP4, AP5, and AP6. When the W78958B fetches the external program, $\overline{\text{IPME}}$ outputs "1" to indicate that the access buses are Port 0 and Port 2. Finally, in the standard type, $\overline{\text{PSEN}}$, Port 0, Port 2, DP4, AP5, and AP6 are used to configure the device to emulate products with different ROM code sizes, such as the W78C51 (4 KB ROM), W78C52 (8 KB ROM), W78C154* (16 KB ROM), and W78C58 (32 KB ROM). Pins ROMS1 and ROMS0 are used to select the ROM size. Concerning the functions of $\overline{\text{PSEN}}$, Port 0, Port 2, DP4, AP5, and AP6, see tables D1 to D4.

In an ICE system, when a breakpoint condition is met or the user forces the CPU to stop running, the W78958B's ICESET pin is forced high by the system operation. When ICESET active is sampled at the end of the S1 state, the EMU pin is set to high to indicate that the W78958B has entered the emulation mode. Once this occurs, the W78958B will remain in the S2 state of the instruction

currently specified by the breakpoint. In this mode, all internal clocks are stopped and the primary I/O pins of the W78958B are frozen in their previous states; only the oscillator continues to run. Also, the contents of all the SFRs/PC and the scratchpad RAM remain as they were at the end of the last instruction.

When the device is in the emulation mode, the internal SFR/PC/RAM can be accessed directly, and the external ROM/RAM can also be accessed easily. The $\overline{\text{ESEL}}$ input is used to separate the two access spaces (the internal SFR/PC/RAM and the external ROM/RAM). To access the internal SFR/PC/RAM, hold $\overline{\text{ESEL}}$ at "L" level. DP4 then serves as a bidirectional data bus, AP5 and AP6<0> as the address input bus, and AP7<0>/AP7<1> as the write/read control input signals, When AP6<0> is "0," the SFR/PC can be accessed; when AP6<0> is "1," the internal RAM can be accessed. The SFRs' addresses are the same as those specified in the W78C32. The HB (0A1H), EPMA (0A2H), P8 (0A6H), and XICON (0C0H) registers can be accessed only in the advanced type. The addresses of the PC's low-byte (PCL) and high-byte (PCH) are 0A3H and 0A4H, respectively, which are not the standard SFRs in the W78C32 and cannot be accessed in normal mode.

When $\overline{\text{ESEL}}$ is held at "H" level, DP4, AP5, AP6, and AP7 are in high impedance state, but the functions of Port 0 and Port 2 depend on the type of W78958B. In the advanced type, Port 0 and Port 2 are in the original state. In the standard type, Port 0 is floating, and the individual bits of Port 2 are either in the original state or in high impedance state, depending on the contents of the MP2 (Mask Port 2) register. If the content of a particular bit in MP2 is "0," the corresponding pin of Port 2 is in the original state; if the content of a particular bit in MP2 is "1," the corresponding pin of Port 2 is in the high impedance state. For example, when 16 KB external program/data memory is needed and the remaining two pins, P26 and P27, are used as the I/O, MP2 must be filled with 3FH before the external program/data memory can be accessed. The MP2 register is a nonstandard 8-bit SFR at address 0A5H in the W78C32, and its default value is 0FFH. It can be accessed only in the emulation mode of the standard type.

After the W78958B enters the emulation mode, the code located on the breakpoint address is filled into the IR register but is not decoded, and the content of PC is incremented by one. The content of PC may be modified during the emulation mode, but the code within IR will not be modified accordingly. For this reason, the W78958B clears the content of IR (00H is the opcode of instruction NOP) before leaving the emulation mode. The emulation mode can be released by resetting the ICESET pin to low. After the signal is acknowledged, the W78958B clears the content of IR, and then the W78958B will resume operation from the S2 state. At this time, the W78958B runs an NOP instruction to prevent improper code from being executed, because the content of PC may have been changed. After the W78958B leaves the emulation mode, i.e., the internal clock and states start to run, it takes four states to fetch the second (ignored) byte of NOP. EMU will go low until the complete NOP instruction has been finished; that is, it will go low at the end of the S4 state. EMU goes low four states after the device exits the emulation mode. For more information, see the Timing Diagram for the emulation cycle.

The content of PC must be handled carefully. For example, if the W78958B enters emulation mode after the content of PC has reached a user-defined breakpoint address, say 100H, the content of PC will be incremented by 1, to 101H. To restart the program from the same address (100H) after the device exits the emulation mode, 1 must be subtracted from the content of PC–that is, 100H must be filled into PC before the device exits emulation mode. To restart the program from a new program address (for example, 200H) after leaving the emulation mode, fill the new address value (200H) into PC. If one breakpoint is set in the current PC, this breakpoint will be reached again after leaving the emulation mode, however, so this breakpoint must be avoided carefully.

It is important that the W78958B not enter emulation mode after entering power-down mode, even if the ICESET pin goes high. If the breakpoint address is the instruction that immediately follows activation of the idle mode, the EMU pin will go high after the execution of the interrupt service routine while the W78958B is being awakened from interrupt.

New Special Function Registers

NAME	ADDR	OBJECT	VALUE AFTER RESET	TIME TO ACCESS	NOTES
HB	A1	During the execution of "MOVX @Ri," the content of HB is output to AP6.	00H	Both modes for advanced type	1
EPMA	A2	EPMA.7 determines functions of AP7. EPMA.3–EPMA.0 determine values of AP7<3:0> when EPMA.7 is "0."	70H	Both modes for advanced type	1
PCL	A3	Accessed by ICE makers.	00H	Emu. mode for both types	
PCH	A4	Accessed by ICE makers.	00H	Emu. mode for both types	
MP2	A5	The bits of MP2 determine functions of P2<7:0> during the emulation mode for standard type.	0FFH (for POR only)	Emu. mode for Ver. type	2
P8	A6	The content of P8 is output to port 8.	0FFH	Both modes for advanced type	1
XICON	C0	The bits of XICON determine/show the functions/status of $\overline{\text{INT}}$ 2–3.	00H	Both modes for advanced type	1

Notes:

1. The instructions used to access these nonstandard registers may cause assembling errors with respect to the 2500 A. D. assembler, but these errors can be ignored by adding directive ".RAMCHK OFF" ahead these instructions.
2. In standard type, the contents of MP2 must be set up correctly before the external ROM/RAM is accessed.

Power Reduction Function

The W78958B supports power reduction but is not guaranteed to duplicate the current specifications of the W78C32.

The status of the external pins during the idle and power-down modes for the W78958B is shown in the following tables.

Advanced Type:

MODE \ PIN	ALE	$\overline{\text{PSEN}}$	PT0–PT3, P8	DP4	AP5 AP6	AP7
Idle	1	1	Port Data	Floating	Address	@1
Power-down	0	0	Port Data	Floating	Address	@1

Note: Either 0 or decoded value by AP6<7:6>, depending the value of EPMA.7.

Standard Type:

MODE		ALE	PSEN	PT0–PT3	DP4	AP5 AP6
Idle	Internal	1	1	Same as W78C52	Floating	Address
	External	1	1	Same as W78C52	Floating	Address
Power-down	Internal	0	0	Same as W78C52	Floating	Address
	External	0	0	Same as W78C52	Floating	Address

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	VDD–V	-0.3	+7.0	
Input Voltage	V	VSS	VDD	V
Operating Temperature	OPR	0		°C
	TSTG		+150	°

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

(VDD VSS ±10%, T = 25° OSC = 40 MHz, unless otherwise specified.)

	SYM.	TEST CONDITIONS				UNIT
			MIN.		MAX.	
Oper. Voltage	DD		4.5		5.5	V
	IDD		-	-		mA
Idle Current	IDLE	Program Idle Mode		-	10	
Pwdn Current	I	Program Power-down Mode	-		50	µ
Input Leakage Current	LK1	$\overline{\text{ENSTD}}$, $\overline{\text{INT 2}}$ $\overline{\text{INT 3}}$ Internal Pull-high Notes 1, 2		-	+10	A
Input Leakage	ILK2	Internal Pull-low Notes 1,	-10	-		µA
Current	I	$\overline{\text{EA}}$, Port 0, DP4 Note 1		-	+10	A
Input Leakage	ILK4	Note 1	-50		+10	µ
O/P Low Voltage	V	IOL1 = 2 mA (Port 1, 2, 3, 8)	-	-	0.45	V
O/P High Voltage	VOH1	IOH1 = -100 µA (Port 1, 2, 3, 8)	2.4	-	-	V
O/P Low Voltage	VOL2	IOL2 = 4 mA Note 3 (ALE, $\overline{\text{PSEN}}$	-	-		V

DC Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			MIN.	TYP.	MAX.	
O/P High Voltage	V_{OH2}	I_{OH2} = -400 µA Note 3 (ALE, $\overline{PSEN}$, P0, DP4, EMU)	2.4	-	-	V
O/P Low Voltage	V_{OL3}	I_{OL2} = 2 mA ($\overline{AP5}$, $\overline{AP6}$, $\overline{AP7}$, $\overline{ESEL}$, CLKS1)	-	-	0.45	V
O/P High Voltage	V_{OH3}	I_{OH2} = -100 µA ($\overline{AP5}$, $\overline{AP6}$, $\overline{AP7}$, $\overline{ESEL}$, CLKS1)	2.4	-	-	V
Input Voltage	V_{ILT}	V_{DD} = 5V ±10%	0	-	0.8	V
Input Voltage	V_{IHT}	V_{DD} = 5V ±10%	2.4	-	Note 4	V
Input Voltage	V_{ILC}	V_{DD} = 5V ±10%, XTAL1 Note 5	0	-	0.8	V
Input Voltage	V_{IHC}	V_{DD} = 5V ±10%, XTAL1 Note 5	3.5	-	Note 4	V
Input Voltage	V_{ILR}	V_{DD} = 5V ±10%, RESET Note 5	0	-	0.8	V
Input Voltage	V_{IHR}	V_{DD} = 5V ±10%, RESET Note 5	2.4	-	Note 4	V

Notes:

1. 0 < V_{IN} < V_{DD}, for $\overline{ENSTD}$, $\overline{INT2}$, $\overline{INT3}$, RESET, $\overline{EA}$, ICESET, Port 0, DP4, P1, P2, P3, and P8 inputs in leakage.
2. Using an internal pull low/high resistor (approx. 30K).
3. ALE, $\overline{PSEN}$, P0 and DP4 in external program or data access mode.
4. The maximum input voltage is V_{DD} +0.2V.
5. XTAL1 is a CMOS input and RESET is a Schmitt trigger input.

AC CHARACTERISTICS

AC specifications are a function of the particular process used to manufacture the product, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The figures below represent the performance expected from a 0.8 micron CMOS process.
Refer to the W78C52 data sheet for further AC specifications.

Clock Input Waveform

PARAMETR	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	10	-	-	nS	3
Clock Low	T_{CL}	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle in Advanced Type

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{PSEN}$ Low	TAPL	2 TCP	-	-	nS
$\overline{PSEN}$ Low to Data Valid	TPDV	-	-	2 TCP	nS

Data Memory Read/Write Cycle in Advanced Type

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{RD}$ Low	TARL	4 TCP	-	4 TCP+Δ	nS
$\overline{RD}$ Low to Data Valid	TRDV	-	-	4 TCP	nS
Data Hold After $\overline{RD}$ High	TRDQ	0	-	2 TCP	nS
$\overline{RD}$ Pulse Width	TRS	6 TCP-Δ	6 TCP	-	nS
Address Valid to $\overline{WR}$ Low	TAWL	4 TCP	-	4 TCP+Δ	nS
Data Valid to $\overline{WR}$ Low	TDWL	1 TCP	-	-	nS
Data Hold After $\overline{WR}$ High	TWDQ	1 TCP	-	-	nS
$\overline{WR}$ Pulse Width	TWS	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Program Fetch Cycle in Standard Type

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{PSEN}$ Low	TAPL	2 TCP	-	-	nS
Address Valid to Data Valid	TADV	-	-	4 TCP	nS

Emulation Mode Cycle (Internal SFR/PC/RAM Access Only)

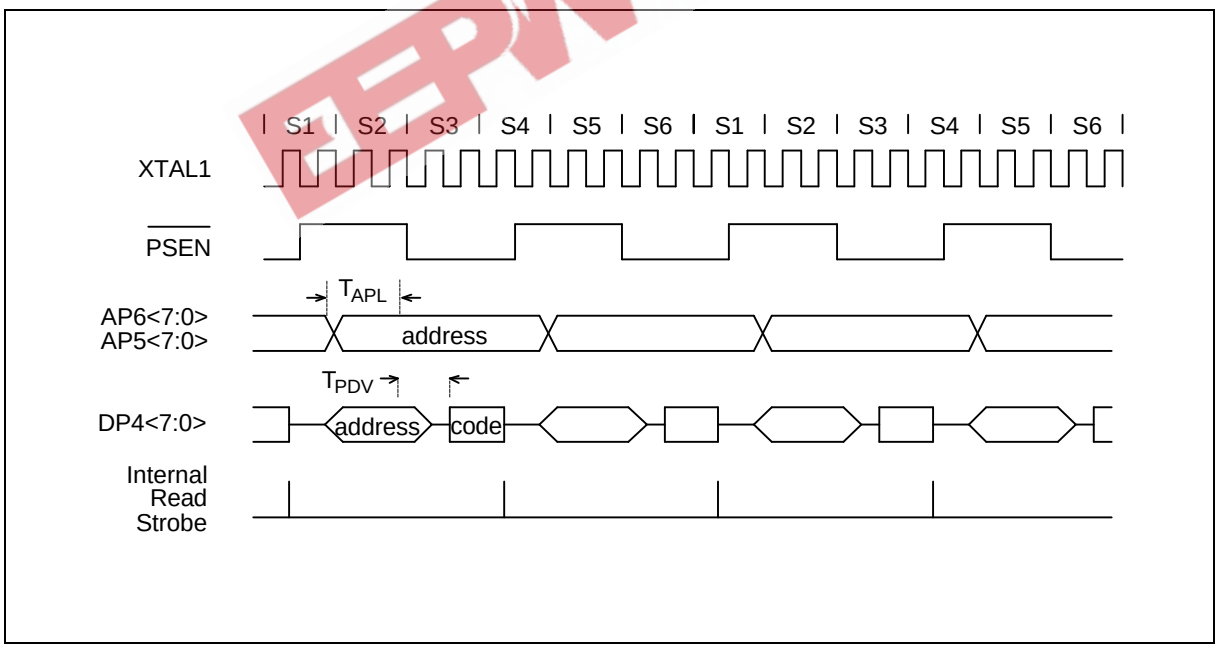
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to ICESET Set	TAIS	-	-	6 TCP-50	nS
Address Valid to EMU High	TAUH	-	6 TCP	-	nS
ICESET Low to Emulation Mode Re-exit	TIER	-	-	3 TCP	nS
ICESET Low to EMU Low	TIUL	-	-	11 TCP	nS
Emu. Address Valid to AP7<1> Low	TEARL	25	-	-	nS
AP7<1> Low to Data Valid	TERDV	-	25	-	nS

Emulation Mode Cycle (Internal SFR/PC/RAM Access Only), continued

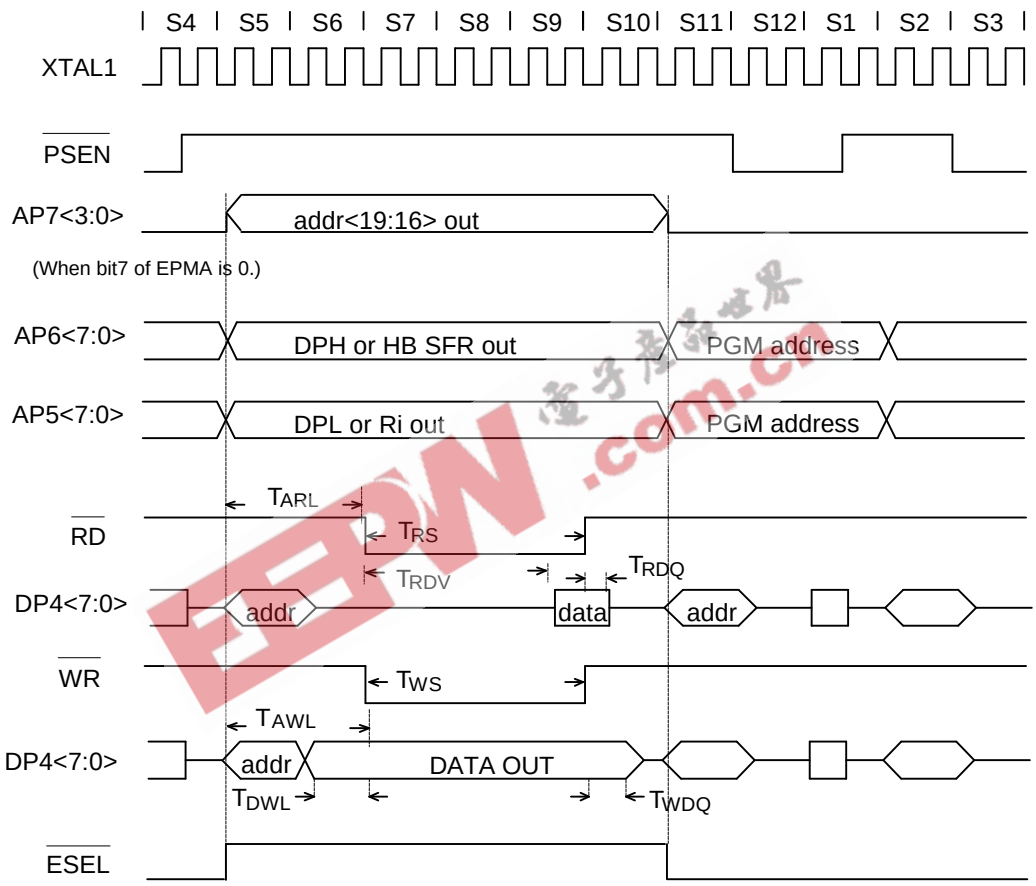
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Emu. Addr. Hold After AP7<1> High	T_{ERAQ}	25	-	-	nS
Data Hold After AP7<1> High	T_{ERDQ}	-	0	-	nS
AP7<1> Pulse Width	T_{ERS}	75	-	-	nS
Emu. Address Valid to AP7<0> Low	T_{EAWL}	25	-	-	nS
Emu. Data Valid to AP7<0> Low	T_{EDWL}	25	-	-	nS
Emu. Addr. Hold After AP7<0> High	T_{EWAQ}	25	-	-	nS
Emu. Data Hold After AP7<0> High	T_{EWDQ}	25	-	-	nS
AP7<0> Pulse Width	T_{EWS}	75	-	-	nS

TIMING WAVEFORMS

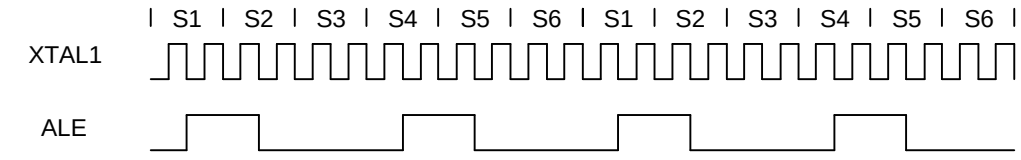
Program Fetch Cycle in Advanced Type



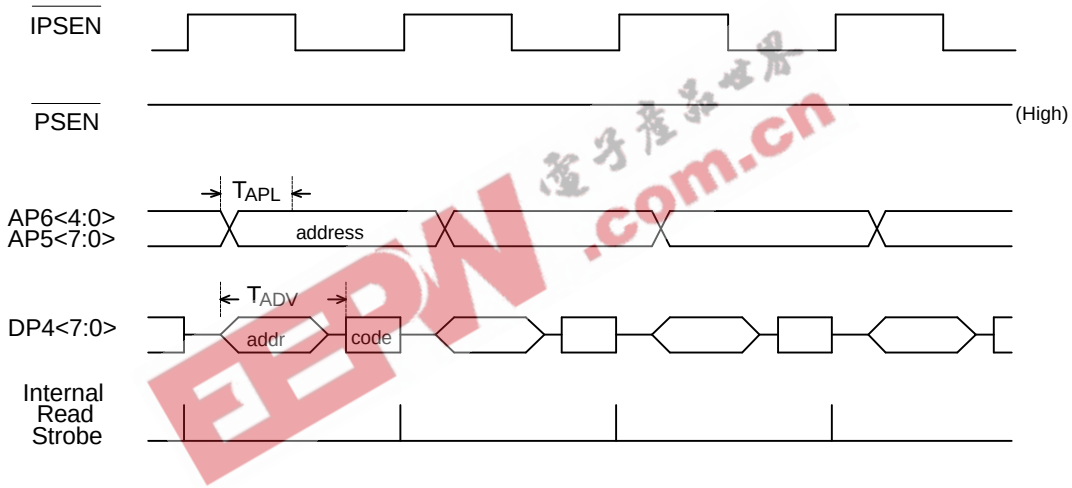
Data Memory Read/Write Cycle in Advanced Type



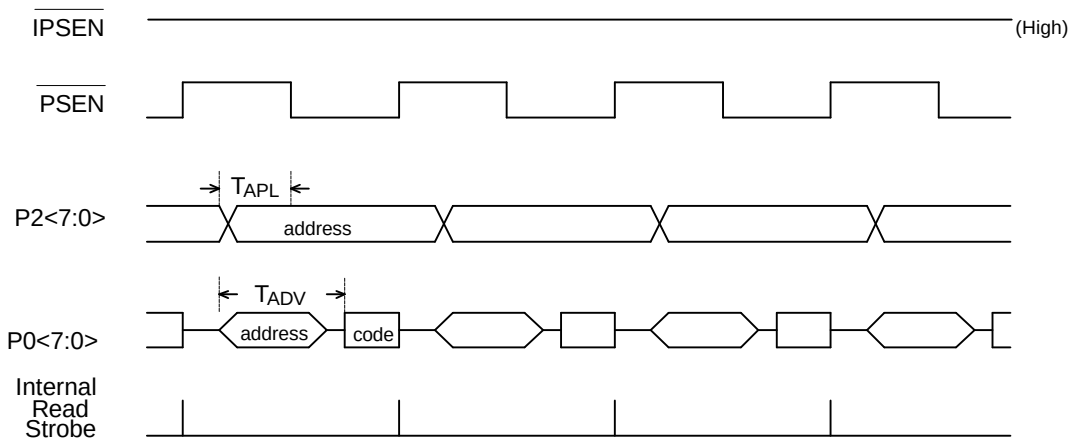
Program Fetch Cycle in Standard Type (Example: W78C52)



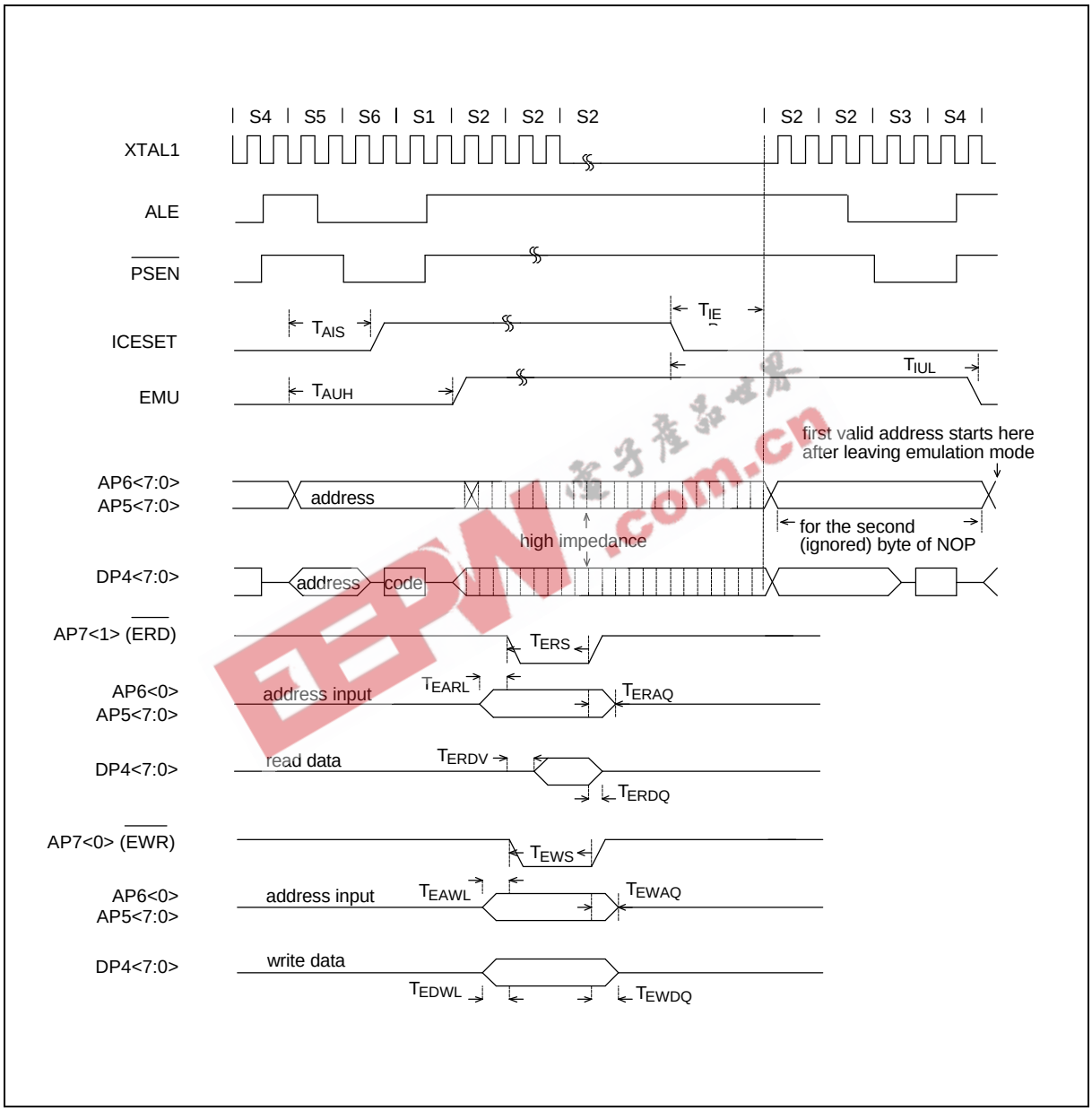
Internal (address: 0 ~ 1FFFH) program fetch:



External (address: 2000H ~ 0FFFFH) program fetch:

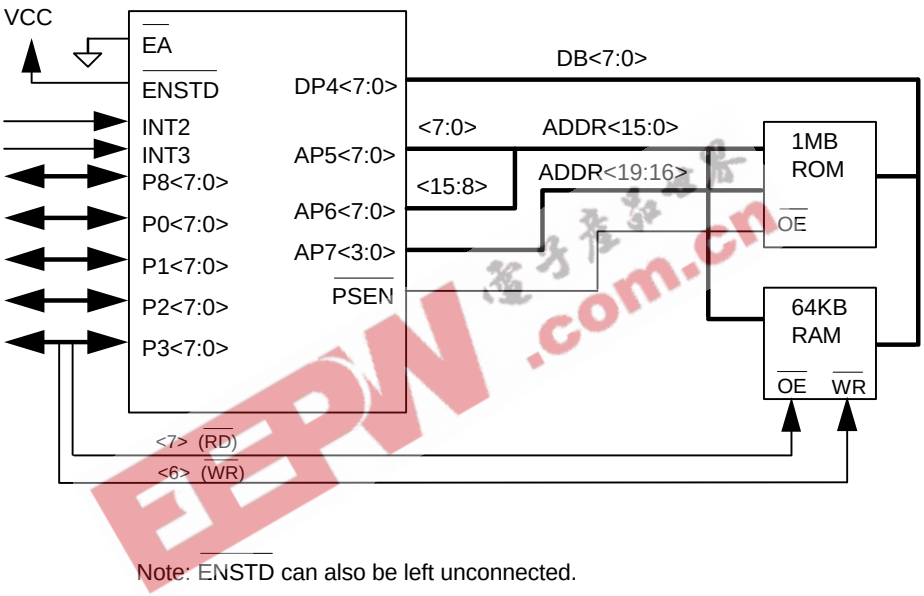


Emulation Mode Cycle (Internal SFR/PC/RAM Access)



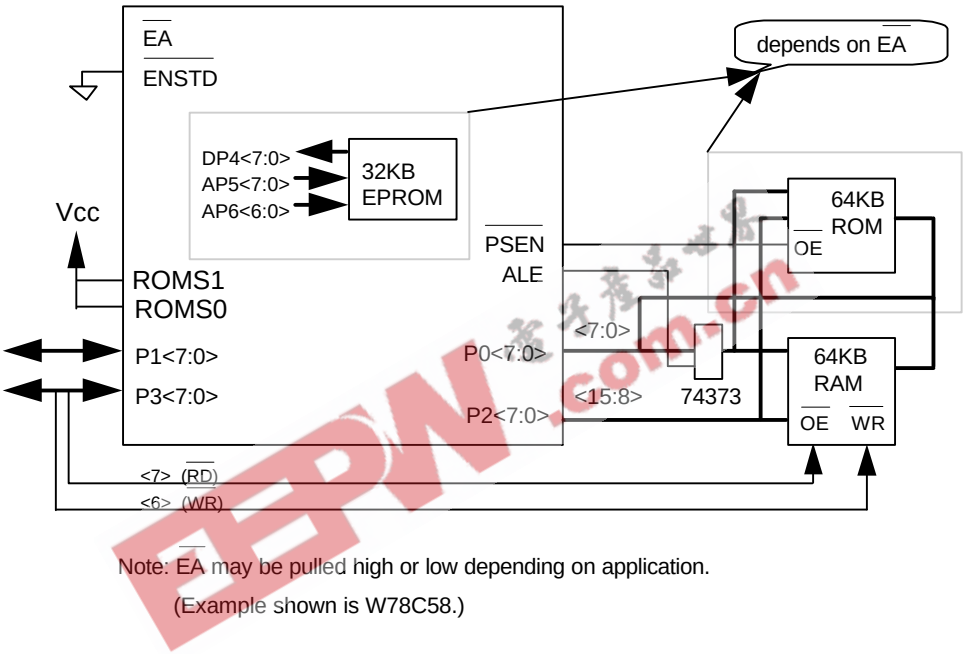
TYPICAL APPLICATION CIRCUITS

Advanced Type Application in Normal Mode



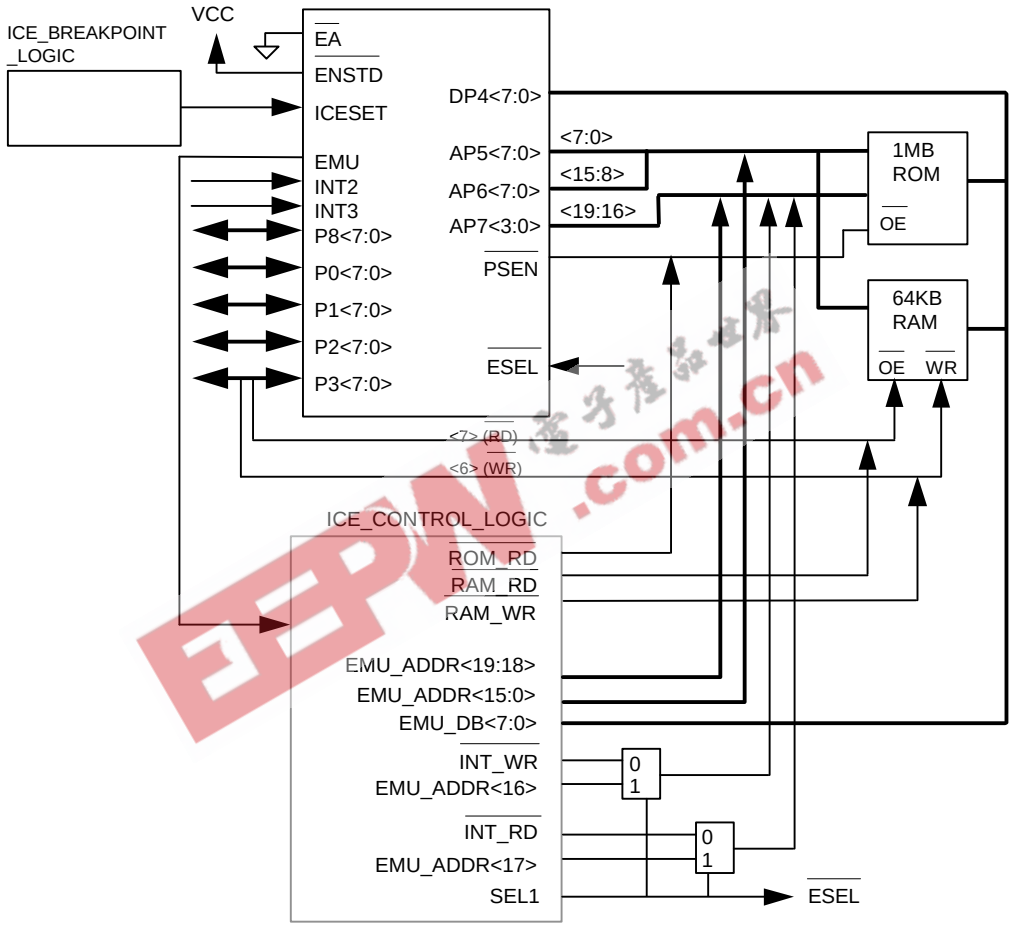
Note: ENSTD can also be left unconnected.

Standard Type Application in Normal Mode



Note: EA may be pulled high or low depending on application.
(Example shown is W78C58.)

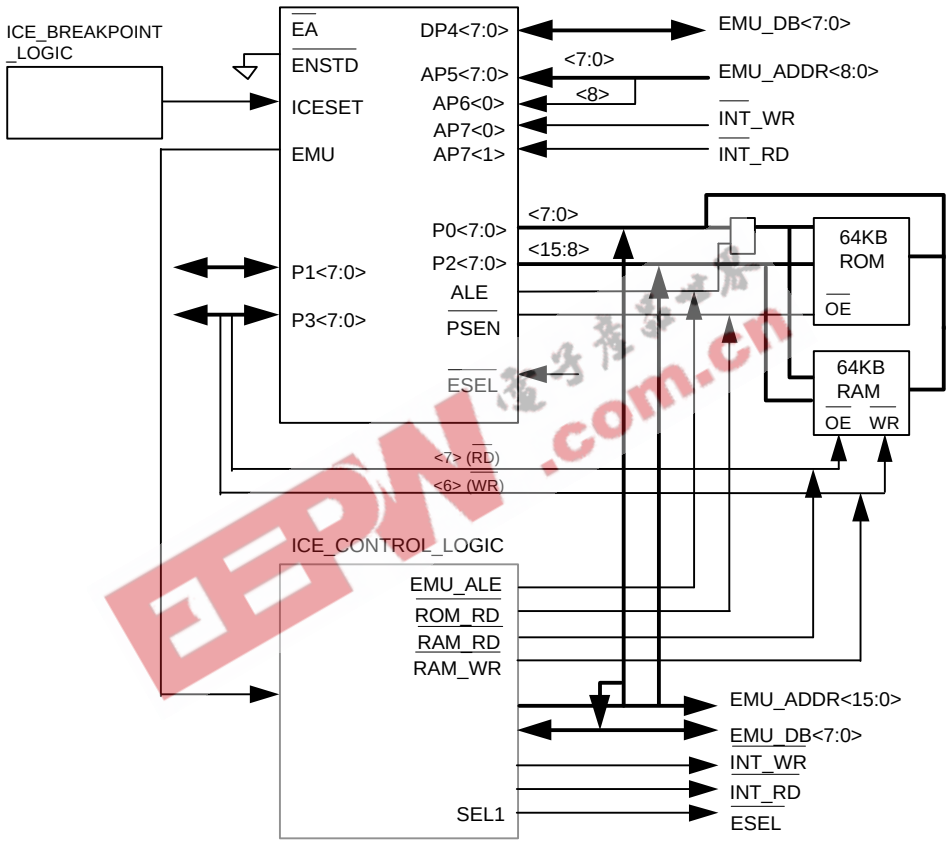
Advanced Type Application in Emulation Mode



SEL1	SEL0	access space		ESEL	AP6<0>
0	0	SFR/PC	80 - FF	0	0
0	1	Internal RAM	0 - FF	0	1
1	0	ROM	0 - FFFFF	1	-
1	1	RAM	0 - FFFF	1	-

Note: When ESEL=1, ALE and PSEN are high-impedence.

Standard Type Application in Emulation Mode

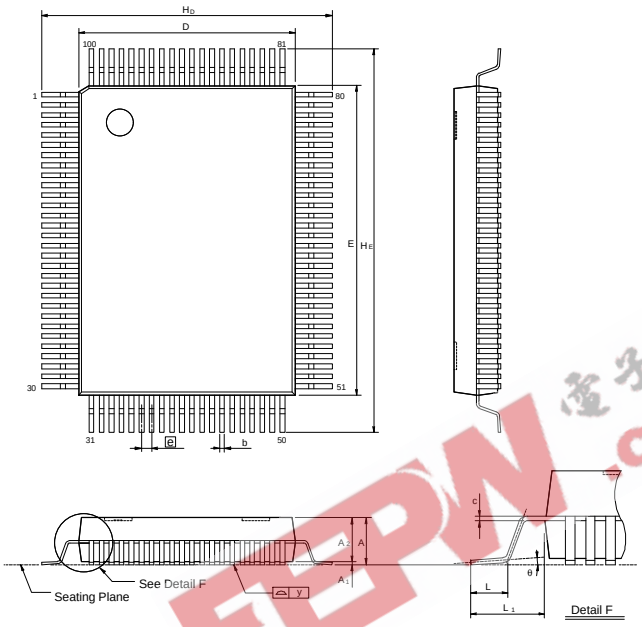


SEL1	SEL0	Access Space		ESEL	AP6<0>
0	0	SFR/PC	80 - FF	0	0
0	1	Internal RAM	0 - FF	0	1
1	0	ROM	0 - FFFFF	1	-
1	1	RAM	0 - FFFF	1	-

Note: When ESEL = 1, ALE and PSEN are high-impedence.

PACKAGE DIMENSIONS

100-pin QFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.718	2.845	2.972
b	0.010	0.012	0.016	0.254	0.305	0.407
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	0.991	1.194	1.397
L_1	0.087	0.095	0.103	2.21	2.413	2.616
y	—	—	0.004	—	—	0.102
θ	0°	—	12°	0°	—	12°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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