256K x 8 Static RAM

Features

- **High Speed**
  - **70ns availability**
- **Voltage range**
  - **2.7V–3.6V**
- **Ultra low active power**
  - **Typical active current: 1 mA @ f = 1MHz**
  - **Typical active current: 7 mA @ f = f_{max} (70ns speed)**
- **Low standby power**
- **Easy memory expansion with $\overline{CE_1}$, CE_2, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The WCMA2008U1X is a high-performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is device is ideal for portable applications. The device also has an automatic power-down feature that significantly reduc-es power consumption by 80% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE_1}$ HIGH or CE_2 LOW).
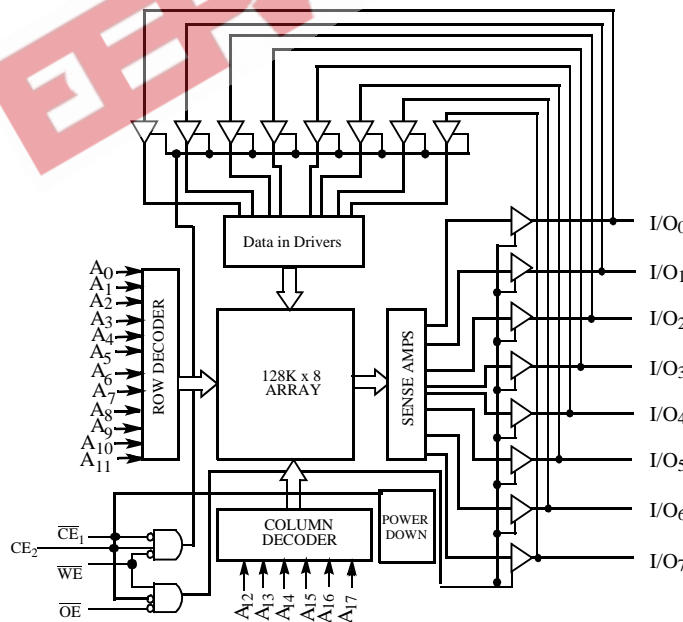
Writing to the device is accomplished by taking Chip Enable ($\overline{CE_1}$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable 2 (CE_2) HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{17}).
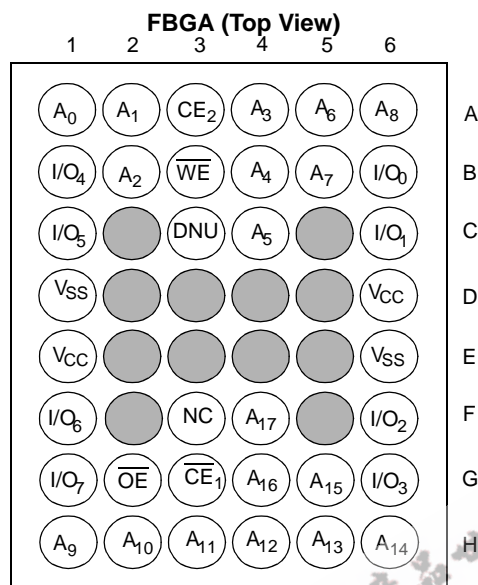
Reading from the device is accomplished by taking Chip Enable ($\overline{CE_1}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable 2 (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE_1}$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

The WCMA2008U1X is available in a 36-ball FBGA package.

Logic Block Diagram

Pin Configurations

FBGA (Top View)

	1	2	3	4	5	6	
A	A_0	A_1	CE_2	A_3	A_6	A_8	
B	I/O_4	A_2	$\overline{WE}$	A_4	A_7	I/O_0	
C	I/O_5		DNU	A_5		I/O_1	
D	V_{SS}					V_{CC}	
E	V_{CC}					V_{SS}	
F	I/O_6		NC	A_{17}		I/O_2	
G	I/O_7	$\overline{OE}$	$\overline{CE_1}$	A_{16}	A_{15}	I/O_3	
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied..55°C to +125°C

Supply Voltage to Ground Potential..... ....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1] ....0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ....–0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)............................20 mA

Static Discharge Voltage ....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ....>200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}
WCMA2008U1X	Industrial	–40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating, I_{CC}				Standby (I_{SB2})	
					f = 1 MHz		f = f_{max}			
	Min.	Typ.[2]	Max.		Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.
WCMA2008U1X	2.7V	3.0V	3.6V	70 ns	1 mA	2 mA	7 mA	15 mA	1 µA	30 µA

Notes:
1. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Param-eter	Description	Test Conditions		WCMA2008U1X-70			Unit
				Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0$ mA	$V_{CC} = 2.7V$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA	$V_{CC} = 2.7V$			0.4	V
V_{IH}	Input HIGH Voltage			2.2		$V_{CC} + 0.5V$	V
V_{IL}	Input LOW Voltage			−0.5		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		−1		+1	µA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		−1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6V$ $I_{OUT} = 0$ mA CMOS Levels		7	15	mA
		$f = 1$ MHz			1	2	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$, $CE_2 < V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$				100	µA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC} - 0.3V$, $CE_2 < 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$			1	15	

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, $f = 1$ MHz, $V_{CC} = Vcc_{(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance[3] (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ_{JA}	55	°C/W
Thermal Resistance[3] (Junction to Case)		Θ_{JC}	16	°C/W

Note:
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms
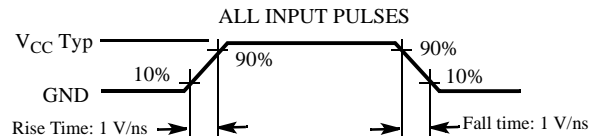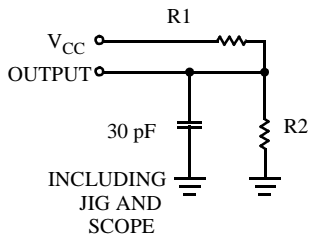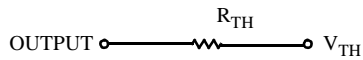
Parameters	3.3V	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		3.6	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$, $\overline{CE_1} \geq V_{CC} - 0.3V$, $CE_2 < 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		0.1	5	μA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0			ns
t_R[4]	Operation Recovery Time		100			ns

Data Retention Waveform
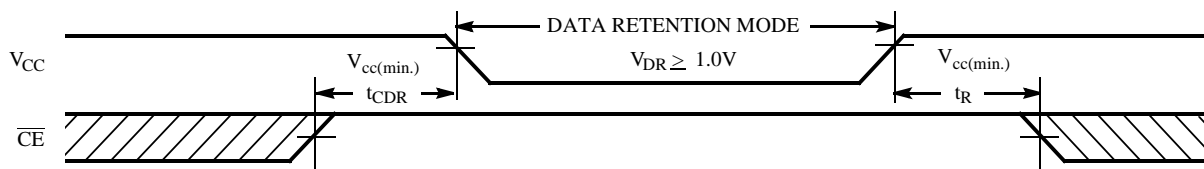
Note:
4.   Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100\,\mu s$ or stable at $V_{CC(min.)} \geq 100\,\mu s$.

## Switching Characteristics Over the Operating Range[5]

Parameter	Description	WCMA2008U1X-70		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		25	ns
t_{LZCE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Low Z[6]	10		ns
t_{HZCE}	$\overline{CE_1}$ HIGH or CE_2 LOW to High Z[6, 7]		25	ns
t_{PU}	$\overline{CE_1}$ LOW and CE_2 HIGH to Power-Up	0		ns
t_{PD}	$\overline{CE_1}$ HIGH or CE_2 LOW to Power-Down		70	ns
WRITE CYCLE[8,]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	10		ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
8. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) [9, 10]
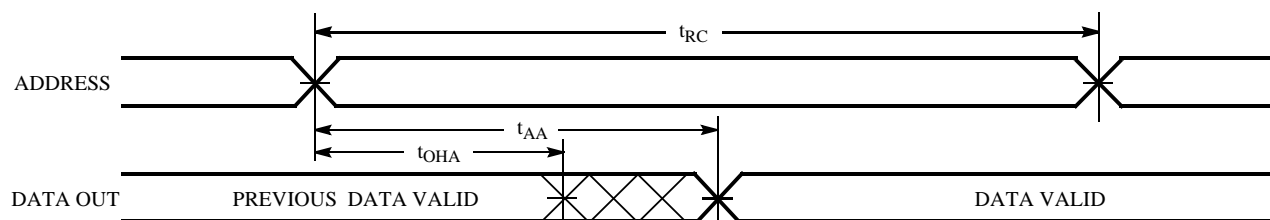
Read Cycle No. 2 (OE Controlled)[10, 11]
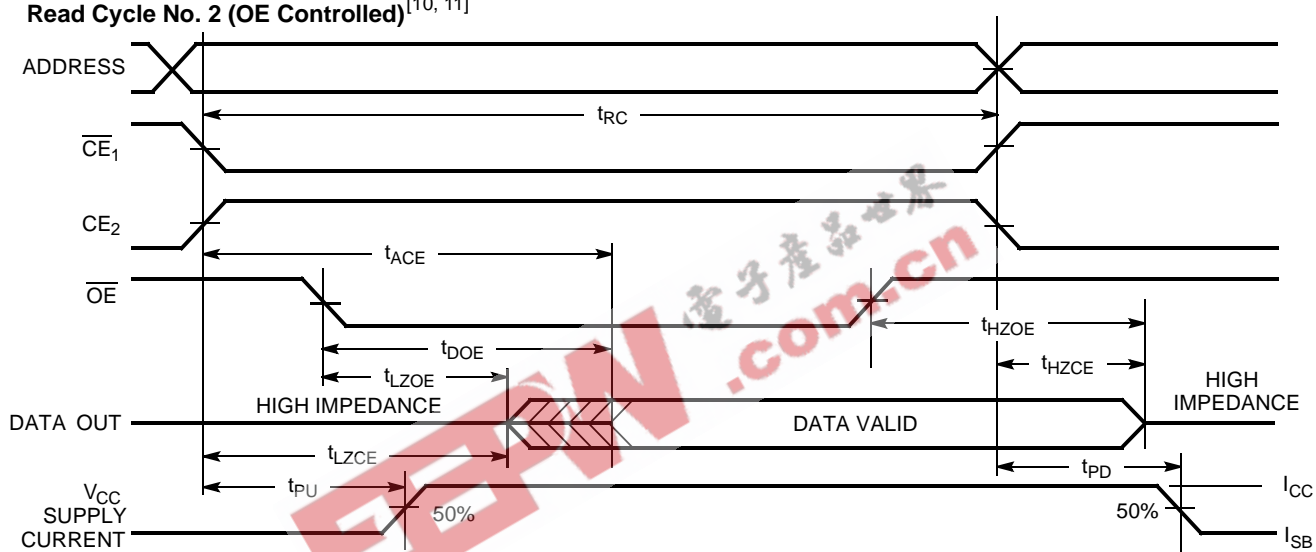

Notes:

9. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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Switching Waveforms (continued)

Write Cycle No. 1($\overline{\text{WE}}$ Controlled) [8, 12, 14]
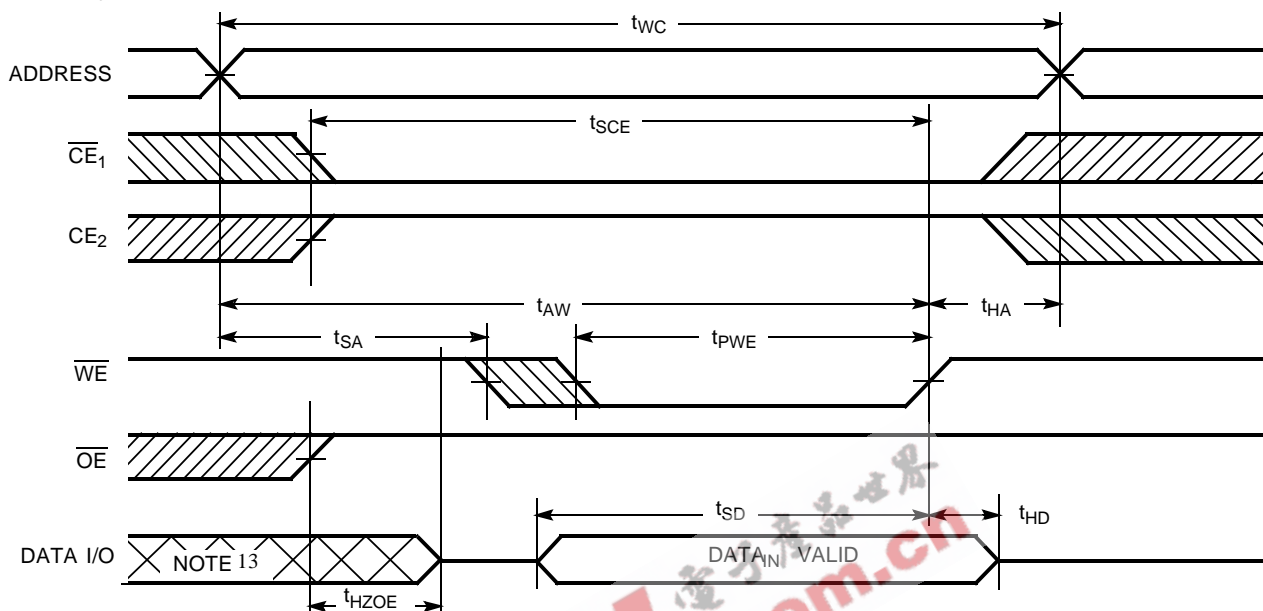
Write Cycle No. 2($\overline{\text{CE}}_1$ or CE$_2$ Controlled) [8, 12, 14]
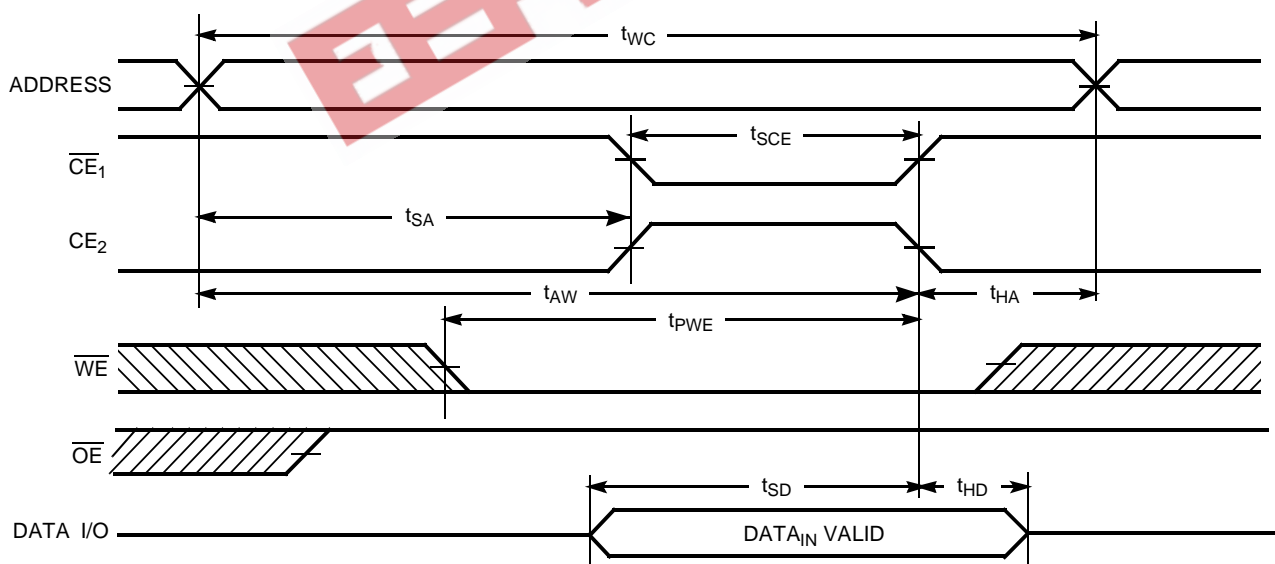
Notes:

12. Data I/O is high impedance if $\overline{\text{OE}}$ = V$_{IH}$.
13. During this period, the I/Os are in output state and input signals should not be applied.
14. If CE$_1$ goes HIGH or CE$_2$ goes LOW simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [14]
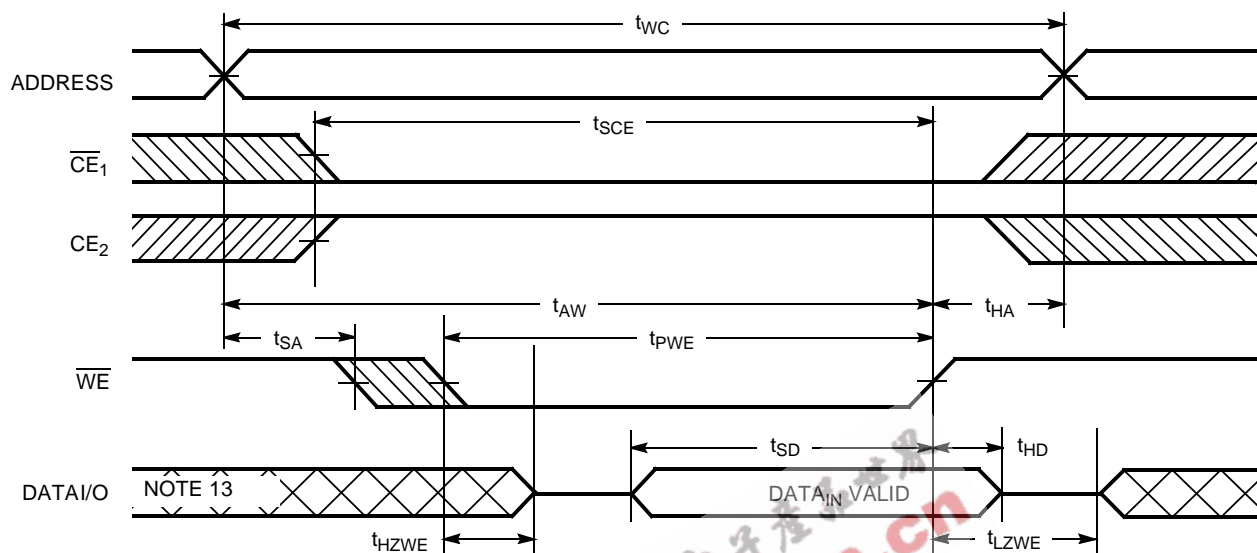
Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA2008U1X-FF70	FA36A	36-ball Fine Pitch BGA	Industrial

Package Diagrams

36-ball (7.0 mm x 7.0 mm x 1.2 mm) Fine Pitch BGA, FA36A
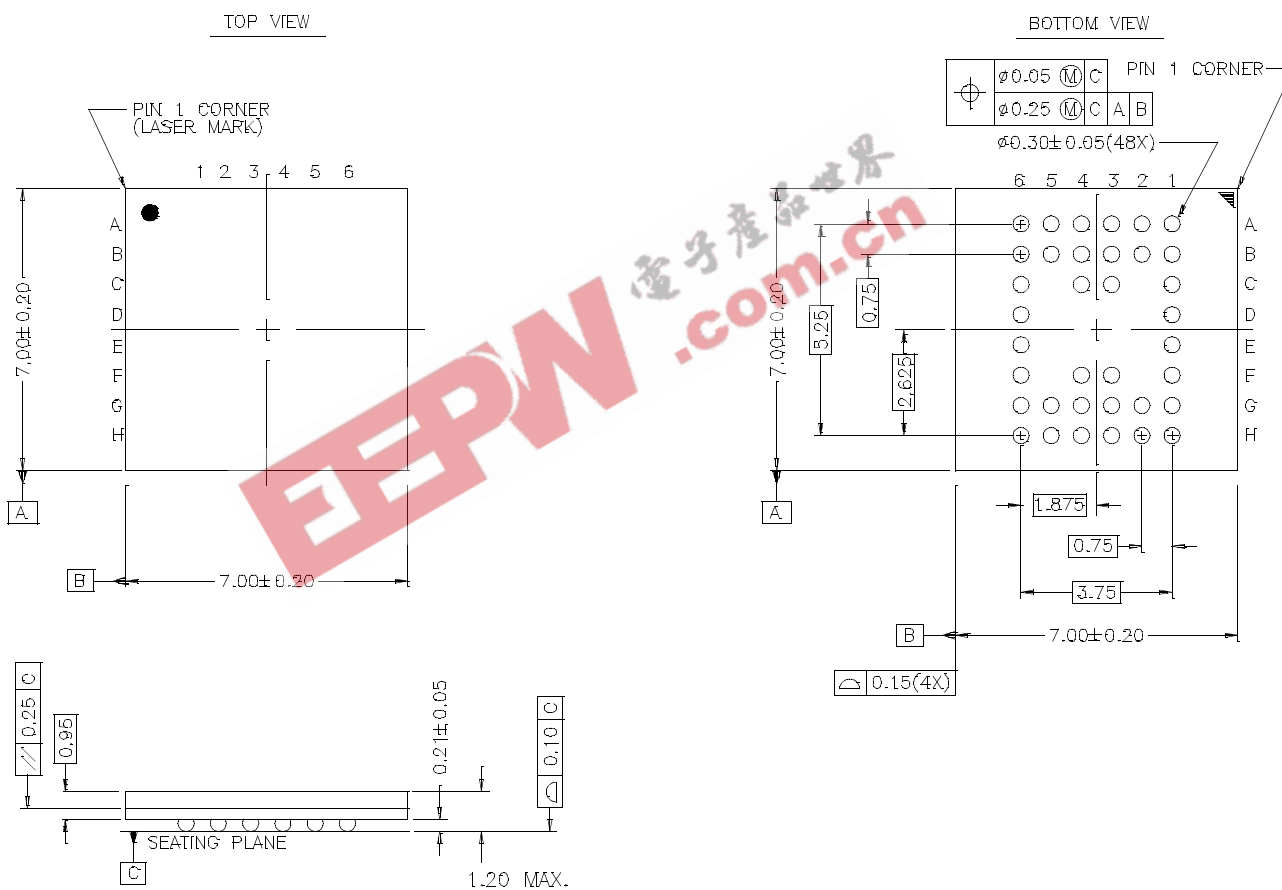
Document Title: WCMA2008U1X, 256K x 8 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-14021	115240	3/18/2002	MGN	New Data Sheet