Winbond Electronics Corp.

8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W78C54 is a derivative of the W78C52 microcontroller family that provides extended internal ROM. The chip has 16K bytes of mask ROM and 256 bytes of RAM.

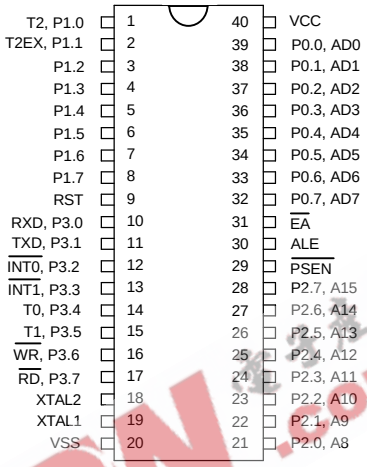
This device provides an enhanced architecture that makes it more powerful and suitable for a variety of applications for general control systems. It provides on-chip 16KB mask ROM to accommodate large program codes, 256-bytes of non-volatile on-chip RAM, four 8-bit I/O ports, one 4-bit I/O port, three 16-bit timer/counters, eight sources with two-level interrupt structures, and on-chip oscillator clock circuits.

FEATURES

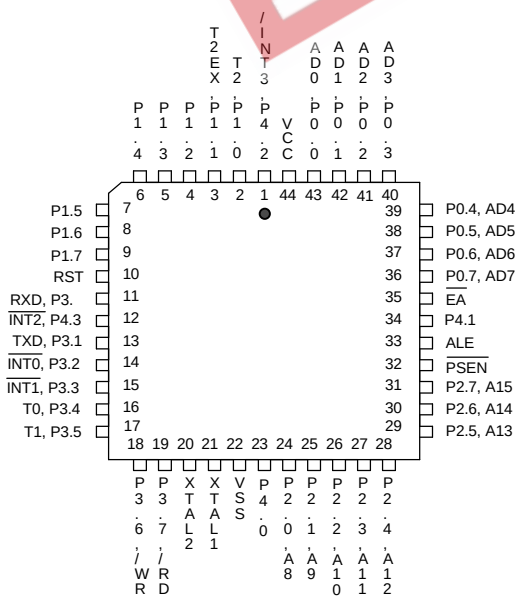
- DC to 40 MHz extensive operating frequency
- 256-byte on-chip scratch pad RAM
- 16K-byte on-chip mask ROM
- 64K-byte address space for external Program Memory
- 64K-byte address space for external Data Memory
- Three 16-bit timer/counters
- Four 8-bit bit-addressable I/O ports
- One extra 4-bit bit-addressable I/O port, additional $\overline{\text{INT2}}$/ $\overline{\text{INT3}}$ (Available on 44-pin PLCC/QFP package)
- Eight-source, two priority-level interrupts
- Low EMI emission mode
- Built-in programmable power-saving modes - Idle mode & Power-down mode
- Packages:
  - DIP 40: W78C54-16/24/40
  - PLCC 44: W78C54P-16/24/40
  - QFP 44: W78C54F-16/24/40
  - TQFP 44: W78C54M-16/24/40

PIN CONFIGURATIONS

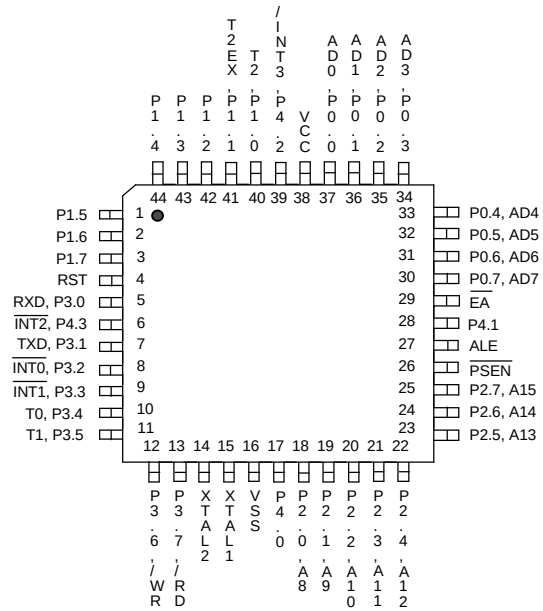
40-Pin DIP (W78C54)



44-Pin PLCC (W78C54P)



44-Pin QFP/TQFP (W78C54F/W78C54M)



PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
EA	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute out of external ROM. The ROM address and data will not be present on the bus if the $\overline{EA}$ pin is high and the program counter is within the 16 KB area. Otherwise they will be present on the bus.
PSEN	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
RST	I L	RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	CRYSTAL 1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O D	PORT 0: Function is the same as that of the standard 8052.
P1.0–P1.7	I/O H	PORT 1: Function is the same as that of the standard 8052.
P2.0–P2.7	I/O H	PORT 2: Function is the same as that of the standard 8052.
P3.0–P3.7	I/O H	PORT 3: Function is the same as that of the standard 8052.
P4.0–P4.3	I/O H	PORT 4: A 4-bit bi-directional parallel port and bit-addressable with internal pull-ups. Pin P4.3 and P4.2 have alternative function as external interrupt (INT2/INT3) source input.
INT2 (P4.3)	I H	External interrupt 2: An extra interrupt input source. It cascades to pin P4.3 internally.
INT3 (P4.2)	I H	External interrupt 3: An extra interrupt input source. It cascades to pin P4.2 internally.

* Note : **TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

BLOCK DIAGRAM

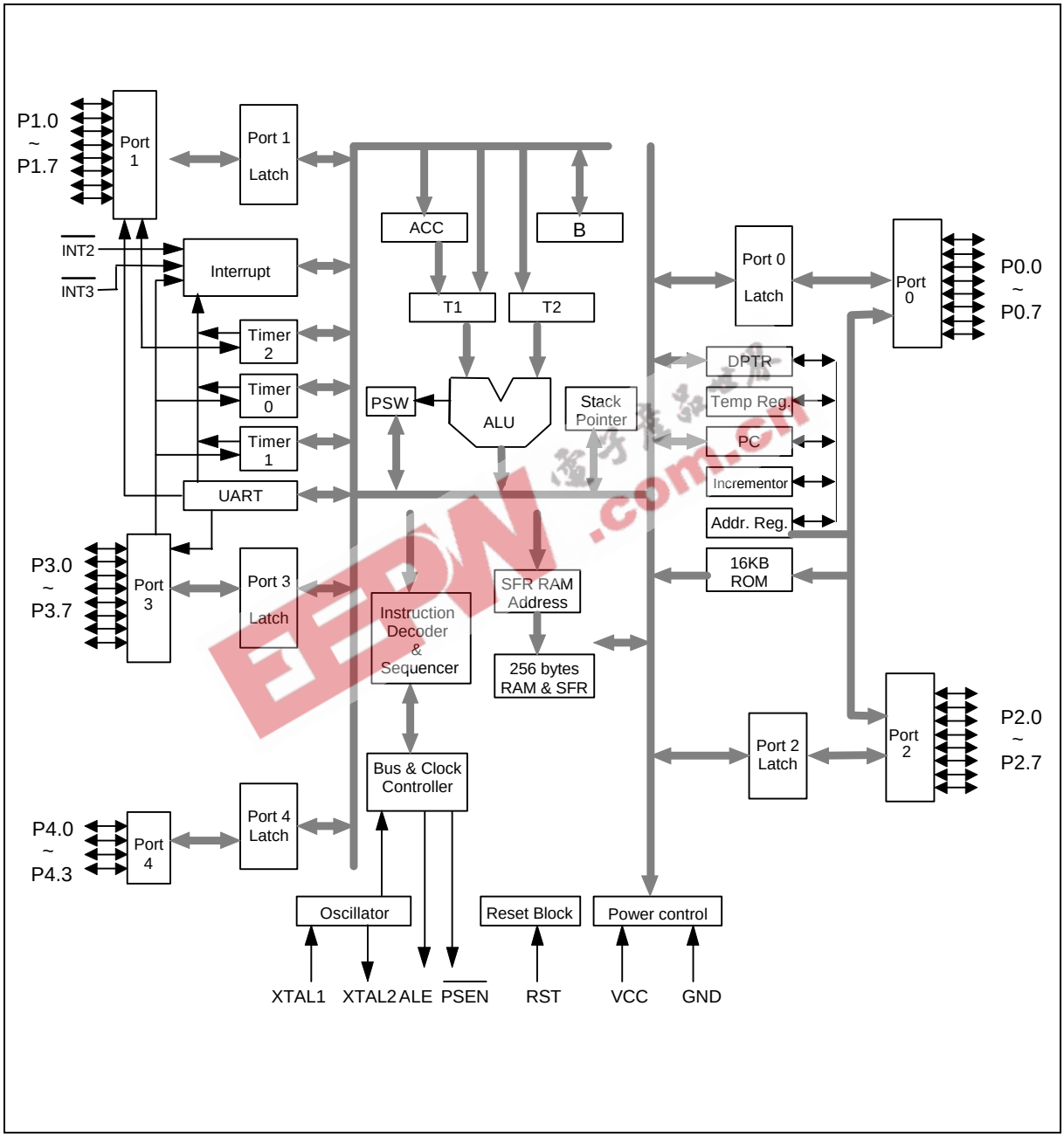


Figure 2. Architecture of the W78C54

FUNCTIONAL DESCRIPTION

The W78C54 is pin-to-pin compatible with the W78C52, except that the internal 8K mask ROM has been replaced with 16K of internal mask ROM. The processor supports 111 different opcodes and references both 64K program address space and 64K data storage space.

Clock

The W78C54 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78C54 relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78C54 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal is connected across pins XTAL1 and XTAL2. In addition, a load capacitance of 30 pf (typically) must be connected from each pin to ground. Resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level greater than 3.5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDLE bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line when the W78C54 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt INT2, INT3 has been added to either the PLCC or QFP 44 pin package. And description follows:

1. INT2 / INT3

Two additional external interrupts, $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

2. PORT4

Another bit-address port P4 is also available except only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1,except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources (INT2/INT3).

Example:

```
P4      REG     0D8H
MOV     P4, #0AH    ; Output data "A" through P4.0–P4.3.
MOV     A, P4       ; Read P4 status to Accumulator.
SETB    P4.0        ; Set bit P4.0
CLR     P4.1        ; Clear bit P4.1
```

Reduce EMI Emission

Because of the large on-chip mask-ROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is useless. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space..

POF Flag

The Power-Off-Reset flag is set by on-chip circuitry when the V_{CC} level rises from 0 to 5V. The POF bit can be set/cleared by software allowing a user to determine if the reset is the result of a power-on or a warm up by external reset. To avoid effect of POF flag, the power voltage must remain above 3V.

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0, 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78C52C: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

DESCRIPTIONS OF THE SPECIAL FUNCTION REGISTERS (SFRS)

SYM.	DEFINITION	ADDR.	MSB		BIT ADDRESS, SYMBOL					LSB	RESET
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
P4*	Port 4	D8H	-	-	-	-	(DB) INT2	(DA) INT3	(D9)	(D8)	xxxx0000B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) -	(D0) P	00000000B
TH2	T2 reg. high	CDH									00000000B
TL2	T2 reg. low	CCH									00000000B
RCAP2H	T2 capture high	CBH									00000000B
RCAP2L	T2 capture low	CAH									00000000B
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	00000000B
XICON*	External interrupt control	C0H	(C7) PX3	(C6) EX3	(C5) IE3	(C4) IT3	(C3) PX2	(C2) EX2	(C1) IE2	(C0) IT2	00000000B
IP	Interrupt priority	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	11111111B
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	00000000B
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	11111111B
SBUF	Serial buffer	99H									xxxxxxxxB
SCON*	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	00000000B
P1*	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91) T2EX	(90) T2	11111111B
AUXR*	Auxiliary	8EH	-	-	-	-	-	-	-	AO	xxxxxxx0B
TH1	Timer high 1	8DH									00000000B
TH0	Timer high 0	8CH									00000000B
TL1	Timer low 1	8BH									00000000B
TL0	Timer low 0	8AH									00000000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00000000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	00000000B
PCON*	Power control	87H	SMOD	SMOD0	-	POF+	GF1	GF0	PD	IDL	00xxxx00B
DPH	Data pointer high	83H									00000000B
DPL	Data pointer low	82H									00000000B
SP	Stack pointer	81H									00000111B
P0	Port 0	80H	(87)	(86)	(85)	(84)	(83)	(82)	(81)	(80)	11111111B

Note: In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.

* SFRs modified or added to the W78C52. + Reset value depends on reset condition.

W78C54 SFRs address location map:

F8									FF
F0	+ B								F7
E8									EF
E0	+ ACC								E7
D8	**+P4**								DF
D0	+ PSW								D7
C8	+T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	+XICON								C7
B8	+ IP								BF
B0	+ P3								B7
A8	+ IE								AF
A0	+ P2								A7
98	+ SCON	SBUF							9F
90	+ P1								97
88	+ TCON	TMOD	TL0	TL1	TH0	TH1	AUXR		8F
80	+P0	SP	DPL	DPH				PCON	87

Notes:

1. + SFR is bit-addressable.
2. is additional defined function.

Power-off Flag

***PCON - Power Control (87H)

SMOD	SMOD0	-	POF	GF1	GF0	PD	IDL

SMOD: Double baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2, 3.

SMOD0: Enable FE bit in SCON. This bit is an alternative switch of SM0 and FE (Frame Error) bit. When set to a 1, SCON.7 means a FE bit, otherwise a SM0 bit.

POF: Power off flag. Bit is set by hardware when power on reset. It can be cleared by software to determine chip reset is a warm boot or cold boot.

GF1, GF0: These two bits are general-purpose flag bits for the user.

PD: Power down mode bit. Set it to enter power down mode.

IDL: Idle mode bit. Set it to enter idle mode.

The power-off flag is located at PCON.4. This bit is set when V_{DD} has been applied to the part. It can be used to determine if a reset is a warm boot or a cold boot if it is subsequently reset by software.

* Interrupts

***IE - Interrupt Enable (A8H)

EA	-	ET2	ES	ET1	EX1	ET0	EX0

EA: Lobal interrupt enable flag

ET2: Timer 2 overflow interrupt enable

ES: Serial port interrupt enable

EX1: External interrupt 1 enable

ET1: Timer 1 overflow interrupt enable

EX0: External interrupt 0 enable

***IP - Interrupt Priority (B8H)

-	-	PT2	PS	PT1	PX1	PT0	PX0

PT2: Timer 2 interrupt priority high if set

PS: Serial port priority high if set

PT1: Timer 1 interrupt priority high if set

PX1: External interrupt 1 priority high if set

PT0: Timer 0 interrupt priority high if set

PX0: External interrupt 0 priority high if set

***XICON - External Interrupt Control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

The W78C54 supports an eight-source and a four-priority-level interrupt architectures. Besides the SFRs of IP and IE to control the six-source of the standard 8052 interrupt functions. There is an another SFR (XICON) to control the extra two-source of the external interrrupt (INT2 and INT3). This priority scheme is formed by combining IPH with IP to determine the priority of each interrupt. Except the INT2 and INT3, they are not defined in IP SFR but in XICON.

Following tables show the interrupt informations and priority definitions.

Eight-source interrupt informations:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.IT0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.IT1
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.EX2	XICON.IT2
External Interrupt 3	3BH	7 (lowest)	XICON.EX3	XICON.IT3

***Timer/Counter**

*****TL0, TH0, TL1, TH1, TL2, TH2, RCAP2L, RCAP2H**

*****TMOD - Timer 0, 1 mode (89H)**

GATE	C//T	M1	M0	GATE	C//T	M1	M0
TIMER0				TIMER1			

GATE: Gating control. When set, Timer/counter x is enabled only while INTx pin is high and TRx control pin is set. When cleared, Timer x is enabled whenever the TRx conrol bit is set.

C//T: Timer or Counter Selector. Cleared for timer operation. Set for counter operation.

M1 M0: Operating Mode

0 0: 13-bit Timer/Counter.

0 1: 16-bit Timer/Counter.

1 0: 8-bit auto-reload Timer/Counter. THx holds a value which is to be reloaded into TLx each time it overflows.

1 1: Timer 0: TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits.
TH0 is an 8-bit timer only controlled by Timer 1 control bits.
Timer 1: Timer/counter 1 stopped.

*****TCON - Timer 0, 1 Control (88H)**

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1: Timer 1 overflow flag. Set by hardware on timer/counter overflow. cleared by hardware when processor vectors to interrupt routine.

TR1: Timer 1 run control bit. Set/cleared by software to turn timer/counter on or off.

TF0: Timer 0 overflow flag. Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.

TR0: Timer 0 run control bit. Set/cleared by software to turn timer/counter on or off.

IE1: Interrupt 1 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.

IT1: Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.

IE0: Interrupt 0 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.

IT0: Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.

*****T2CON - Timer 2 Control (C8H)**

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C//T	CP//RL2

TF2: Timer 2 overflow flag. Set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when RCLK = 1 or TCLK = 1.

EXF2: Timer2 external flag. Set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.

RCLK: Receive clock flag. RCLK = 1 causes the serial port to use Timer 2 overflow pulses for its receive clock in mode 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

TCLK: Transmit clock flag. TCLK = 1 causes the serial port to use Timer 2 overflow pulses for its transmit clock in mode 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.

EXEN2: Timer 2 external enable flag. EXEN2 = 1 allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.

TR2: TR2 = 1/0: turns on/off Timer 2.

C//T: Timer or Counter select. Set 1/0 for external event counter(falling edge triggered)/inter timer.

CP//RL2: Capture/reload flag.

*Reduced EMI Mode

The AO bit in the AUXR register, when set, disables the ALE output.

*****AUXR - Auxiliary Register (8EH)**

-	-	-	-	-	-	-	AO

AO: Turn off ALE output.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{CC}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{CC} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(V_{DD}–V_{SS} = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
Idle Current	I_{IDLE}	-	6	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	50	µA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	µA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL} [*4]	-500	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*4]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1 [*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
Output Low Voltage P0, ALE, PSEN [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Sink Current P1, P2, P3, P4	I_{SK1}	4	8	mA	V_{DD} = 4.5V Vs = 0.45V
Sink Current P0, ALE, $\overline{PSEN}$	I_{SK2}	10	14	mA	V_{DD} = 4.5V Vs = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 µA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 µA
Source Current P1, P2, P3, P4	I_{SR1}	-120	-180	µA	V_{DD} = 4.5V Vs = 2.4V
Source Current P0, ALE, $\overline{PSEN}$	I_{SR2}	-10	-14	mA	V_{DD} = 4.5V Vs = 2.4V

Notes:

*1. RST pin is a Schmitt trigger input. RST has internal pull-low resistors of about 30 KΩ.

*3. P0, ALE and /PSEN are tested in the external access mode.

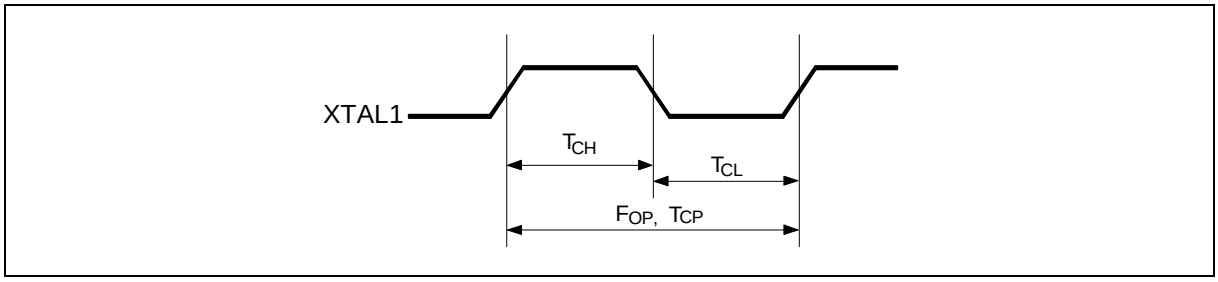
*4. XTAL1 is a CMOS input.

*5. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.8 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



Continued

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	TCH	10	-	-	nS	3
Clock Low	TCL	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

External Program Memory Fetch Cycle (see Figure 6)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UINT	NOTES
Address Valid to ALE Low	TAAS	1TCP -Δ	-	-	nS	
Address Hold After ALE Low	TAAH	1TCP -Δ	-	-	nS	1
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1TCP -Δ	1TCP	1TCP+Δ	nS	
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2TCP	nS	2
Data Hold After $\overline{\text{PSEN}}$ High	TPDH	0	-	1TCP	nS	3
Data Float After $\overline{\text{PSEN}}$ High	TPDZ	0	-	1TCP	nS	
ALE Pulse Width	TALW	2TCP -Δ	2TCP	2TCP +Δ	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3TCP -Δ	3TCP	3TCP +Δ	nS	4

Notes:
1. P00-P07, P20-P27 remain stable through entire memory cycle.
2. Memory access time is 3 Tcp.
3. Data has been latched internally prior to /PSEN going high.
4. Δ is 20 ns (due to buffer driving delay and wire loading).

Data Read Cycle

External Data Memory Read Cycle (see Figure 7)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UINT	NOTES
ALE Low to $\overline{RD}$ Low	TDAR	3 Tcp-Δ	3 Tcp	3 Tcp+Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	TDDA	-	-	4 Tcp	nS	1
Data hold After $\overline{RD}$ High	TDDH	0	-	2 Tcp	nS	
Data Float After $\overline{RD}$ High	TDDZ	0	-	2 Tcp	nS	
$\overline{RD}$ Pulse Width	TDRD	6 Tcp-Δ	6 Tcp	6 Tcp+Δ	nS	2

Notes:
1. Data Memory access time is 5 Tcp.
2. Δ is 20 ns (due to buffer driving delay and wire loading.

Data Write Cycle

External Data Memory Write Cycle (see Figure 8)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UINT	NOTE
ALE Low to $\overline{WR}$ Low	TDAW	3 Tcp-Δ	3 Tcp	3 Tcp+Δ	nS	*
Data Valid to $\overline{WR}$ Low	TDAD	1 Tcp-Δ	-	-	nS	
Data hold After $\overline{WR}$ High	TDWD	1 Tcp-Δ	-	-	nS	
$\overline{WR}$ Pulse Width	TDWR	6 Tcp-Δ	6 Tcp	6 Tcp+Δ	nS	*

*Note: Δ is 20 ns (due to buffer driving delay and wire loading)

Port Access Cycle

Port Access Cycle (see Figure 9)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UINT
Port Input Setup to ALE Low	TPDS	1Tcp	-	-	nS
Port Input Hold After ALE Low	TPDH	0	-	-	nS
Port Output to ALE High	TPDA	1Tcp-Δ	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

TIMING WAVEFORMS

Program Fetch Cycle

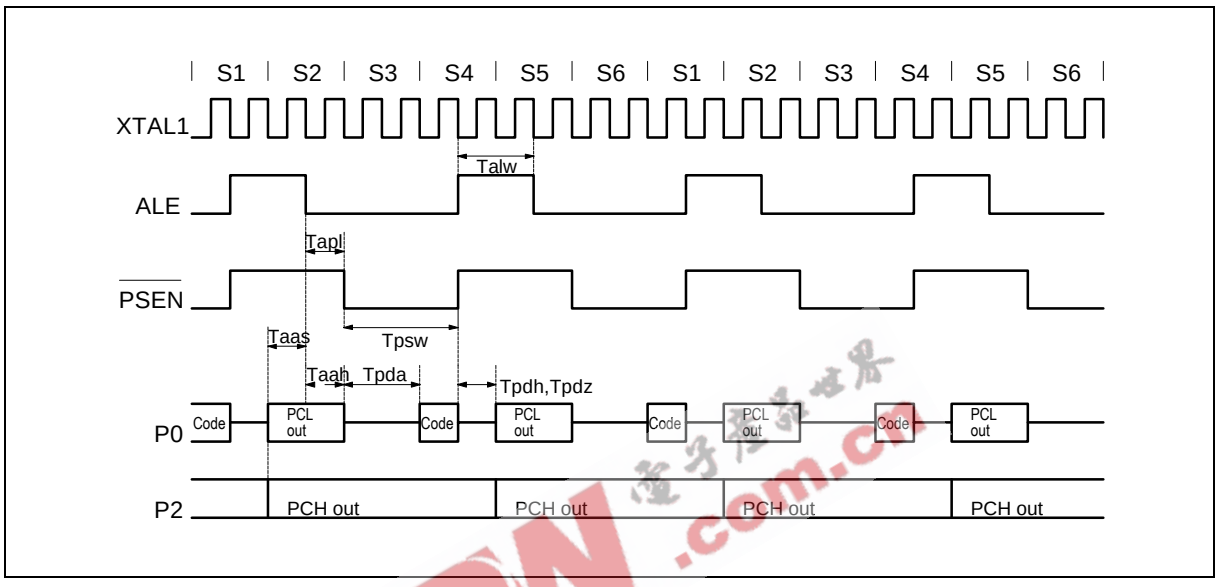


Figure 6. External Program Memory Fetch Cycle

Data Read Cycle

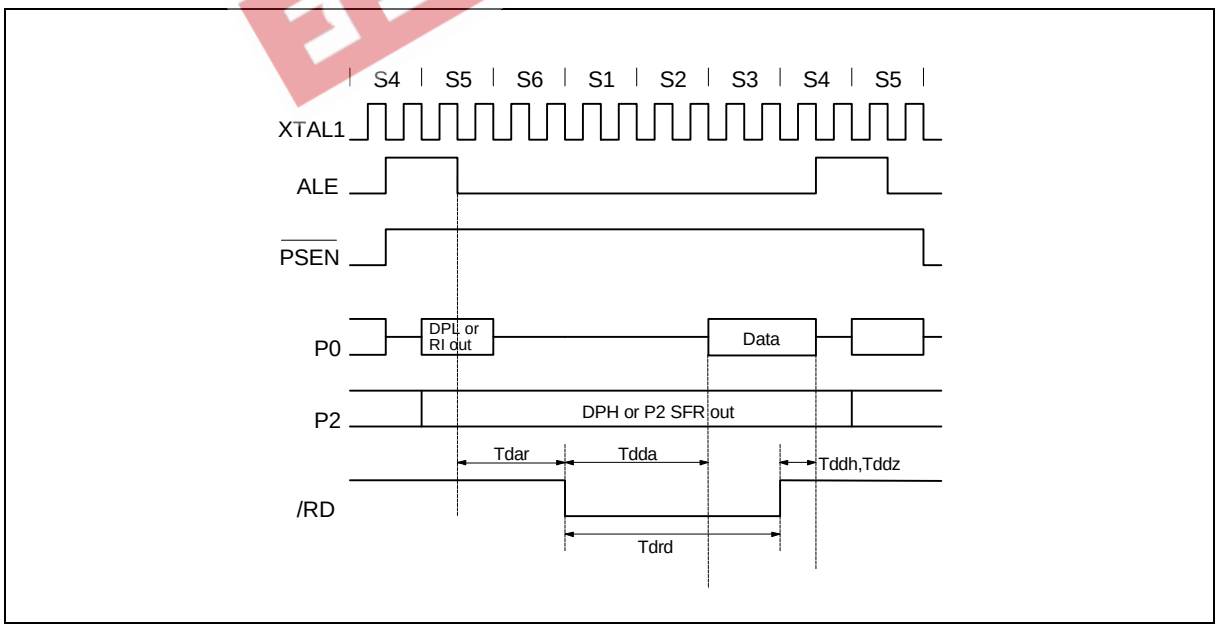


Figure7. External Data Memory Read Cycle

Timing Waveforms, continued

Data Write Cycle

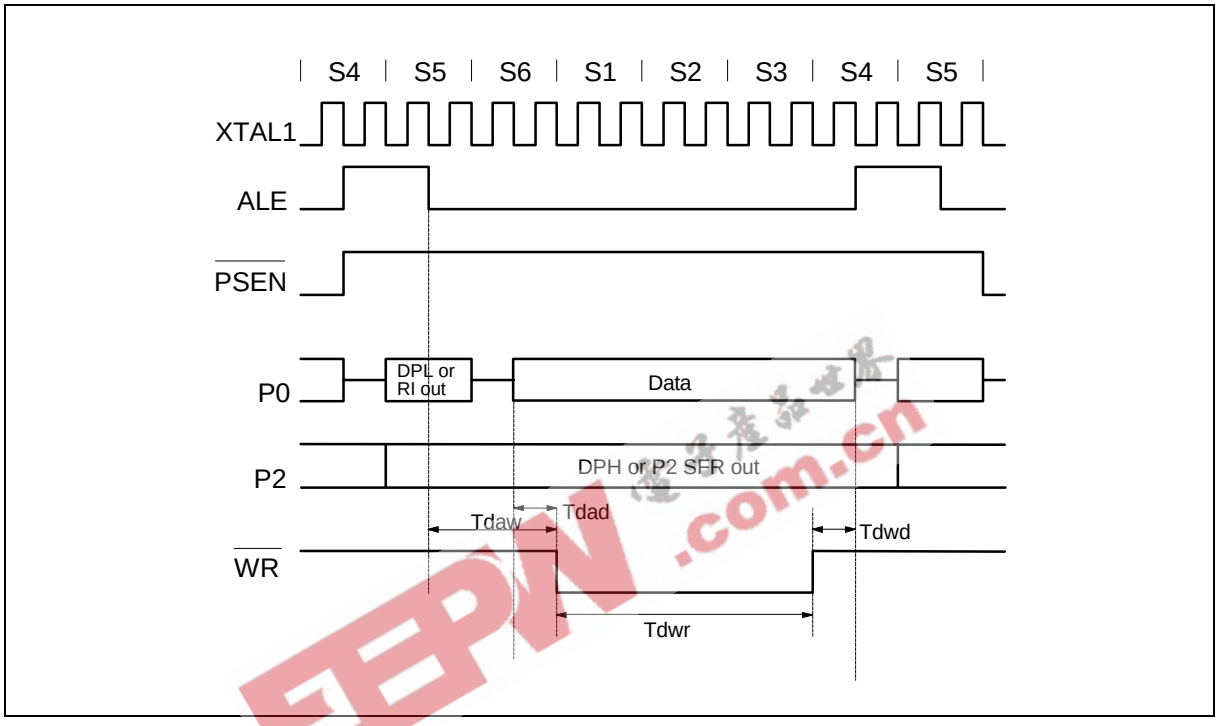


Figure 8. External Data Memory Write Cycle

Port Access Cycle

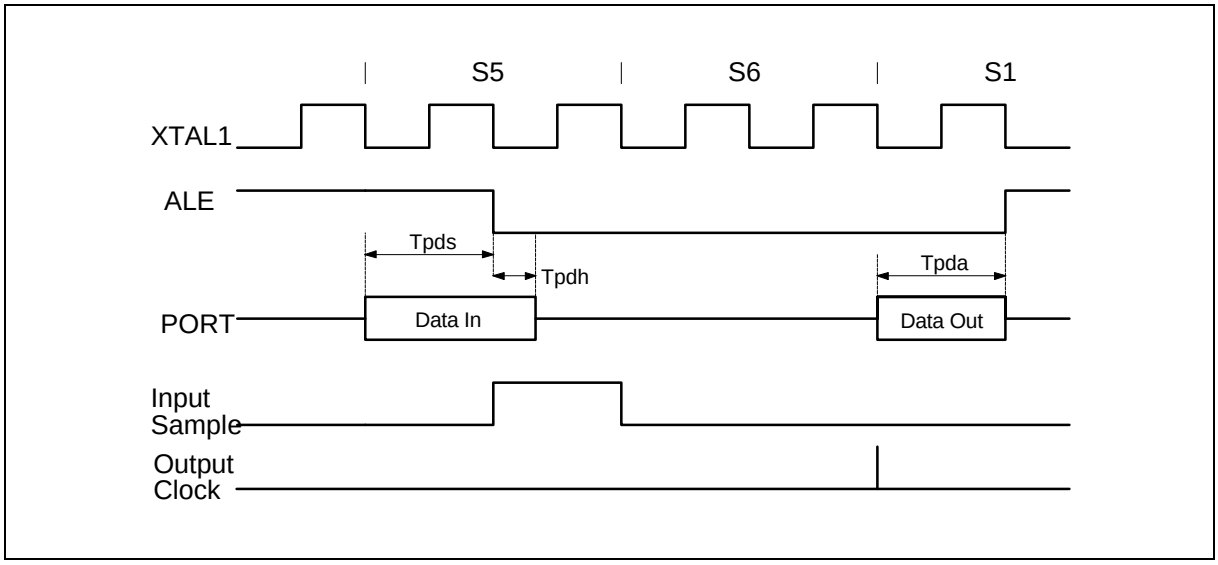


Figure 9. Port Access Cycle

APPLICATION CIRCUIT

Expanded External Program Memory and Crystal

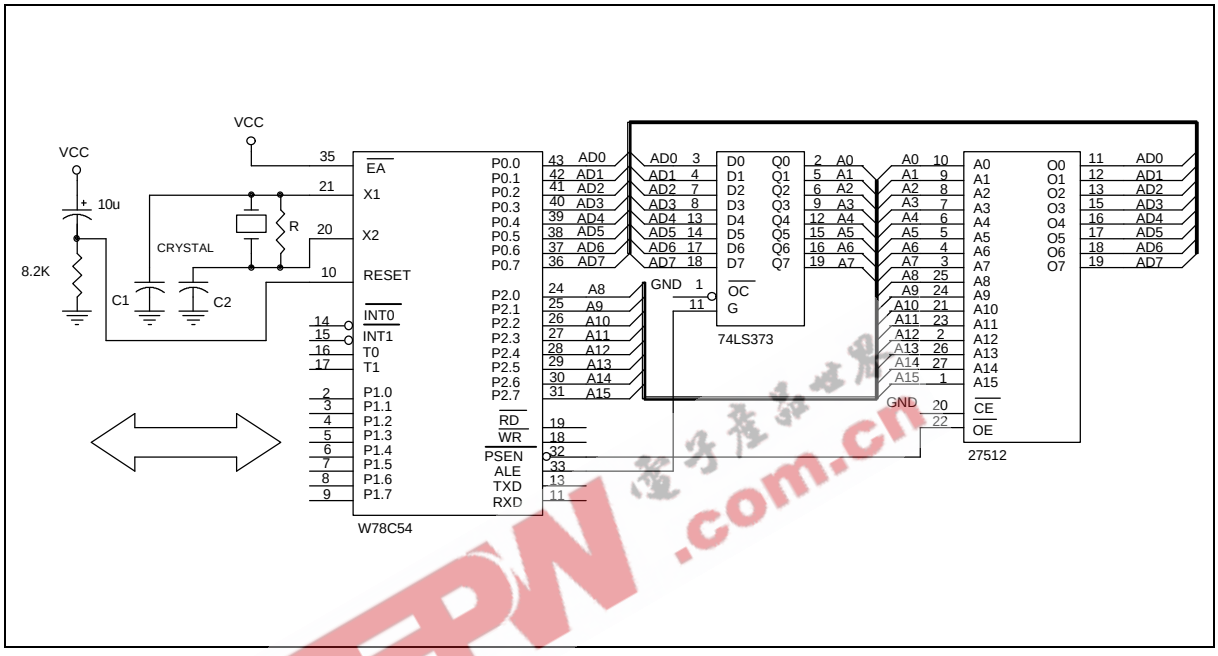


Figure A

Table 1 Shows the typical values of off-chip components to configure the on-chip oscillator.

Table 1. Off-chip components list

CRYSTAL FREQ.	C1	C2	R
12 MHz	30 pF	30 pF	-
16 MHz	30 pF	30 pF	-
20 MHz	15 pF	15 pF	-
24 MHz	15 pF	15 pF	-
33 MHz	10 pF	10 pF	6.8 KΩ
40MHz	5 pF	5 pF	4.3 KΩ

Notes:

1. Refer to Figure 10 for C1, C2 and R.
2. It is recommended that an oscillator be used as external clock source when operating freq. is above 35MHz. Apply the external clock signal to XTAL1, and leave XTAL2 float, as shown in Figure 10.

Application Circuit, continued

Expanded External Data Memory and Oscillator

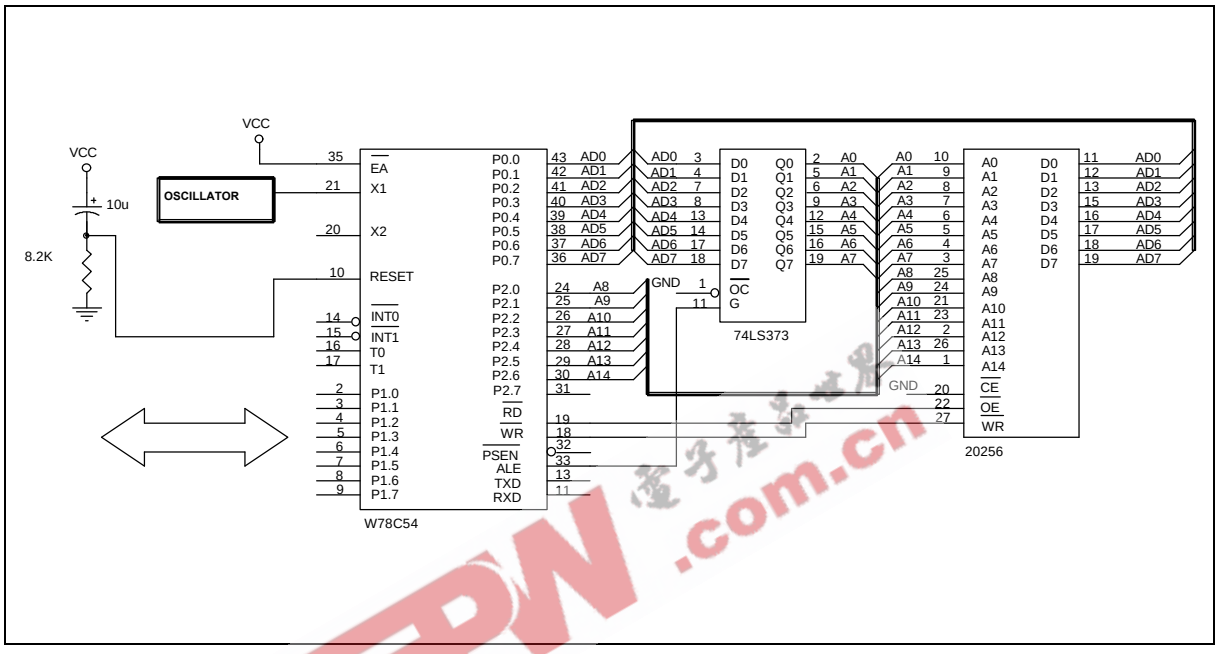


Figure B

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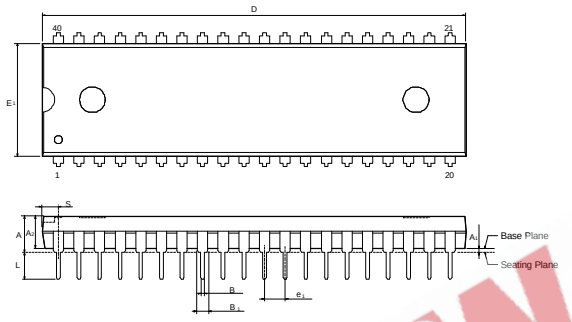
PACKAGE DIMENSIONS

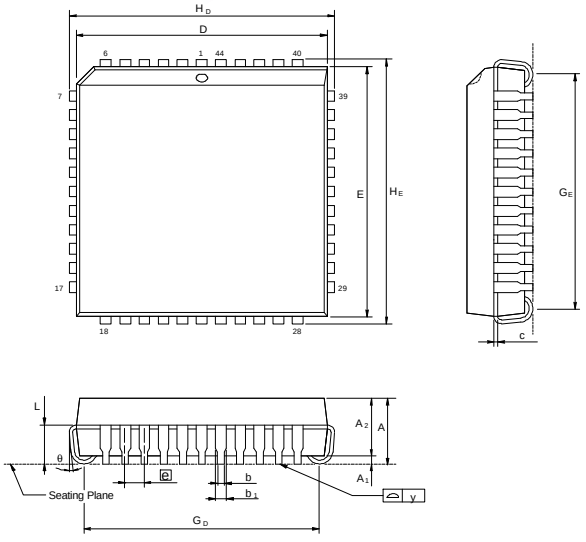
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC

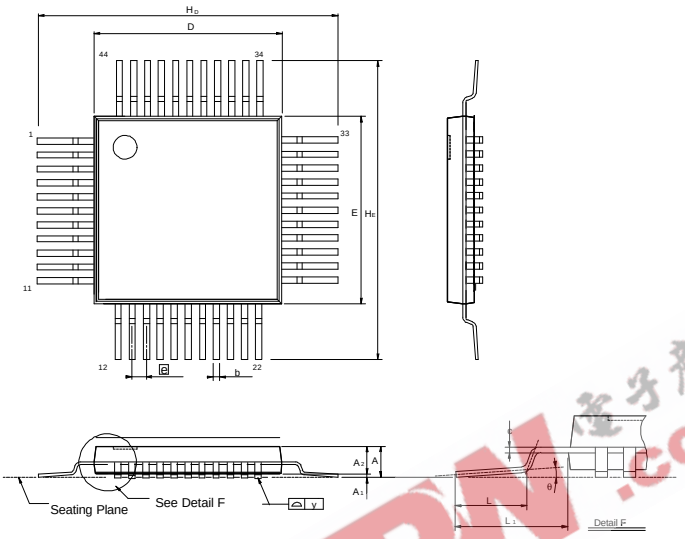


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued

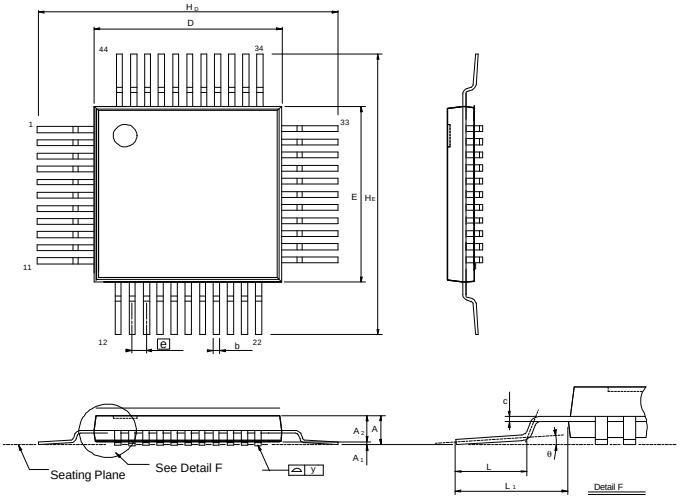
44-pin QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

44-pin TQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	0.047	---	---	1.20
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.0039	0.013	0.015	0.22	0.32	0.38
c	0.004	---	0.008	0.090	---	0.200
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.468	0.472	0.476	11.90	12.00	12.10
H_E	0.468	0.472	0.476	11.90	12.00	12.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	---	0.039	---	---	1.00	---
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

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