



128K x 8 Static RAM

Features

- **Voltage Range**
— 4.5V–5.5V
- **Low active power**
— Typical active current: 6 mA @ f = f_{max} (70 ns speed)
- **Low standby current**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with CE₁, CE₂, and OE features**
- **CMOS for optimum speed/power**

Functional Description

The WCMA1008C1X is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE₁), an active HIGH Chip Enable (CE₂), an active LOW Output Enable (OE), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking Chip Enable 1 (CE₁) and Write Enable (WE) inputs LOW and Chip Enable 2 (CE₂) input HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₆).

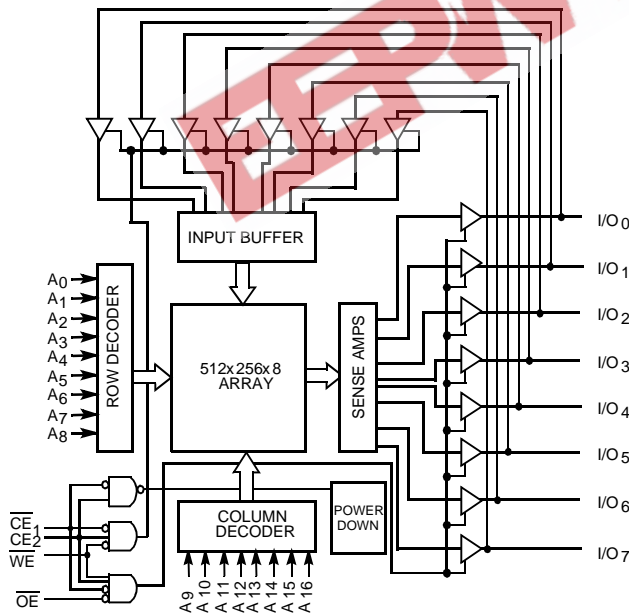
Reading from the device is accomplished by taking Chip Enable 1 (CE₁) and Output Enable (OE) LOW while forcing Write Enable (WE) and Chip Enable 2 (CE₂) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (CE₁ HIGH or CE₂ LOW), the outputs are disabled (OE HIGH), or during a write operation (CE₁ LOW, CE₂ HIGH, and WE LOW).

The WCMA1008C1X is available in a standard 32-pin 450-mil-wide body width SOIC and 32-pin TSOP type I.

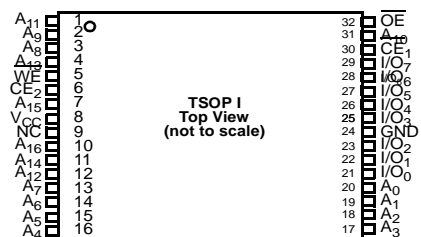
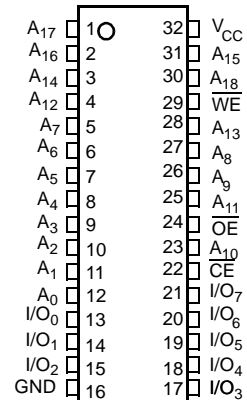
The WCMA1008C1X is available in a standard 32-pin 450-mil-wide body width SOIC and 32-pin TSOP type I.

Logic Block Diagram



Pin Configuration

Top View
SOIC





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V_{CC} to Relative GND -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} +0.5V
- DC Input Voltage^[1] -0.5V to V_{CC} +0.5V
- Current into Outputs (LOW) 20 mA
- Static Discharge Voltage..... 2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Product Portfolio

Product	V _{CC} Range			Speed	Temp.	Power Dissipation			
						Operating, I _{CC}		Standby (I _{SB2})	
	Min.	Typ. ^[2]	Max.			f = f _{max}		Typ. ^[2]	Max.
WCMA1008C1X	4.5 V	5.0V	5.5V	70 ns	Ind'l	Typ. ^[2]	Max.		
				55 ns		6 mA	15 mA		
						7.5 mA	20 mA		

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	4.5V-5.5V

Notes:

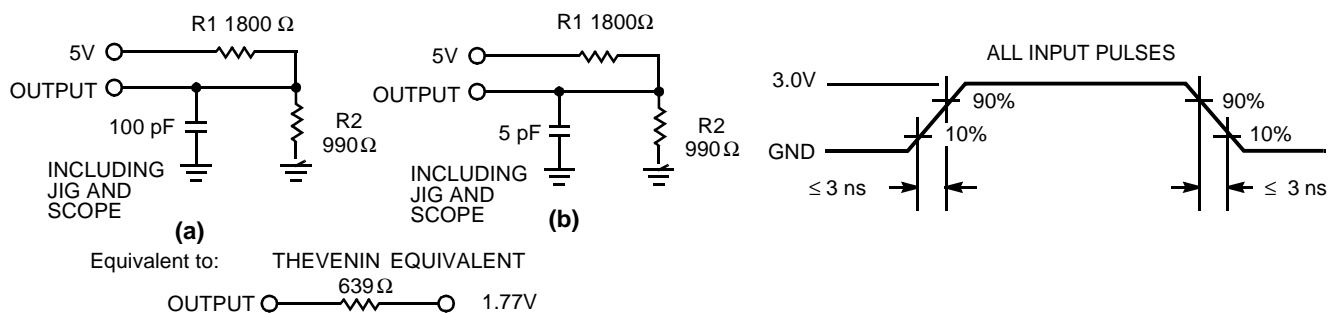
1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. Typical values are measured at V_{CC} = 5V, T_A = 25°C, and are included for reference only and are not tested or guaranteed.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCMA1008C1X-55			WCMA1008C1X-70			Units
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1 mA	2.4			2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3	2.2		V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} , I _{OUT} = 0 mA, V _{CC} = Max.,		7.5	20		6	15	mA
I _{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} , CE ₂ < V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		0.1	2		0.1	1	mA
I _{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, CE ₂ < 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		2.5	15			15	μA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	9	pF
C _{OUT}	Output Capacitance		9	pF

AC Test Loads and Waveforms

Note:

3. Tested initially and after any design or process changes that may affect these parameters.



Switching Characteristics^[4] Over the Operating Range

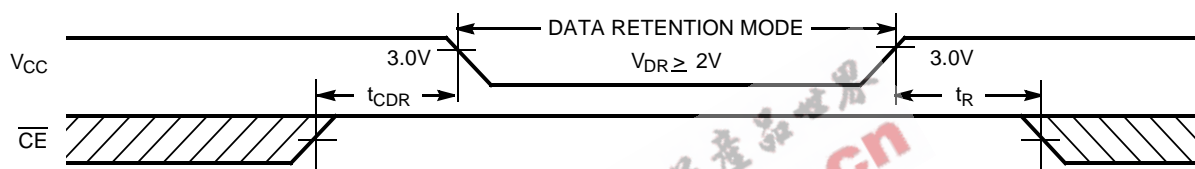
Parameter	Description	55		70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	\overline{CE}_1 LOW to Data Valid, CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		20		35	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[5]	0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[5, 6]		20		25	ns
t _{LZCE}	\overline{CE}_1 LOW to Low Z, CE ₂ HIGH to Low Z ^[5]	5		5		ns
t _{HZCE}	\overline{CE}_1 HIGH to High Z, CE ₂ LOW to High Z ^[5, 6]		20		25	ns
t _{PU}	\overline{CE}_1 LOW to Power-Up, CE ₂ HIGH to Power-Up	0		0		ns
t _{PD}	\overline{CE}_1 HIGH to Power-Down, CE ₂ LOW to Power-Down		55		70	ns
WRITE CYCLE^[7]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	\overline{CE}_1 LOW to Write End, CE ₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	45		50		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[5, 6]	5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6]		20		25	ns

Notes:

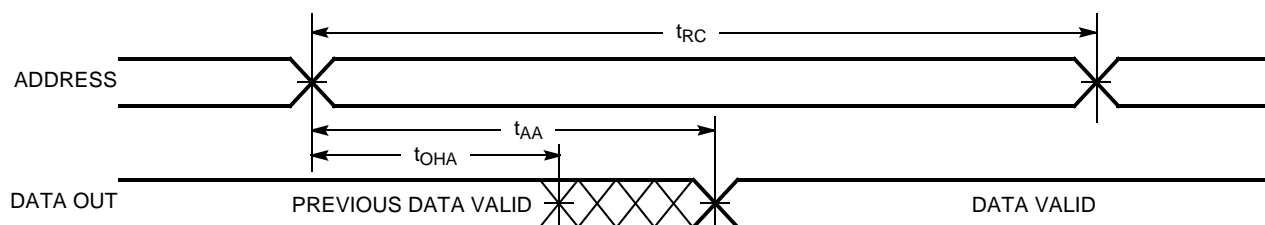
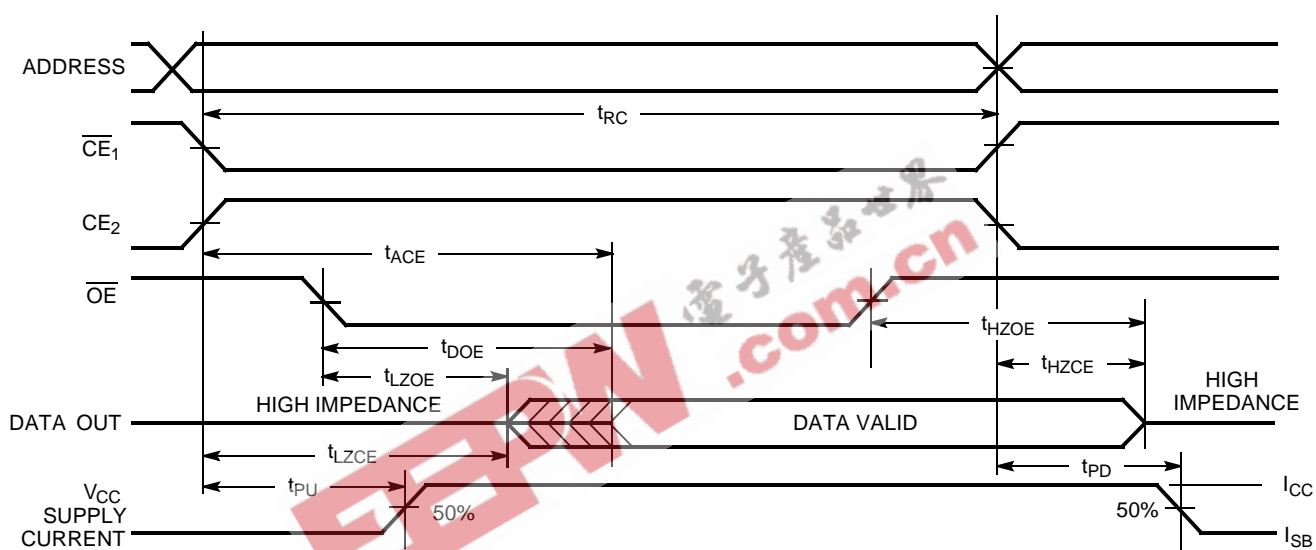
4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW and CE₂ HIGH, and \overline{WE} LOW. CE₁ and \overline{WE} must be LOW and CE₂ HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics (Over the Operating Range)

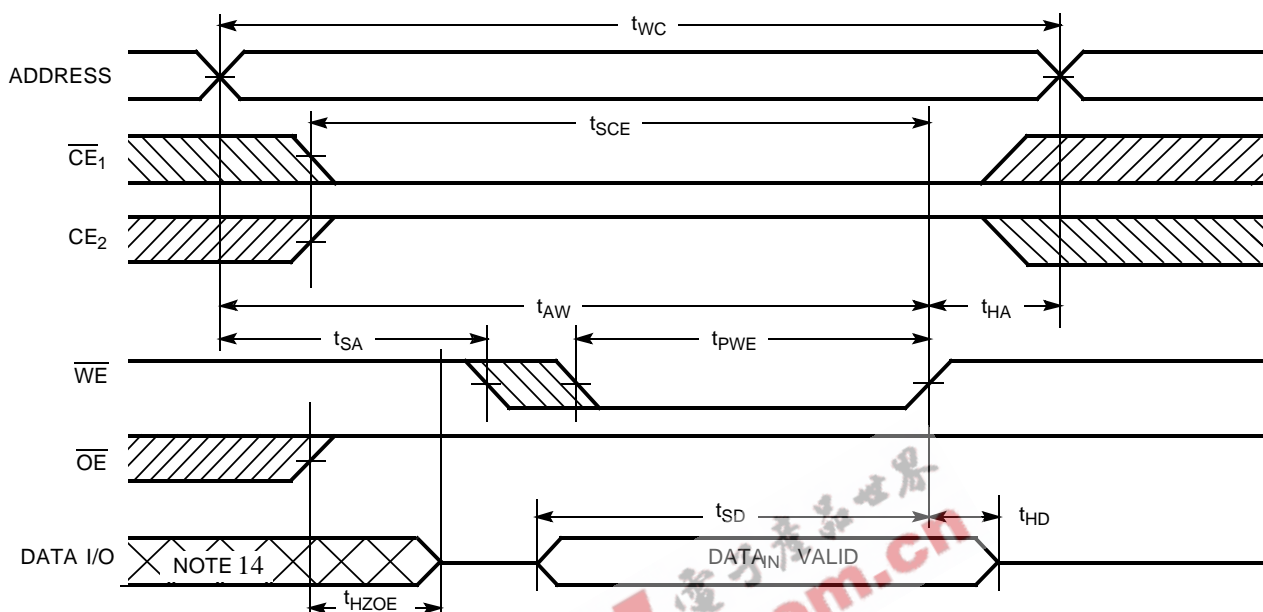
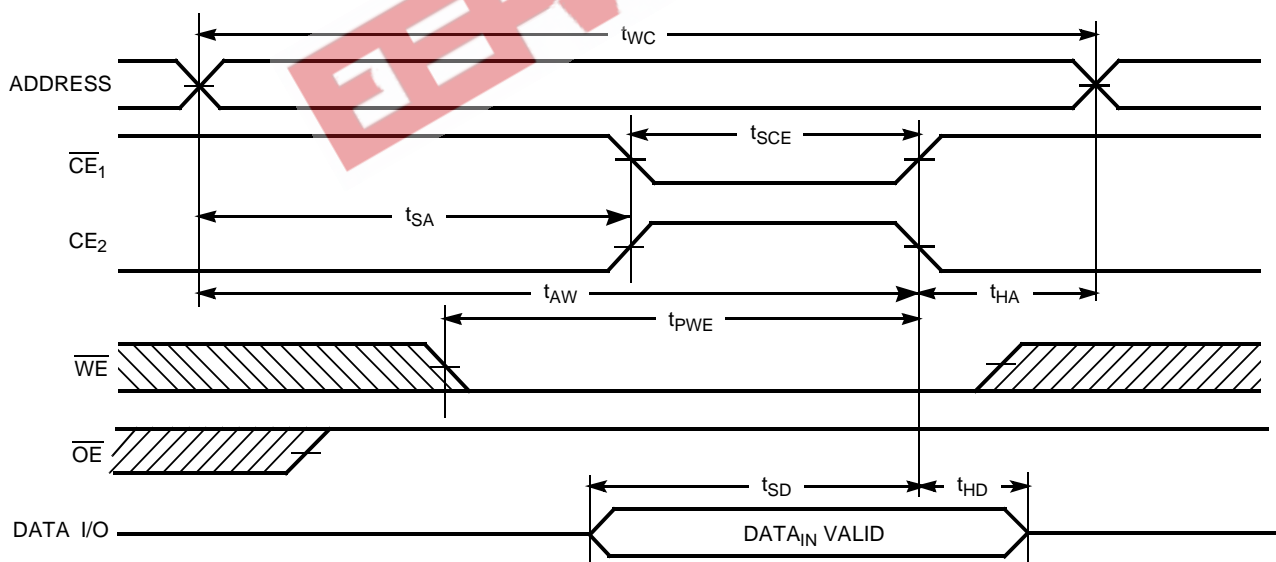
Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0			V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 3.0V$, $CE_1 \geq V_{CC} - 0.3V$, $CE_2 < 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or, $V_{IN} \leq 0.3V$		1.5	20	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		70			ns

Data Retention Waveform


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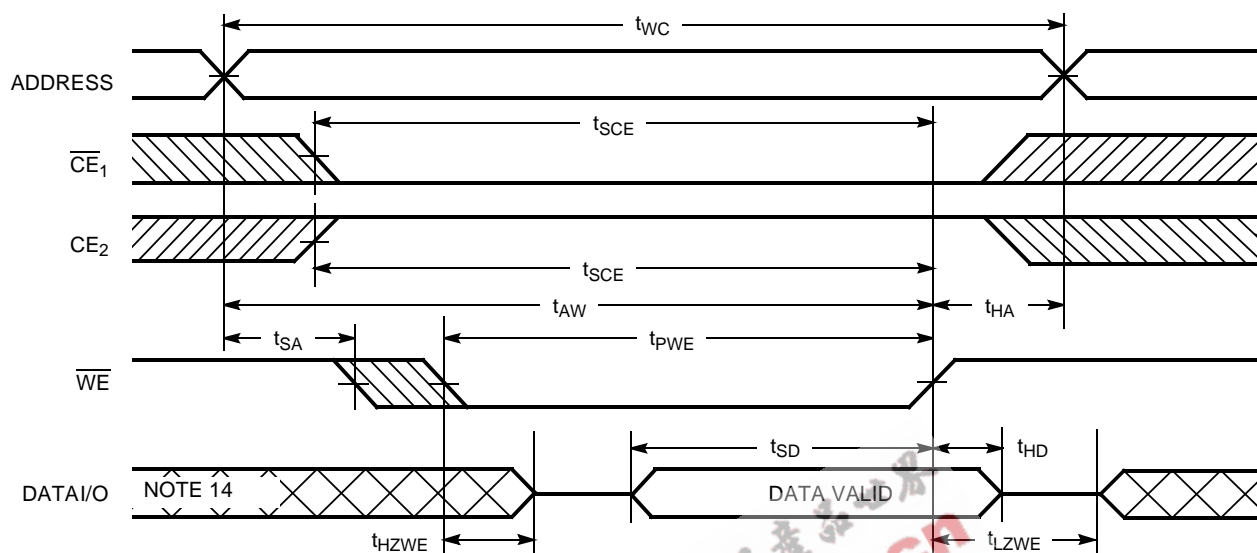
Switching Waveforms
Read Cycle No.1^[9, 10]

Read Cycle No. 2 (\overline{OE} Controlled)^[10, 11]

Notes:

8. Full Device operatin requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu s$ or stable at $V_{CC(min)} \geq 100 \mu s$.
9. Device is continuously selected. \overline{OE} , $CE_1 = V_{IL}$, $CE_2 = V_{IH}$
10. \overline{WE} is HIGH for read cycle.
11. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled)^[7, 12, 13]

Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled)^[7, 12, 13]

Notes:

12. If \overline{CE}_1 goes HIGH and CE_2 LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
13. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No.3 (\overline{WE} Controlled, \overline{OE} LOW)^[12]

Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O ₀ - I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I _{SB})
X	L	X	X	High Z	Power-Down	Standby (I _{SB})
L	H	L	H	Data Out	Read	Active (I _{CC})
L	H	X	L	Data In	Write	Active (I _{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

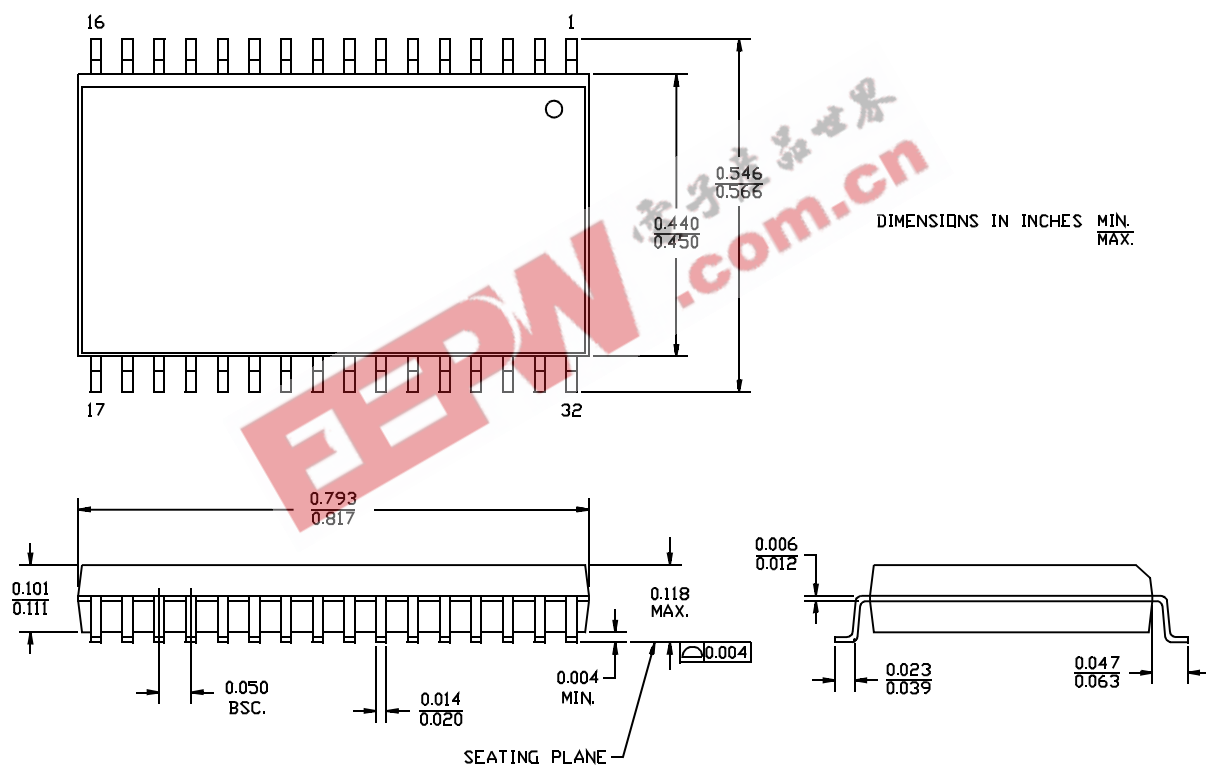


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA1008C1X-GF70	G32	32-Lead (450-Mil) Molded SOIC	Industrial
	WCMA1008C1X-TF70	T32	32-Lead TSOP	
55	WCMA1008C1X-GF55	G32	32-Lead (450-Mil) Molded SOIC	
	WCMA1008C1X-TF55	T32	32-Lead TSOP	

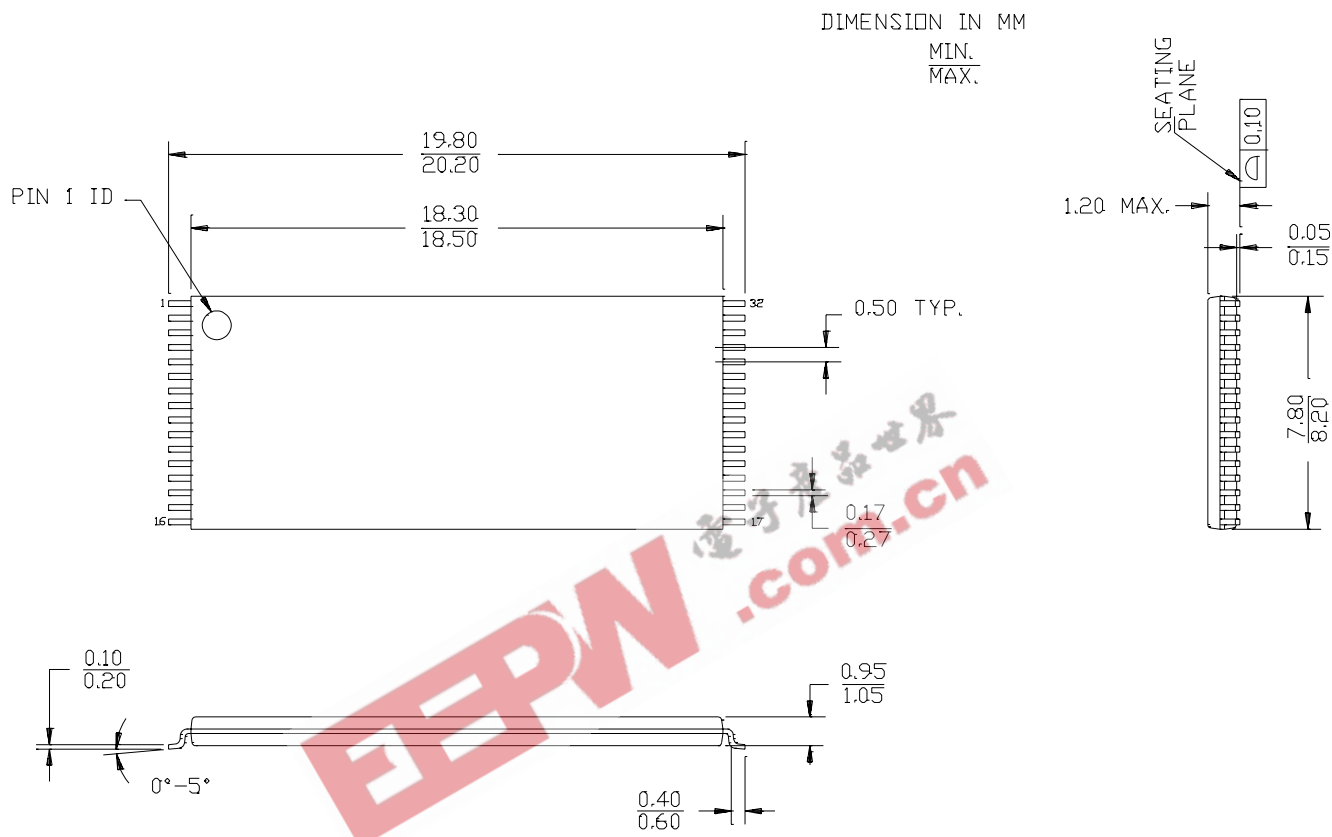
Package Diagrams

32-Lead (450 MIL) Molded SOIC, G32



Package Diagrams (continued)

32-Lead Thin Small Outline Package T32





Document Title: WCMA1008C1X, 128K x 8 Static RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-14022	115241	4/24/2002	MGN	New Datasheet

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