



Preliminary W24L11

128K × 8 CMOS STATIC RAM

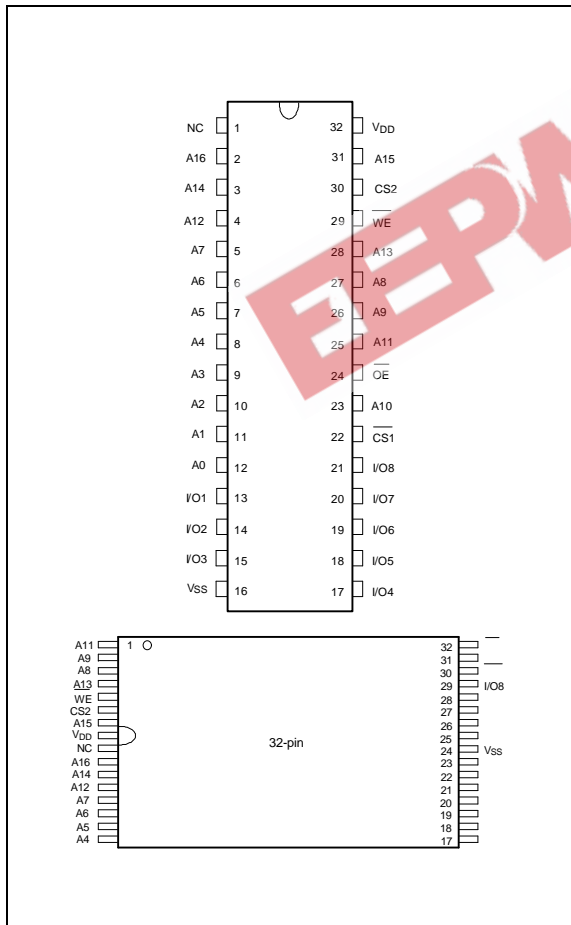
GENERAL DESCRIPTION

The W24L11 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a wide voltage range from 3.0V to 3.6V power supply. This device is manufactured using Winbond's high performance CMOS technology.

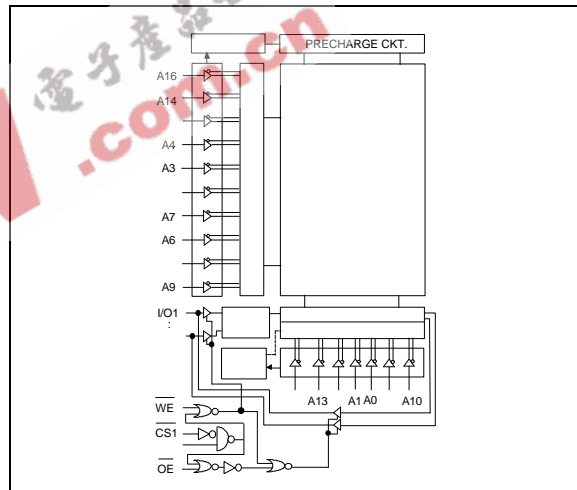
FEATURES

- Low power consumption:
 - Active: 144 mW (max.)
- Access time: 70 nS
- Single 3.3V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 600 mil DIP, 450 mil SOP, standard type one, TSOP (8 mm × 20 mm) , small type one and TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
V _{DD}	Power Supply
V _{SS}	Ground
NC	No Connection

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TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1 - I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to VSS Potential	-0.5 to +4.6	V
Input/Output to VSS Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to 70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VDD = 3.0V to 3.6V; VSS = 0V; TA (°C) = 0 to 70)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	MAX.	UNIT
Input Low Voltage	VIL	-	-0.5	+0.6	V
Input High Voltage	VIH	-	+2.0	VDD +0.5	V
Input Leakage Current	ILI	VIN = VSS to VDD	-1	+1	μA
Output Leakage Current	ILO	VI/O = VSS to VDD, CS1 = VIH (min.) or CS2 = VIL (max.) or OE = VIH (min.) or WE = VIL (max.)	-1	+1	μA
Output Low Voltage	VOL	IOL = +2.1 mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.0 mA	2.2	-	V
Operating Power Supply Current	IDD	CS1 = VIL (max.) and CS2 = VIH (min.), I/O = 0 mA, Cycle = min. Duty = 100%	-	40	mA

Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	MAX.	UNIT
Standby Power Supply Current	ISB	$\overline{CS1} = V_{IH} \text{ (min.) or}$ $CS2 = V_{IL} \text{ (max.)}$ Cycle = min. Duty = 100%	-	1	mA
		$\overline{CS1} \geq V_{DD} - 0.2V \text{ or}$ $CS2 \leq 0.2V$	LL	-	50
	L		-	100	

Note: Typical parameter is measured under ambient temperature $T_A = 25^\circ C$ and $V_{DD} = 3.3V$

CAPACITANCE

($V_{DD} = 3.3 V$, $T_A = 25^\circ C$, $f = 1 \text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	CI/O	$V_{OUT} = 0V$	8	pF

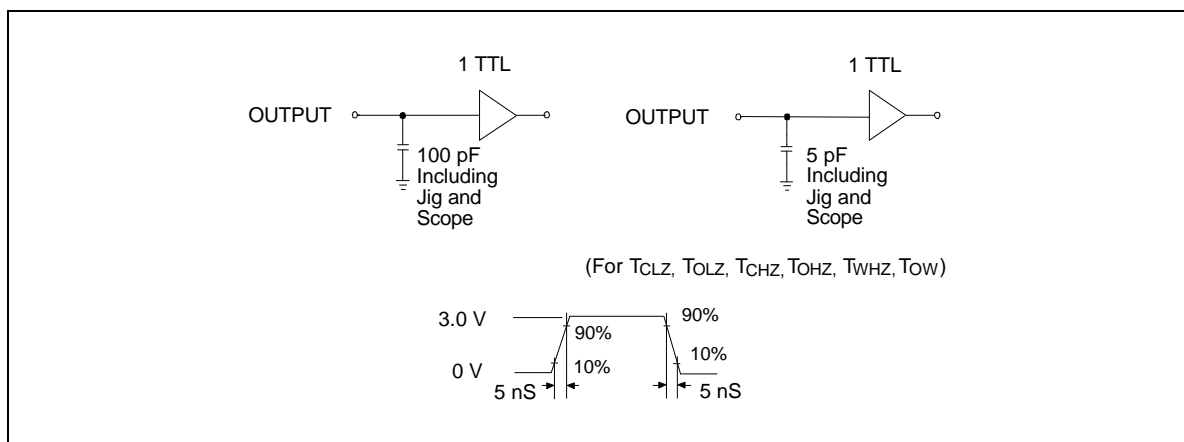
Note: These parameters are sampled but not 100% tested.

AC characteristics

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



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AC Characteristics, continued

(V_{DD} = 3.0V to 3.6 V; V_{SS} = 0V; T_A (°C) = 0 to 70)

Read Cycle

PARAMETER	SYMBOL	W24L11-70L/LL		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	70	-	nS
Address Access Time	TAA	-	70	nS
Chip Select Access Time	TACS	-	70	nS
Output Enable to Output Valid	TAOE	-	35	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	30	nS
Output Hold from Address Change	TOH	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

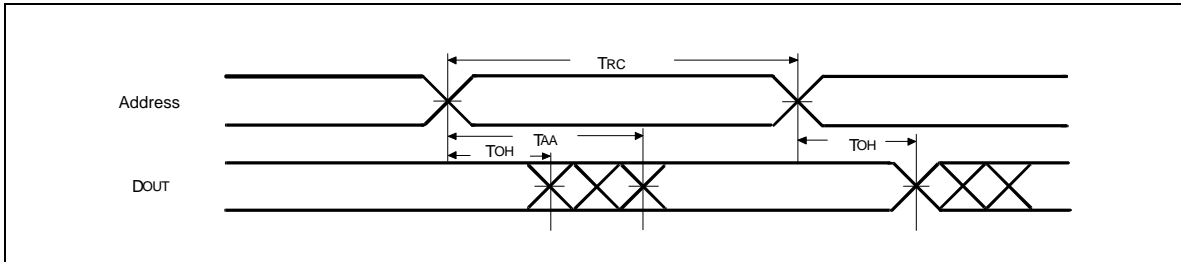
PARAMETER	SYMBOL	W24L11-70L/LL		UNIT
		MIN.	MAX.	
Write Cycle Time	TWC	70	-	nS
Chip Selection to End of Write	TCW	55	-	nS
Address Valid to End of Write	TAW	55	-	nS
Address Setup Time	TAS	0	-	nS
Write Pulse Width	TWP	50	-	nS
Write Recovery Time	$\overline{CS1}, CS2, \overline{WE}$ TWR	0	-	nS
Data Valid to End of Write	TDW	45	-	nS
Data Hold from End of Write	TDH	0	-	nS
Write to Output in High Z	TWHZ*	-	25	nS
Output Disable to Output in High Z	TOHZ*	-	25	nS
Output Active from End of Write	TOW	5	-	nS

* These parameters are sampled but not 100% tested

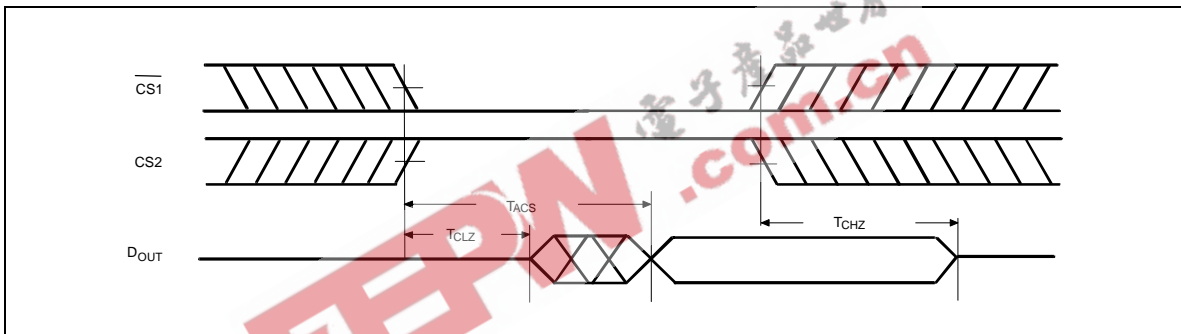


TIMING WAVEFORMS

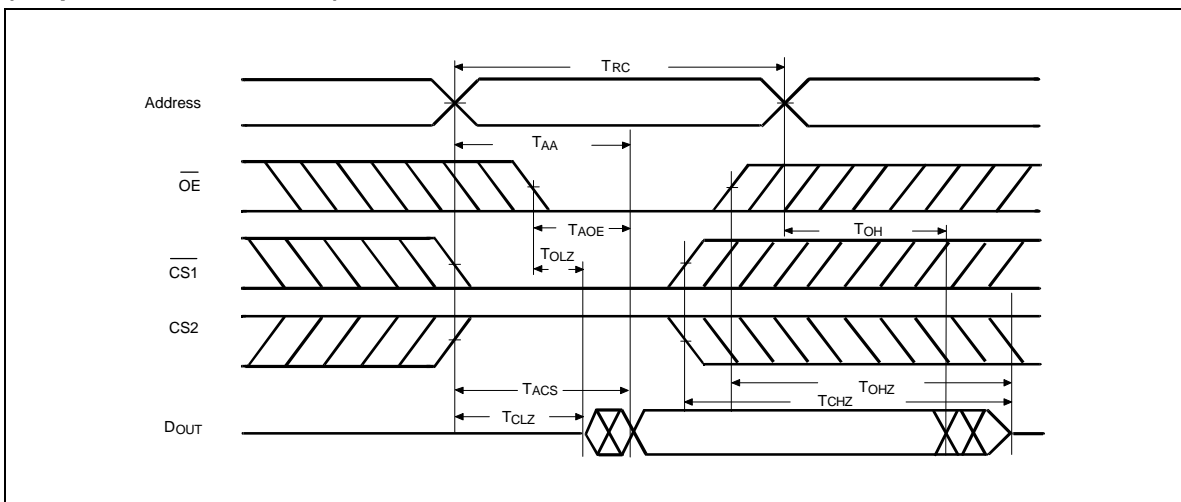
**Read Cycle 1
(Address Controlled)**



**Read Cycle 2
(Chip Select Controlled)**



**Read Cycle 3
(Output Enable Controlled)**

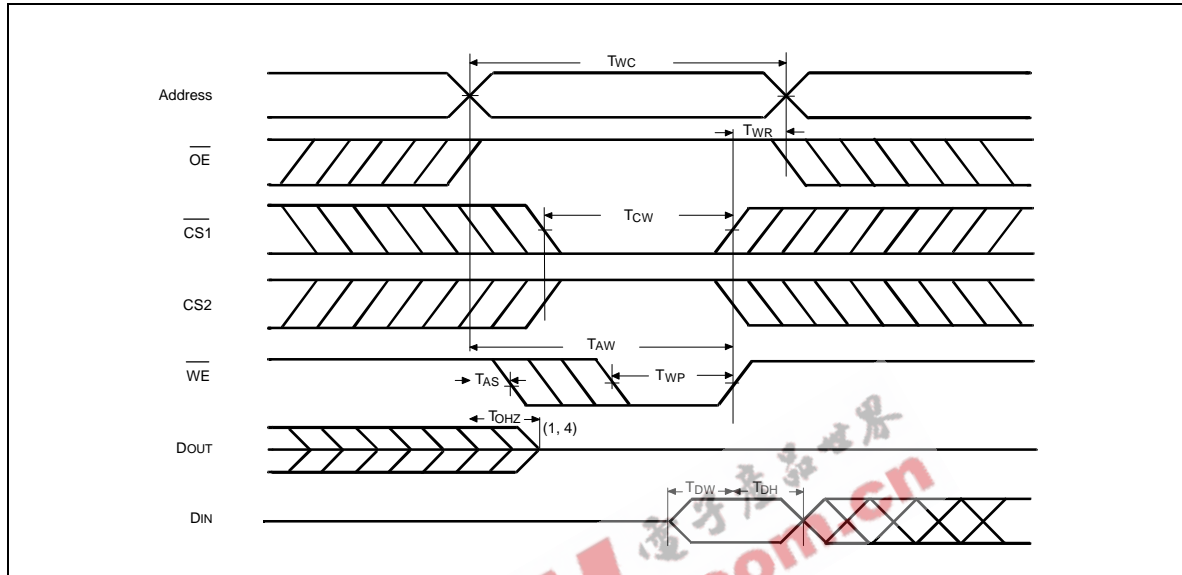


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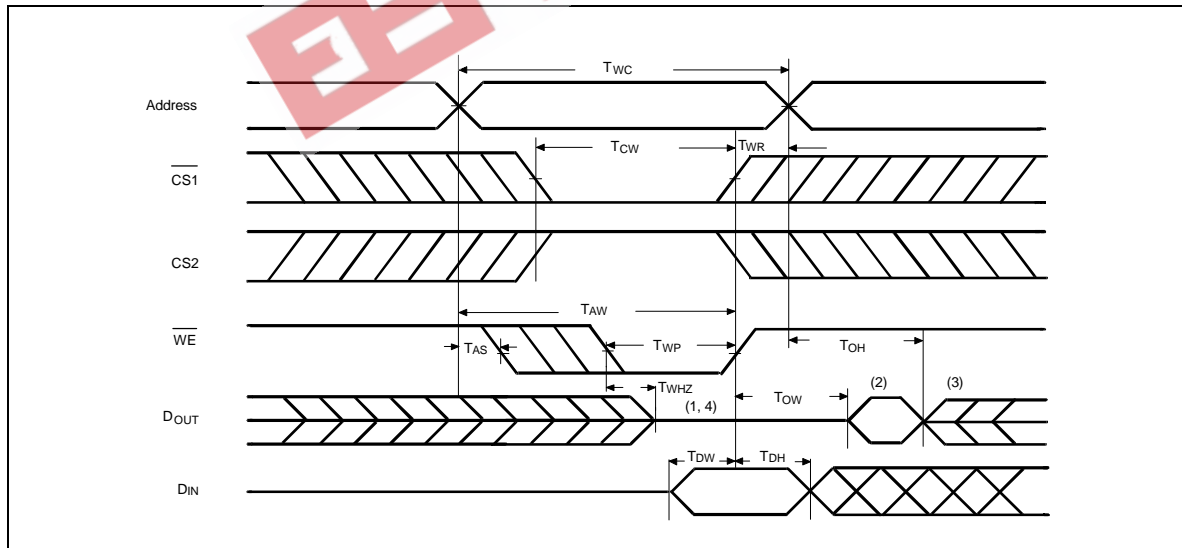
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.



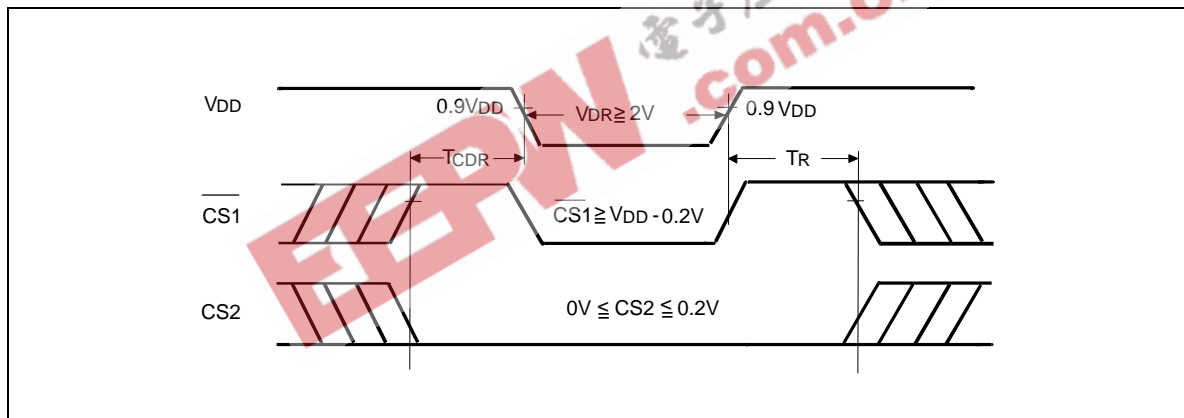
DATA RETENTION CHARACTERISTICS

(T_A (°C) = 0 to 70)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V, V_{DD} = 3V$	-	-	50	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		TRC*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



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ORDERING INFORMATION

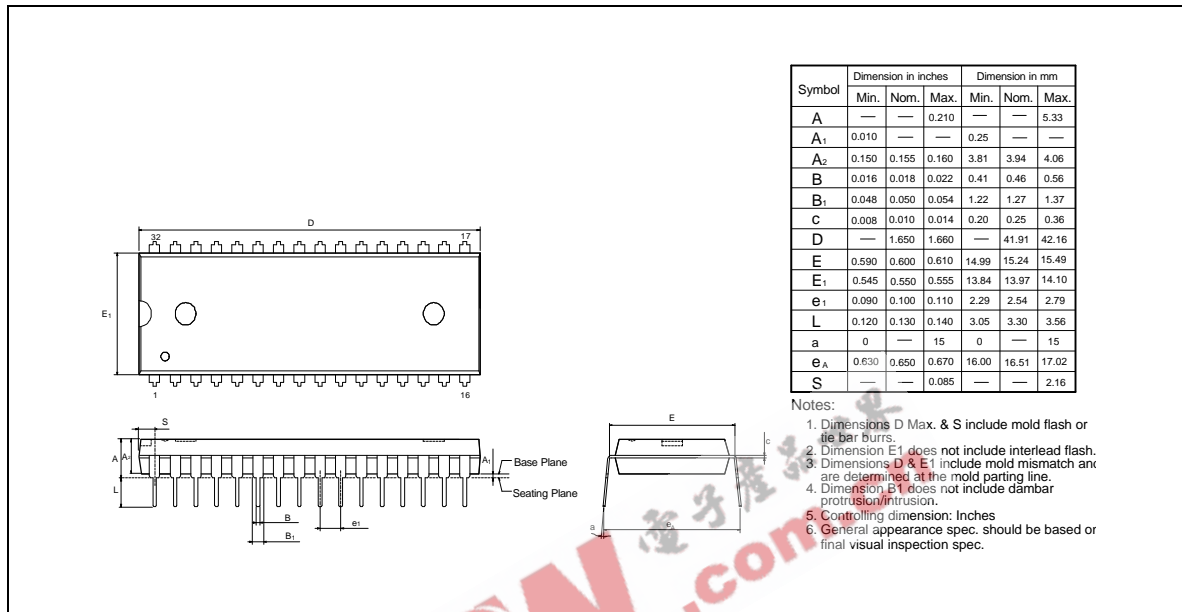
PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	STANDBY CURRENT MAX.(mA)	PACKAGE
W24L11-70LL	70	3.0V to 3.6V	0 to 70	50	600 mil DIP
W24L11S-70LL	70	3.0V to 3.6V	0 to 70	50	450 mil SOP
W24L11T-70LL	70	3.0V to 3.6V	0 to 70	50	Standard type one TSOP
W24L11Q-70LL	70	3.0V to 3.6V	0 to 70	50	Small type one TSOP
W24L11-70L	70	3.0V to 3.6V	0 to 70	100	600 mil DIP
W24L11S-70L	70	3.0V to 3.6V	0 to 70	100	450 mil SOP
W24L11T-70L	70	3.0V to 3.6V	0 to 70	100	Standard type one TSOP
W24L11Q-70L	70	3.0V to 3.6V	0 to 70	100	Small type one TSOP

Notes:

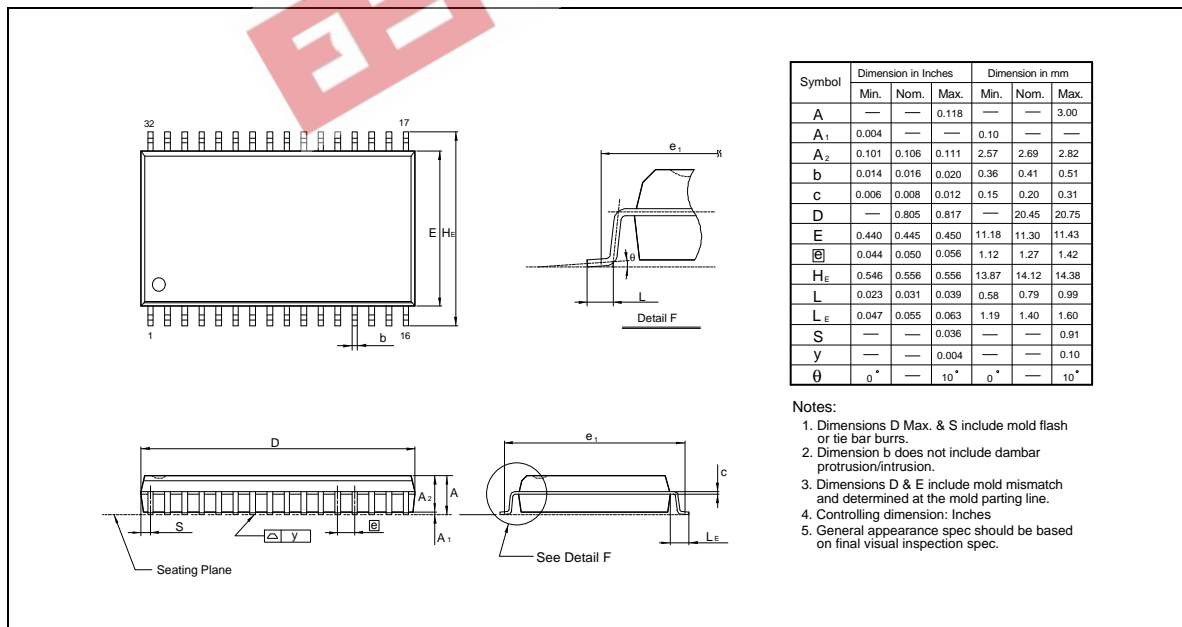
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin P-DIP

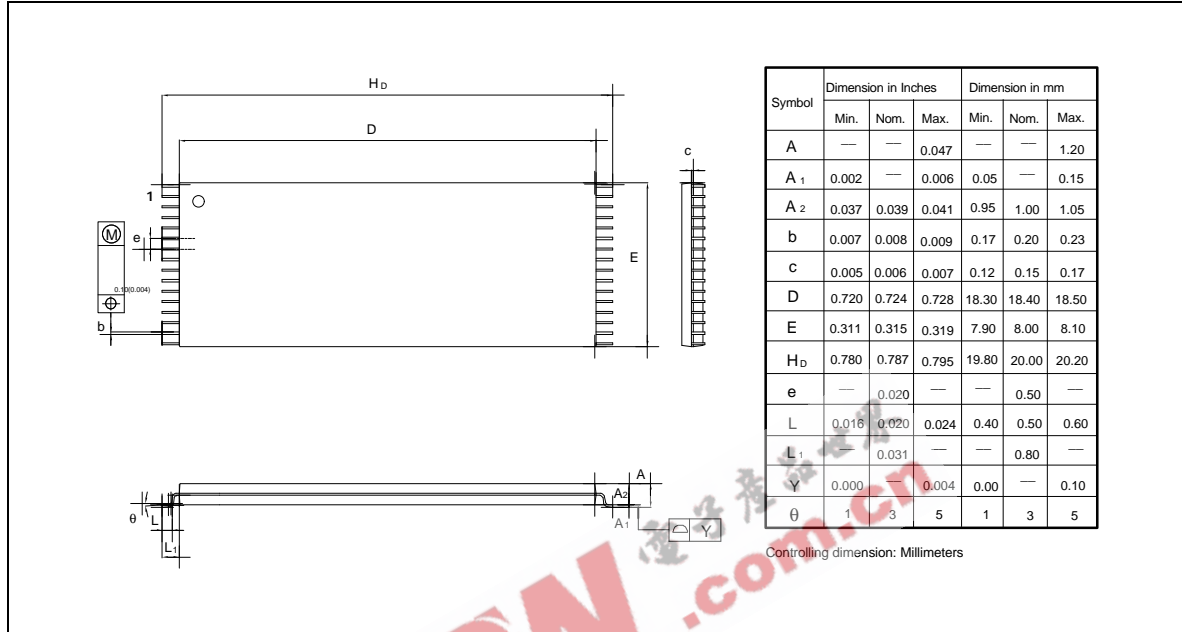


32-pin SOP Wide Body

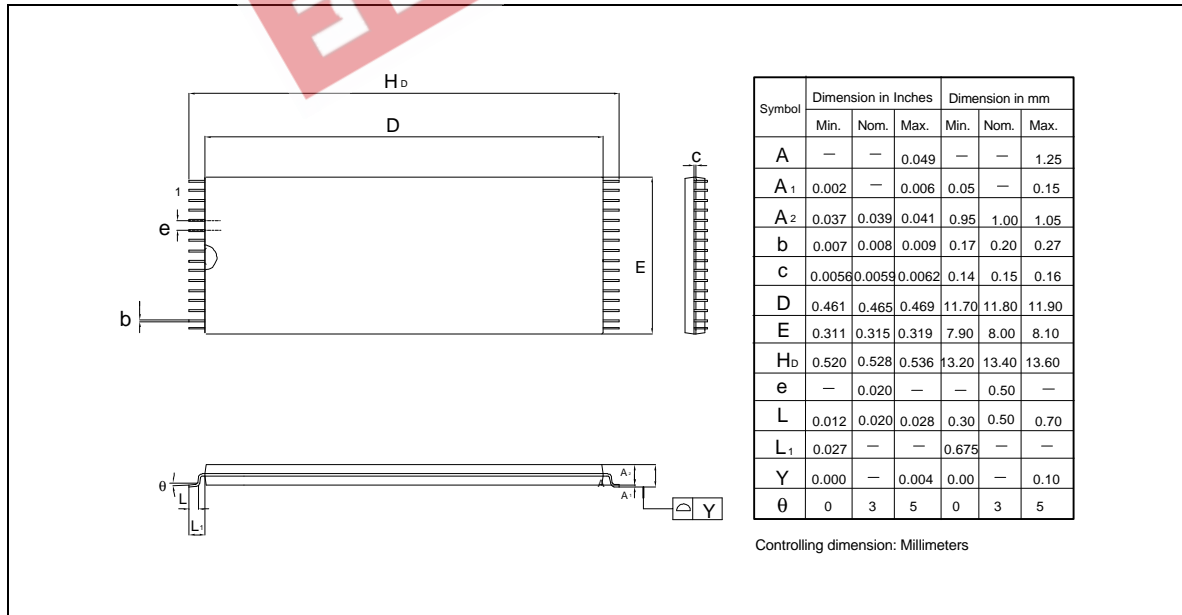


Package Dimensions, continued

32-pin Standard Type One TSOP



32-pin Small Type One TSOP



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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 1999	-	Initial Issued

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Note: All data and specifications are subject to change without notice.

Publication Release Date: October 1999