

W241024A



128K × 8 HIGH SPEED CMOS STATIC RAM

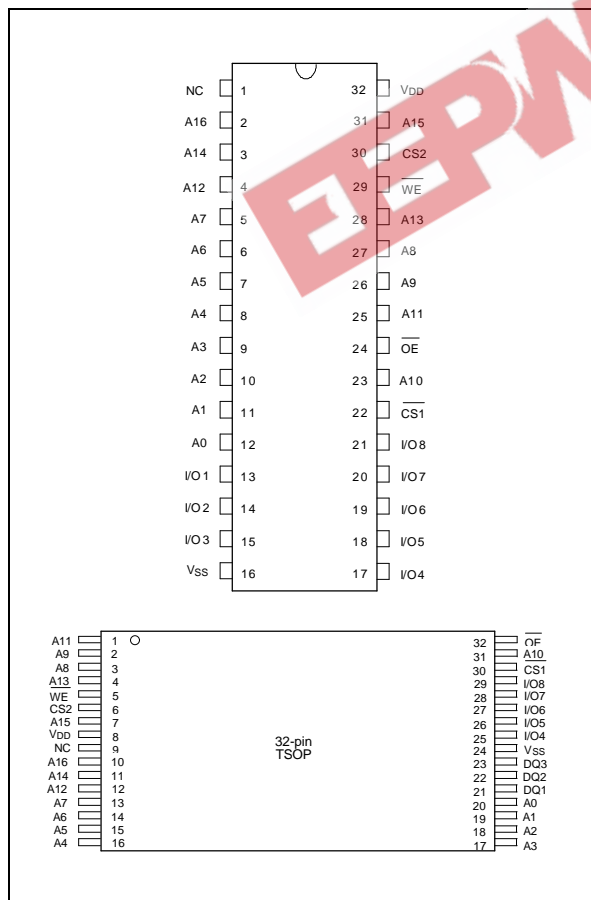
GENERAL DESCRIPTION

The W241024A is a high speed, low power CMOS static RAM organized as 131072 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

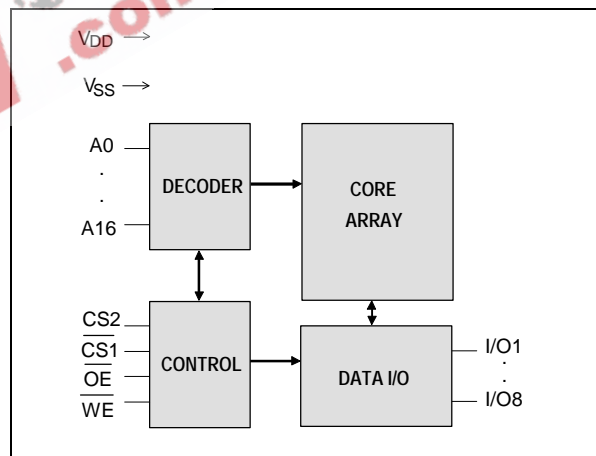
FEATURES

- High speed access time: 12/15/20 nS (max.)
- Low power consumption:
 - Active: 600 mW (typ.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 32-pin 300 mil SOJ, 400 mil SOJ, skinny DIP and standard type one TSOP (8 mm × 20 mm), and small type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection



TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1- I/O8	VDD CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to +7.0	V
Input/Output to Vss Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(VDD = 5V ±10%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Low Voltage	VIL	-	-0.5	-	+0.8	V	
Input High Voltage	VIH	-	+2.2	-	VDD +0.5	V	
Input Leakage Current	ILI	VIN = VSS to VDD	-10	-	+10	μA	
Output Leakage Current	ILO	VIO = VSS to VDD CS1 = VIH (min.) or CS2 = VIL (max.) or OE = VIH (min.) or WE = VIL (max.)	-10	-	+10	μA	
Output Low Voltage	VOL	IOL = +8.0 mA	-	-	0.4	V	
Output High Voltage	VOH	IOH = -4.0 mA	2.4	-	-	V	
Operating Power Supply Current	IDD	CS1 = VIL (max.), and CS2 = VIH (min.) I/O = 0 mA, Cycle = min. Duty = 100%	12	-	-	200	mA
			15	-	-	200	mA
			20	-	-	170	mA
Standby Power Supply Current	ISB	CS1 = VIH (min.), or CS2 = VIL (max.) Cycle = min.	-	-	30	mA	
	ISB1	CS1 ≥ VDD -0.2V or CS2 ≤ 0.2V	-	-	10	mA	

Note: Typical characteristics are at VDD = 5V, TA = 25° C.



CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	8	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	10	pF

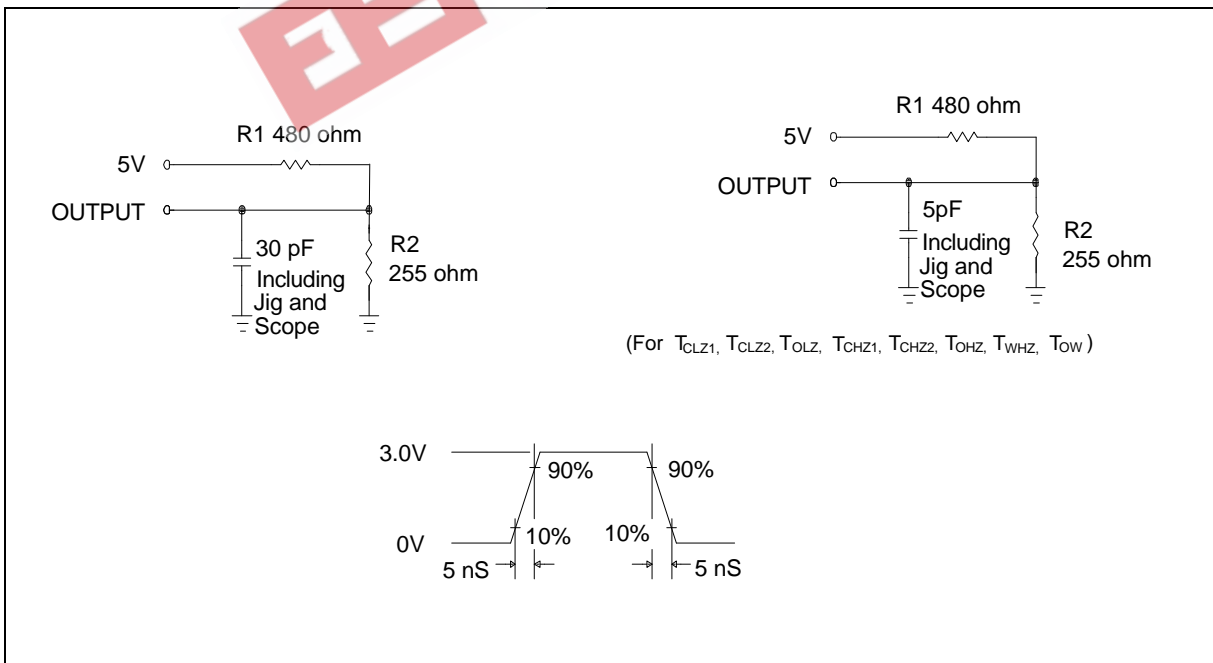
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 30 pF, I _{OH} /I _{OL} = -4 mA/8 mA

AC Test Loads and Waveform



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AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER		SYM.	W241024A-12		W241024A-15		W241024A-20		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time		TRC	12	-	15	-	20	-	nS
Address Access Time		TAA	-	12	-	15	-	20	nS
Chip Select Access Time	$\overline{\text{CS1}}$	TACS1	-	12	-	15	-	20	nS
	CS2	TACS2	-	12	-	15	-	20	nS
Output Enable to Output Valid		TAOE	-	6	-	7	-	10	nS
Chip Selection to Output in Low Z	$\overline{\text{CS1}}$	TCLZ1*	3	-	3	-	3	-	nS
	CS2	TCLZ2*	3	-	3	-	3	-	nS
Output Enable to Output in Low Z		TOLZ*	0	-	0	-	0	-	nS
Chip Deselection to Output in High Z	$\overline{\text{CS1}}$	TCHZ1*	-	6	-	7	-	10	nS
	CS2	TCHZ2*	-	6	-	7	-	10	nS
Output Disable to Output in High Z		TOHZ*	-	6	-	7	-	10	nS
Output Hold from Address Change		TOH	3	-	3	-	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

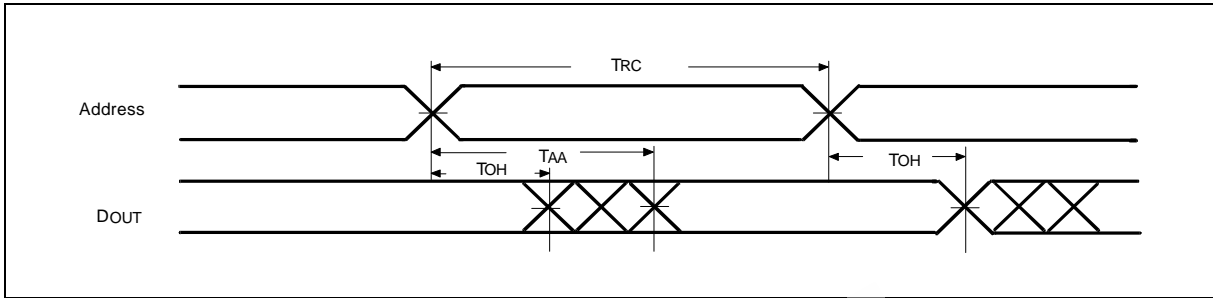
PARAMETER		SYM.	W241024A-12		W241024A-15		W241024A-20		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		TWC	12	-	15	-	20	-	nS
Chip Selection to End of Write	$\overline{\text{CS1}}$	TCW1	10	-	13	-	17	-	nS
	CS2	TCW2	10	-	13	-	17	-	nS
Address Valid to End of Write		TAW	10	-	13	-	17	-	nS
Address Setup Time		TAS	0	-	0	-	0	-	nS
Write Pulse Width		TWP	10	-	10	-	12	-	nS
Write Recovery Time	$\overline{\text{CS1}}, \overline{\text{WE}}$	TWR1	0	-	0	-	0	-	nS
	CS2	TWR2	0	-	0	-	0	-	nS
Data Valid to End of Write		TDW	7	-	9	-	10	-	nS
Data Hold from End of Write		TDH	0	-	0	-	0	-	nS
Write to Output in High Z		TWHZ*	-	7	-	8	-	10	nS
Output Disable to Output in High Z		TOHZ*	-	7	-	8	-	10	nS
Output Active from End of Write		TOW	0	-	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

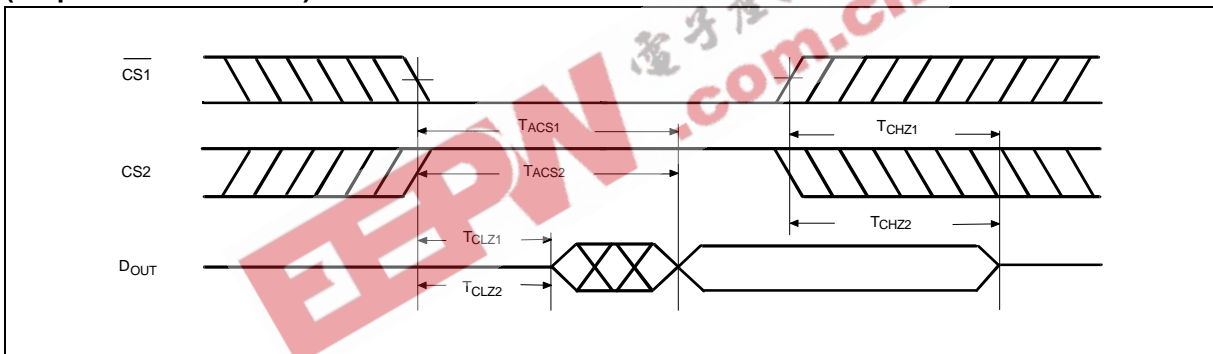


TIMING WAVEFORMS

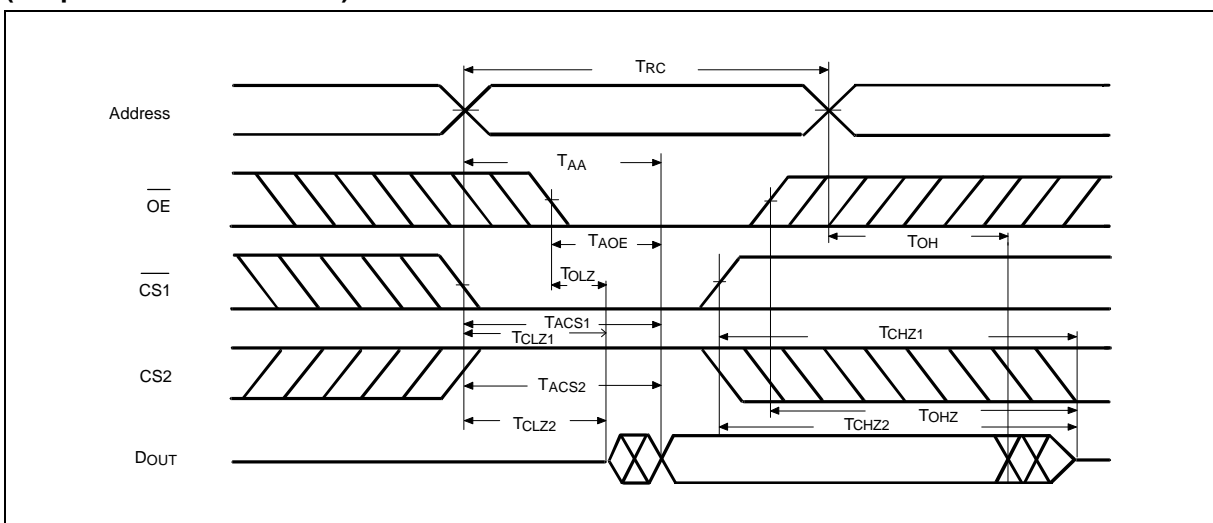
**Read Cycle 1
(Address Controlled)**



**Read Cycle 2
(Chip Select Controlled)**



**Read Cycle 3
(Output Enable Controlled)**

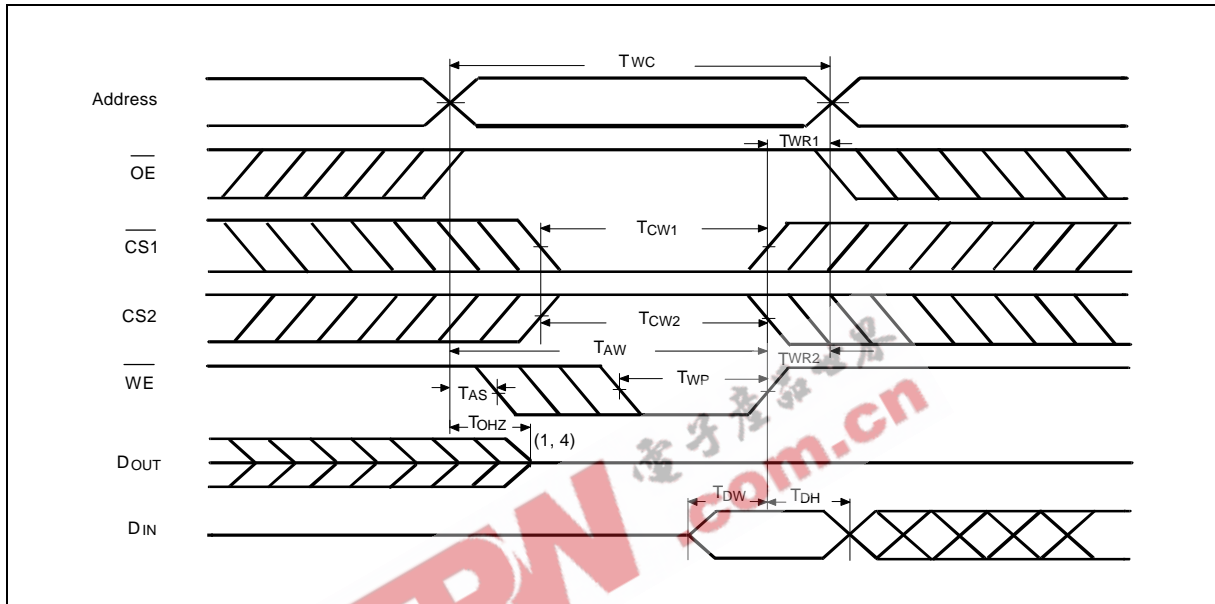




Timing Waveforms, continued

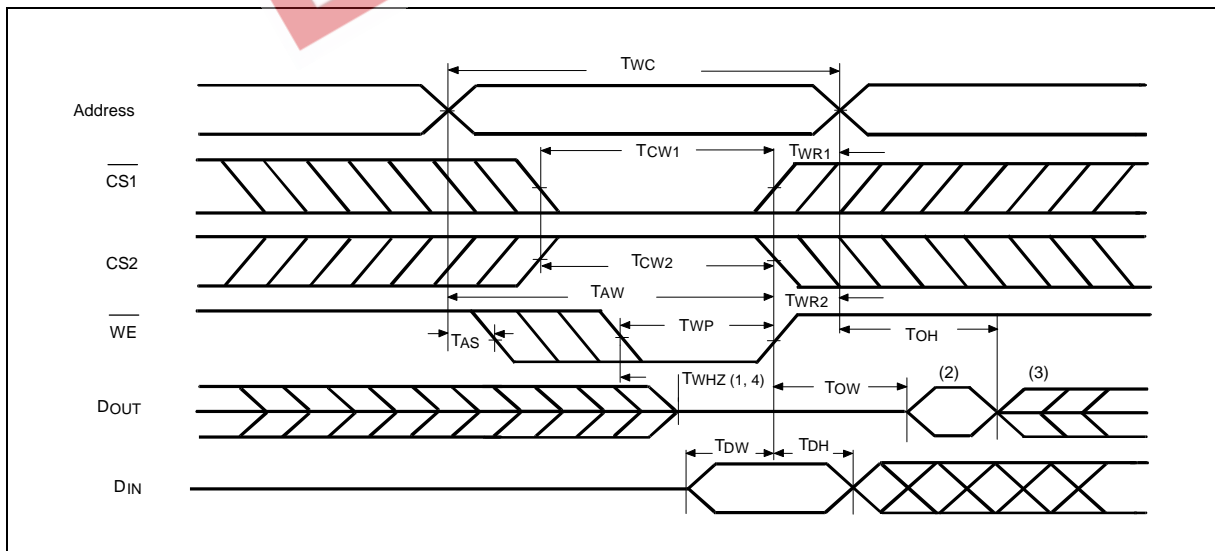
Write Cycle 1

($\overline{\text{OE}}$ Clock)



Write Cycle 2

($\overline{\text{OE}} = \text{VIL Fixed}$)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. Dout provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

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ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W241024AI-12	12	200	10	400 mil SOJ
W241024AI-15	15	200	10	400 mil SOJ
W241024AI-20	20	170	10	400 mil SOJ
W241024AJ-12	12	200	10	300 mil SOJ
W241024AJ-15	15	200	10	300 mil SOJ
W241024AJ-20	20	170	10	300 mil SOJ
W241024AK-12	12	200	10	300 mil skinny DIP
W241024AK-15	15	200	10	300 mil skinny DIP
W241024AK-20	20	170	10	300 mil skinny DIP
W241024AQ-12	12	200	10	Small type one TSOP
W241024AQ-15	15	200	10	Small type one TSOP
W241024AQ-20	20	170	10	Small type one TSOP
W241024AT-12	12	200	10	Standard type one TSOP
W241024AT-15	15	200	10	Standard type one TSOP
W241024AT-20	20	170	10	Standard type one TSOP

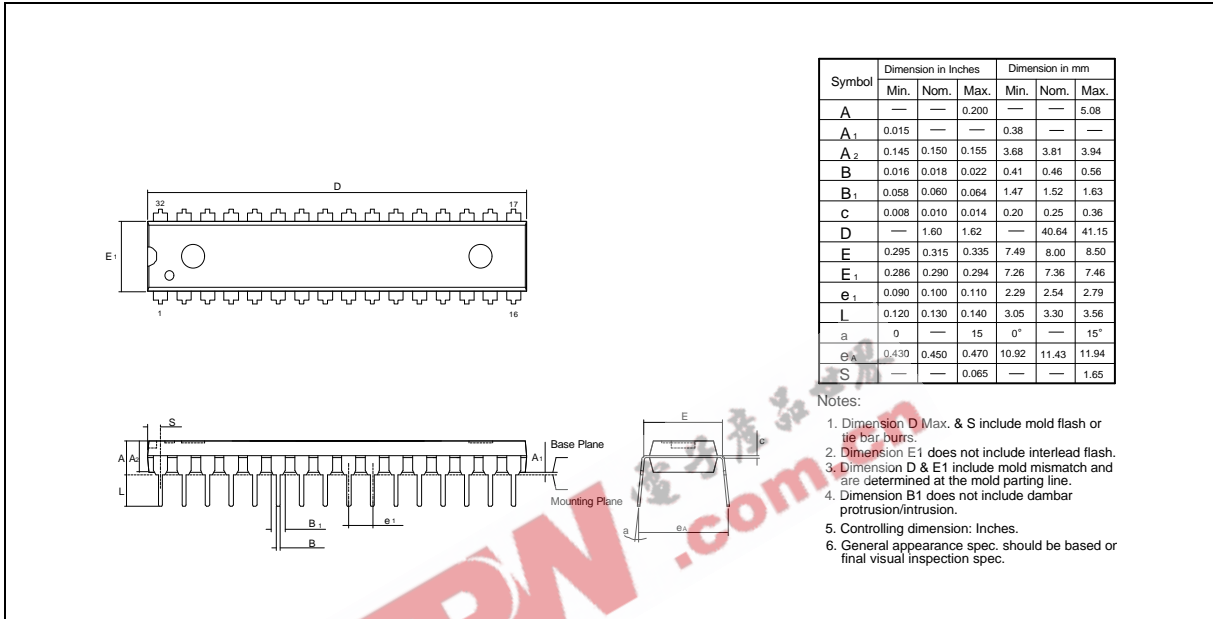
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

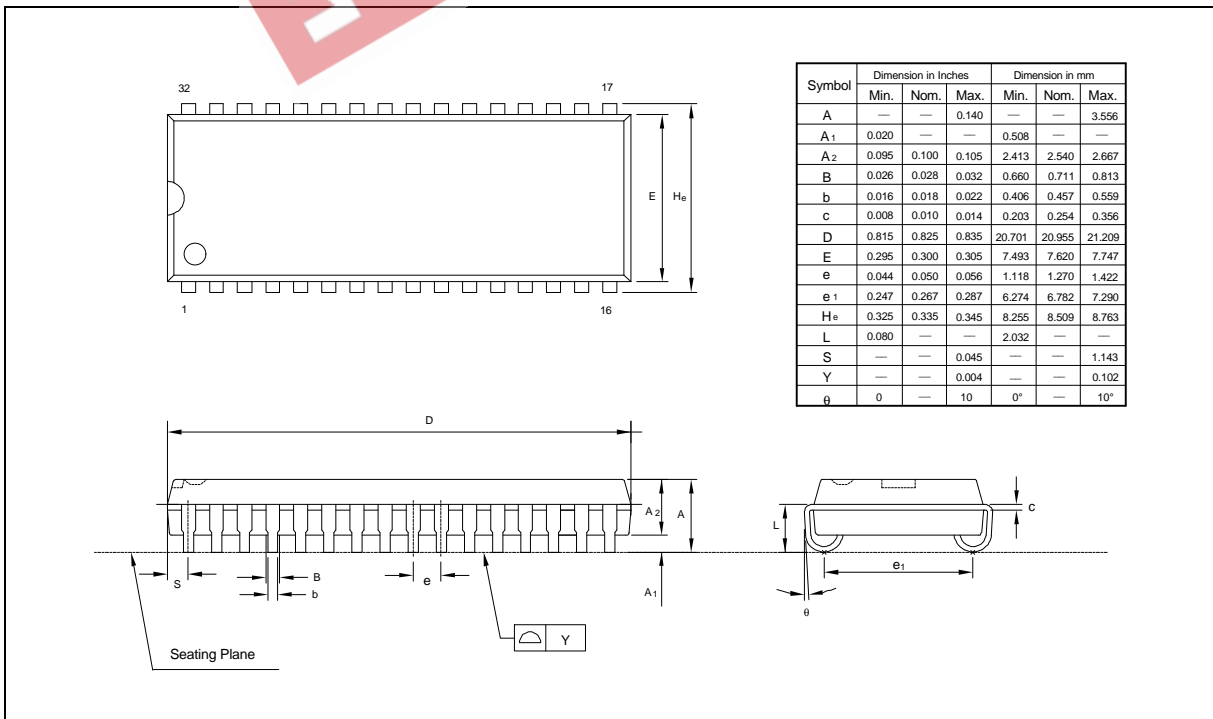


PACKAGE DIMENSIONS

32-pin P-DIP Skinny (300 mil)



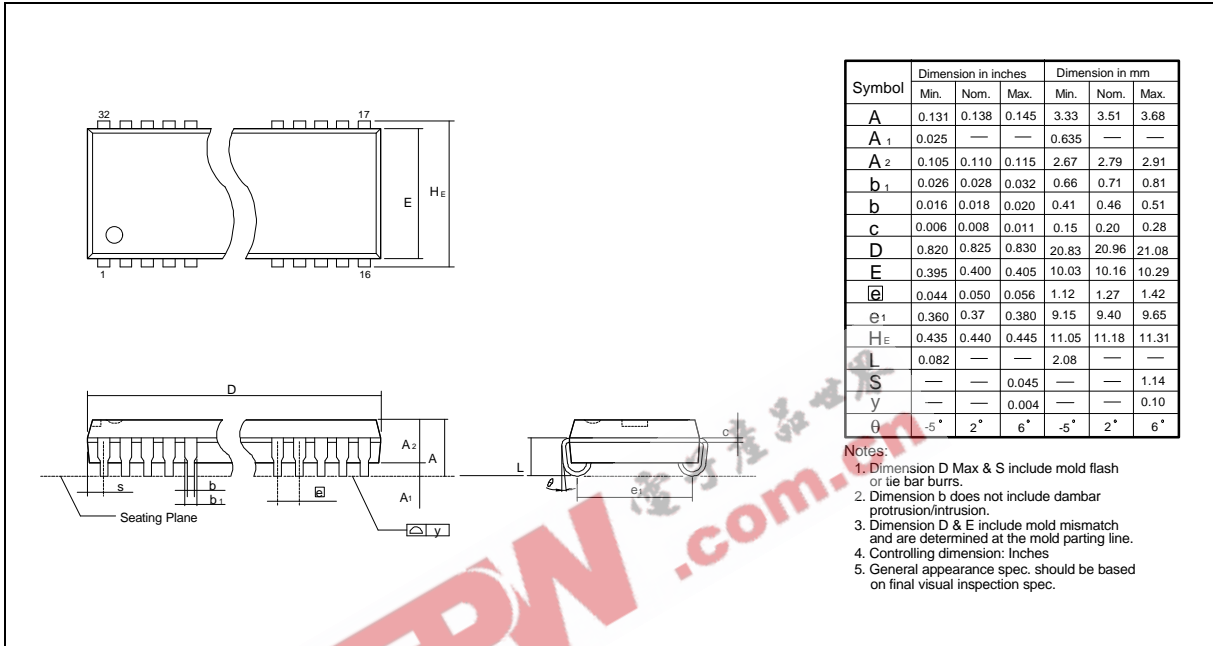
32-pin SOJ (300 mil)



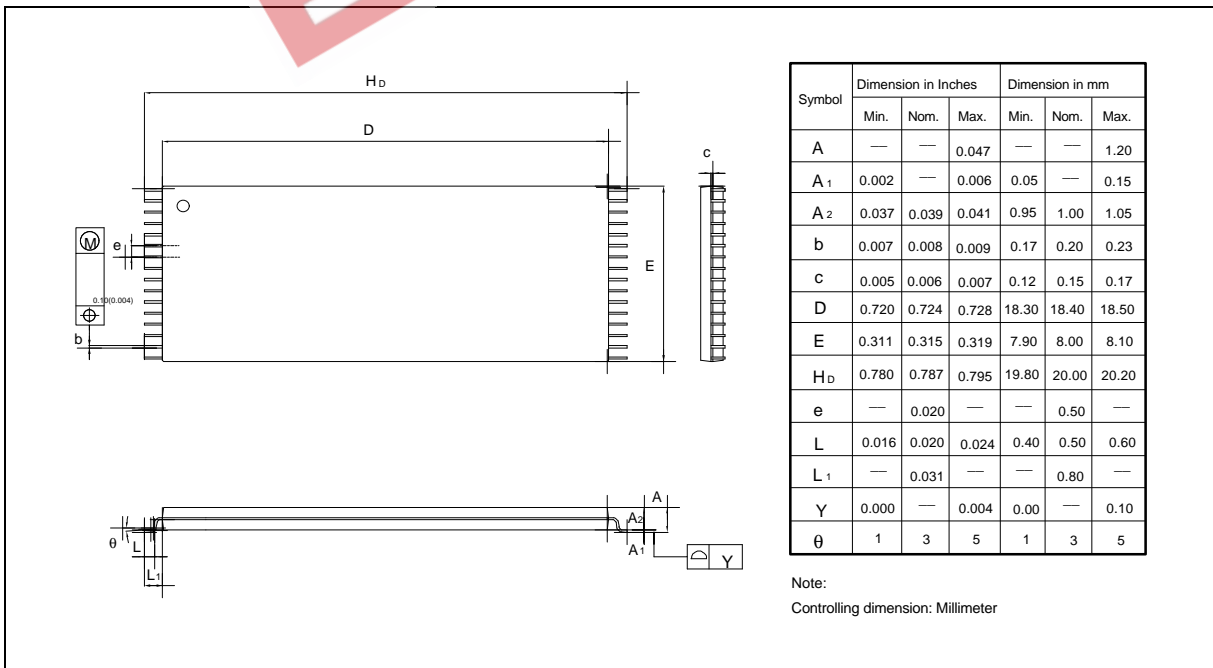


Package Dimensions, continued

32-pin SOJ (400 mil)



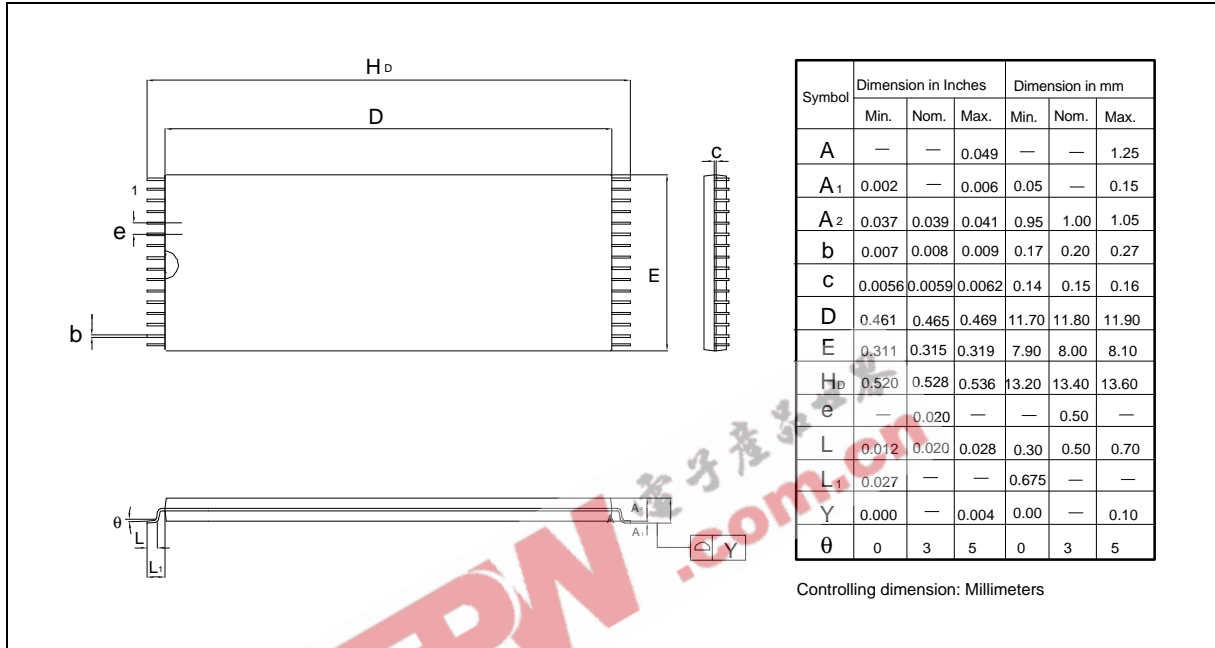
32-pin Standard Type One TSOP





Package Dimensions, continued

32-pin Small Type One TSOP





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A9	Jul. 1998	1, 7, 10	Add small type one TSOP (8 mm × 13.4 mm) package



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Note: All data and specifications are subject to change without notice.