



32K x 8 Static RAM

Features

- High speed
 - 12 ns
- Fast t_{DOE}
- CMOS for optimum speed/power
- Easy memory expansion with \overline{CE} and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

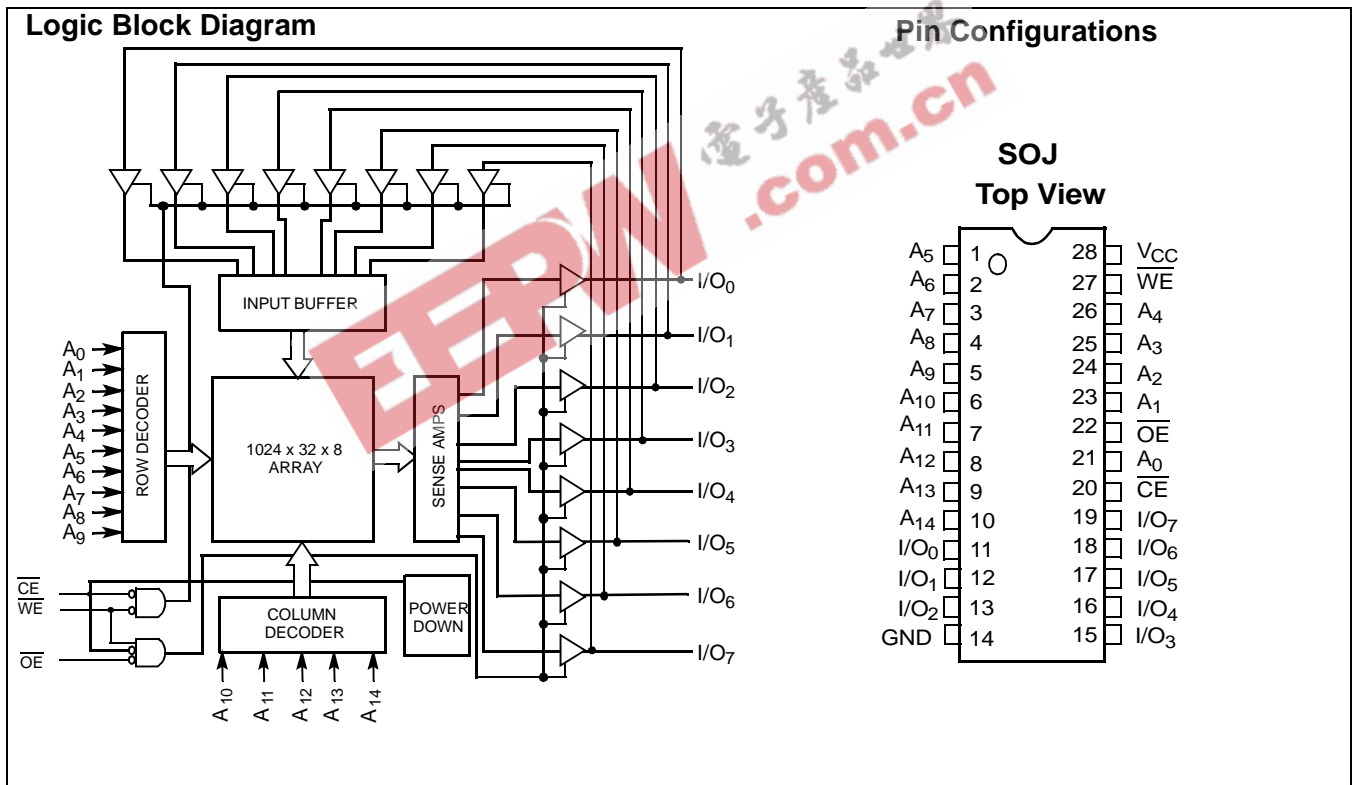
Functional Description

The WCFS0808C1E is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}) and active LOW Output Enable (\overline{OE}) and three-state drivers. This device has

an automatic power-down feature, reducing the power consumption by 81% when deselected. The WCFS0808C1E is in the standard SOJ package.

An active LOW Write Enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable (\overline{WE}) is HIGH. A die coat is used to improve alpha immunity.



Selection Guide

	WCFS0808C1E 12ns	WCFS0808C1E 15ns
Maximum Access Time (ns)	12	15
Maximum Operating Current (mA)	160	155
Maximum CMOS Standby Current (mA)	10	10



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14)	-0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

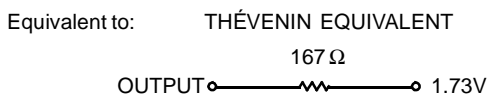
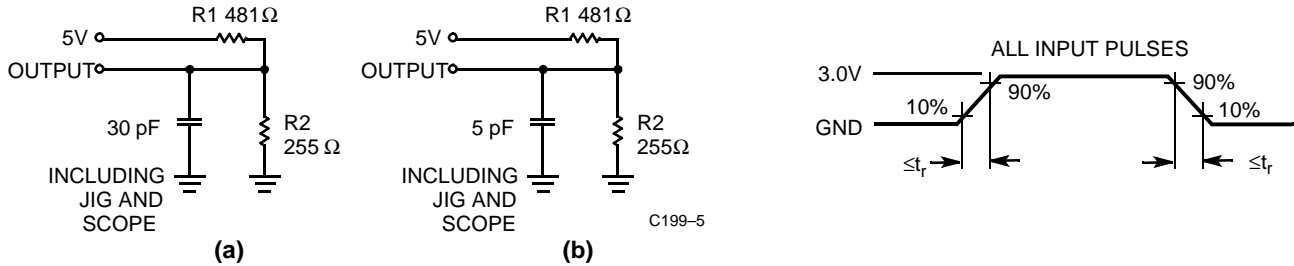
Parameter	Description	Test Conditions	WCFS0808C1E 12ns		WCFS0808C1E 15ns		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		160		155	mA
I _{SB1}	Automatic CE Power-Down Current— TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30	mA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0		10		10	mA

Capacitance^[1]

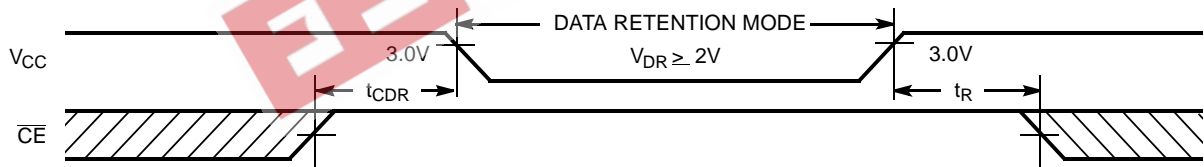
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	8	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	8	pF

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[5]

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[6]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
$t_{CDR}^{[1]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$,	0		ns
$t_R^{[5]}$	Operation Recovery Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	200		μs

Data Retention Waveform

Note:

5. $t_R \leq 3$ ns for the -12 and the -15 speeds. $t_R \leq 5$ ns for the -20 and slower speeds
6. No input may exceed $V_{CC} + 0.5V$.



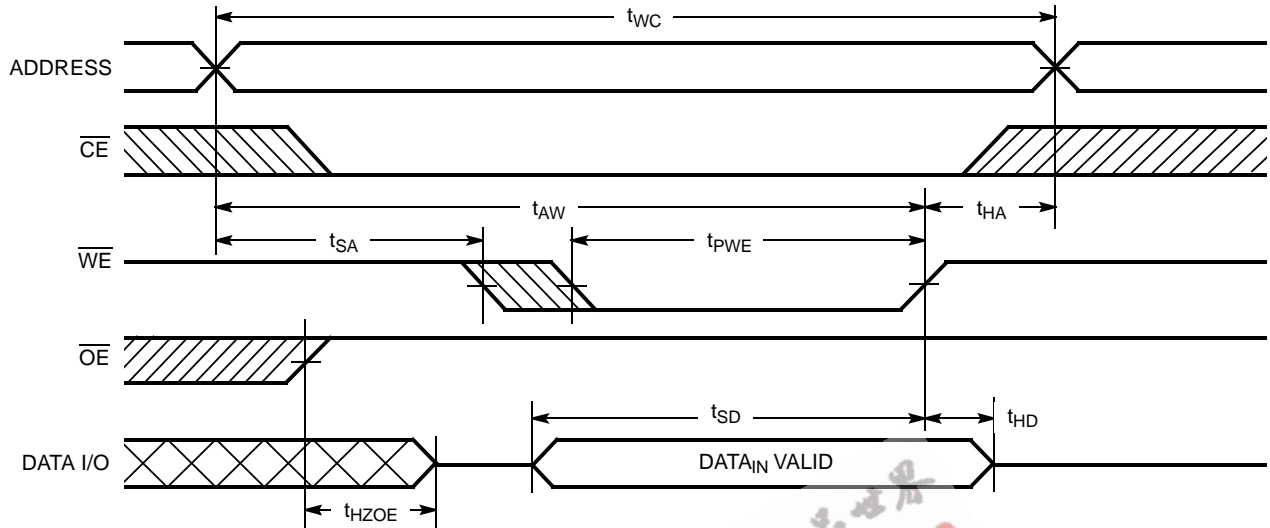
Switching Characteristics Over the Operating Range^[3, 7]

Parameter	Description	WCFS0808C1E 12ns		WCFS0808C1E 15ns		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	12		15		ns
t _{AA}	Address to Data Valid		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15	ns
t _{DOE}	\overline{OE} LOW to Data Valid		5		7	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[8]	0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[8, 9]		5		7	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[8]	3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[8, 9]		5		7	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15	ns
WRITE CYCLE ^[10, 11]						
t _{WC}	Write Cycle Time	12		15		ns
t _{SCE}	\overline{CE} LOW to Write End	9		10		ns
t _{AW}	Address Set-Up to Write End	9		10		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		9		ns
t _{SD}	Data Set-Up to Write End	8		9		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[9]		7		7	ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[8]	3		3		ns

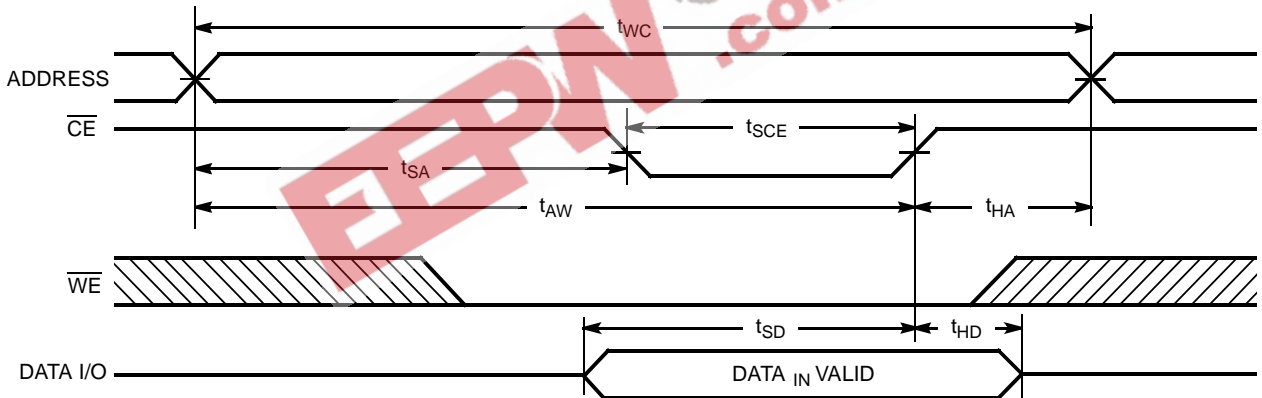
Notes:

7. Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Write Cycle No. 1 (WE Controlled)^[10, 15, 16]

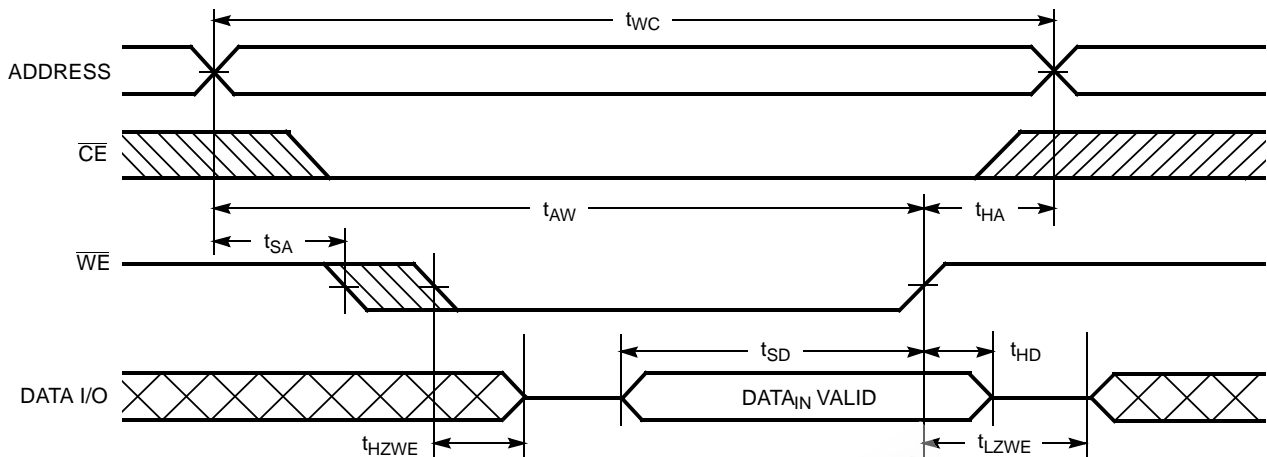
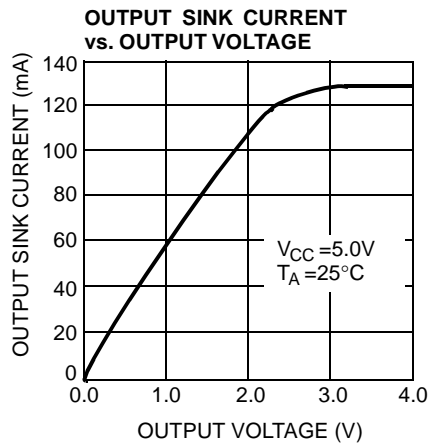
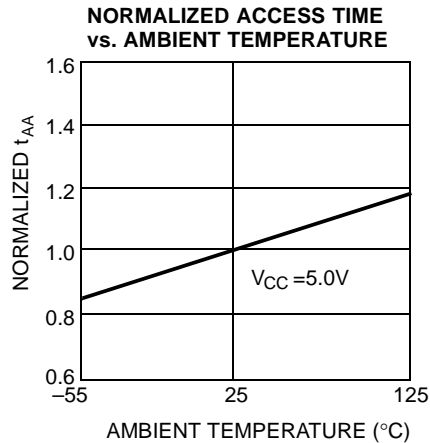
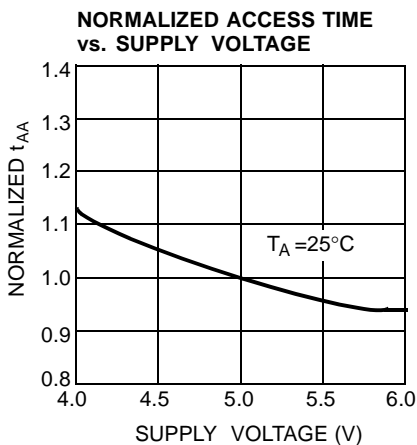
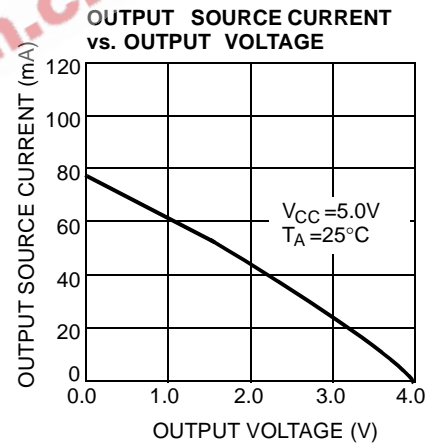
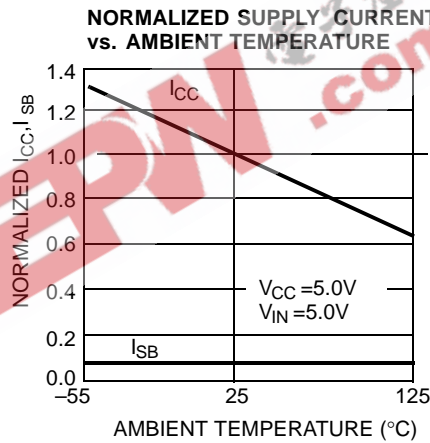
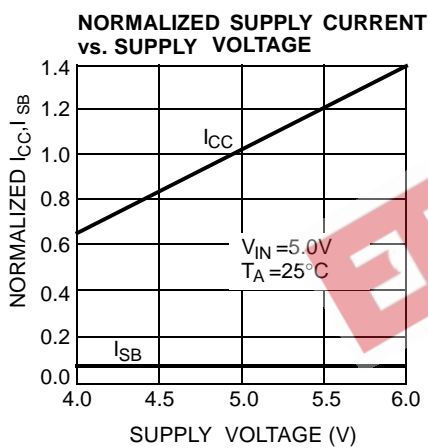


Write Cycle No. 2 (CE Controlled)^[10, 15, 16]



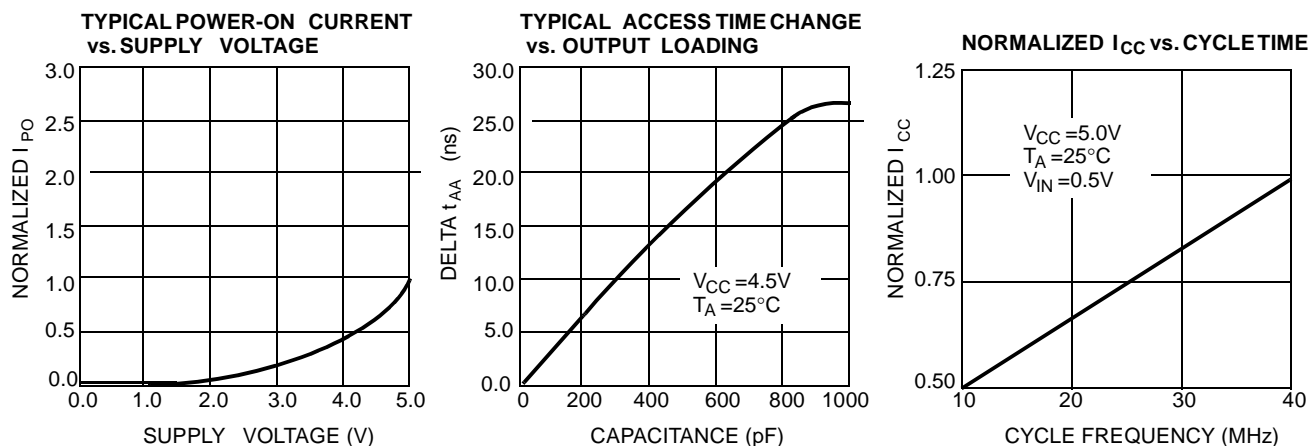
Notes:

- 14. Address valid prior to or coincident with \overline{CE} transition LOW.
- 15. Data I/O is high impedance if $OE = V_{IH}$.
- 16. If \overline{CE} goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Write Cycle No. 3 (WE Controlled \overline{OE} LOW)^[11, 16]

Typical DC and AC Characteristics




Typical DC and AC Characteristics (continued)



Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I _{SB})
L	H	L	Data Out	Read	Active (I _{CC})
L	L	X	Data In	Write	Active (I _{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I _{CC})

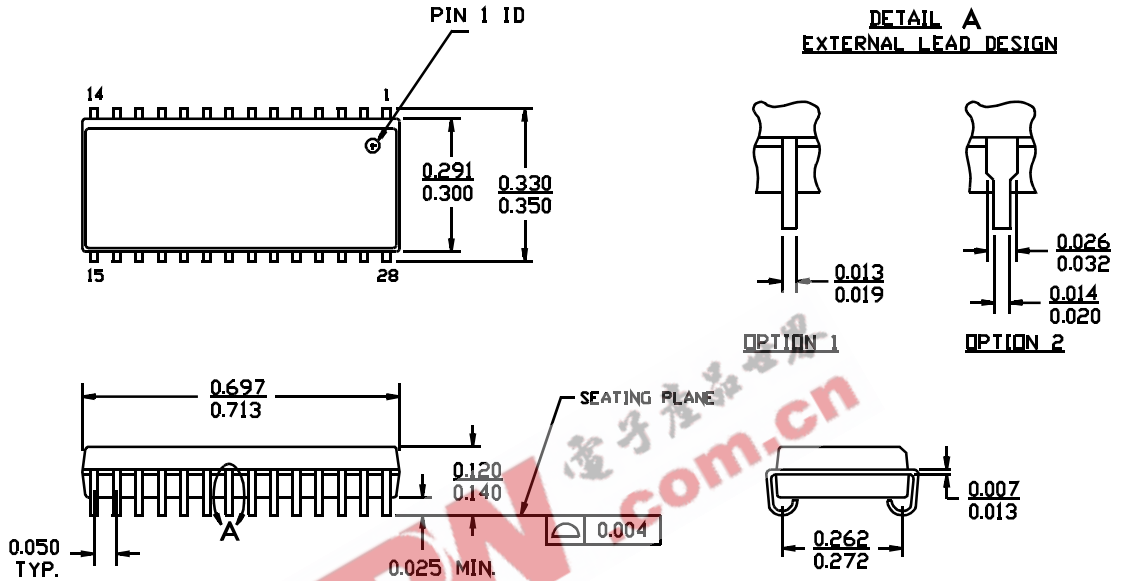
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	WCFS0808C1E-JC12	J	28-Lead Molded SOJ	Commercial
15	WCFS0808C1E-JC15	J	28-Lead Molded SOJ	

Package Diagrams

28-Lead (300-Mil) Molded SOJ,J

DIMENSIONS IN INCHES MIN.
MAX.





Document Title: WCFS0808C1E 32K x 8 Static RAM			
REV.	Issue Date	Orig. of Change	Description of Change
**	4/16/2002	XFL	New Datasheet

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