

W24L257A



32K × 8 HIGH-SPEED CMOS STATIC RAM

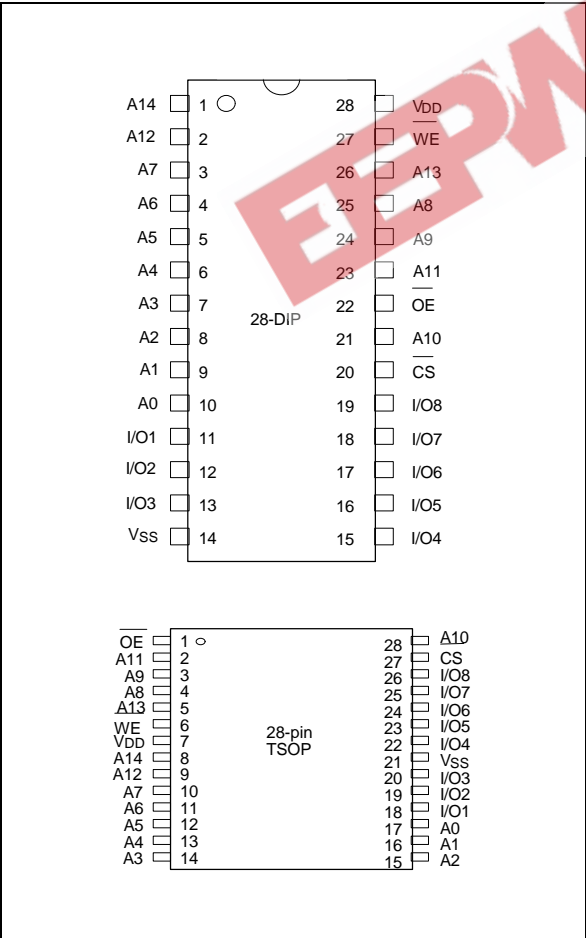
GENERAL DESCRIPTION

The W24L257A is a high-speed, low-power CMOS static RAM organized as 32768 × 8 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

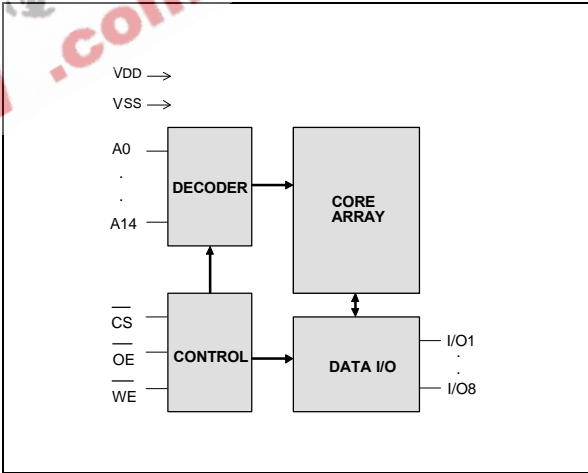
FEATURES

- High-speed access time: 12/15/20 nS (max.)
- Low-power consumption:
 - Active: 200 mW (typ.)
- Single +3.3V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 28-pin 300 mil SOJ, skinny DIP and standard type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
V _{DD}	Power Supply
V _{SS}	Ground



TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	MODE	I/O1–I/O8	V _{DD} CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +4.6	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 3.3V ± 5%, V_{SS} = 0V, T_a = 0 to 70° C)

PARAMETER	SYM	TEST CONDITIONS	MIN	TYP	MAX.	UNIT
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V _{IH}	-	+2.0	-	V _{DD} +0.3	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , \overline{CS} = V _{IH} (min.) or \overline{OE} = V _{IH} (min.) or \overline{WE} = V _{IL} (max.)	-10	-	+10	μA
Output Low Voltage	V _{OL}	I _{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA	2.4	-	-	V
Operating Power Supply Current	I _{DD}	\overline{CS} = V _{IL} (max.), I/O = 0 mA Cycle = min. Duty = 100%	12 15 20	- - -	150 120 100	mA mA mA
Standby Power Supply Current	ISB ISB1	\overline{CS} = V _{IH} (min.), Cycle = min. Duty = 100% $\overline{CS} \geq V_{DD} - 0.2V$	- -	- -	20 200	mA μA

Note: Typical characteristics are at V_{DD} = 3.3V, T_a = 25° C.



CAPACITANCE

(V_{DD} = 3.3V, T_a = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

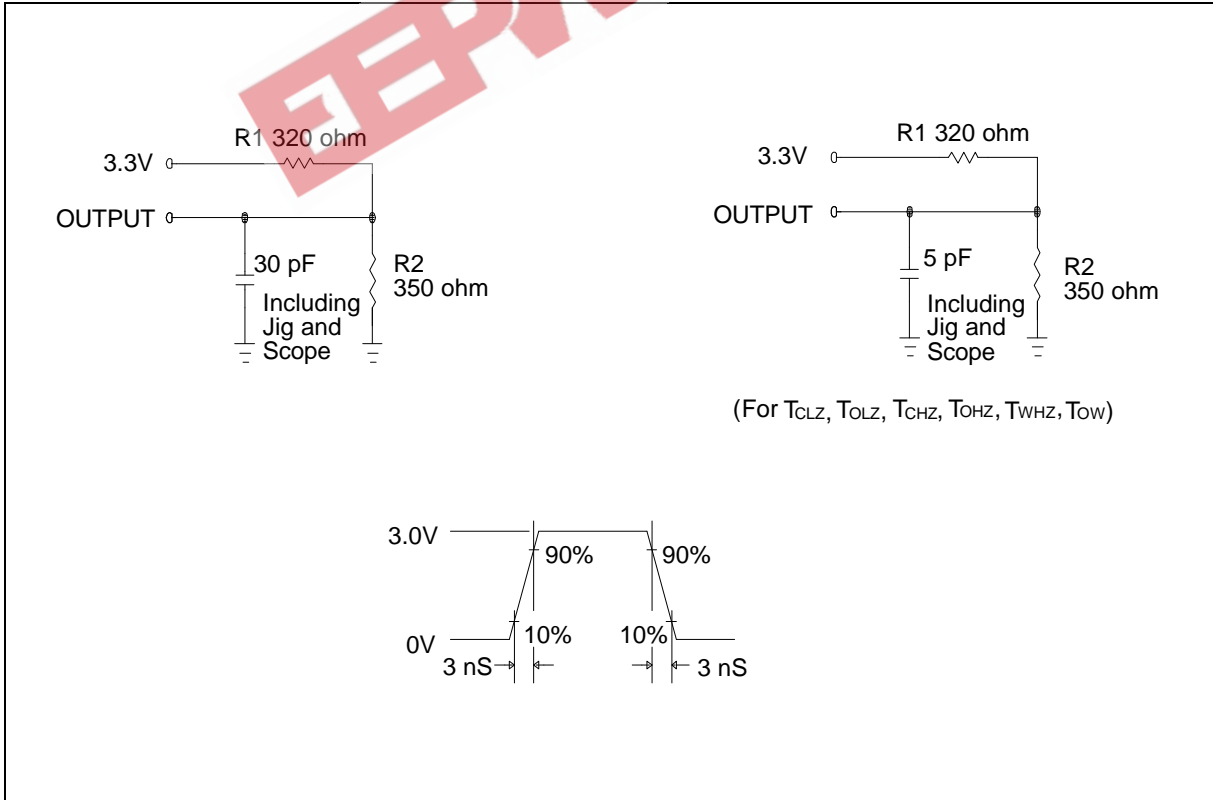
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 nS
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 30 pF, I _{OH} /I _{OL} = -4 mA/8 mA

AC Test Loads and Waveform



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AC Characteristics, continued
(V_{DD} = 3.3V ± 5%, V_{SS} = 0V, T_a = 0 to 70° C)

(1) Read Cycle

PARAMETER	SYM.	W24L257A-12		W24L257A-15		W24L257A-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	12	-	15	-	20	-	nS
Address Access Time	TAA	-	12	-	15	-	20	nS
Chip Select Access Time	TACS	-	12	-	15	-	20	nS
Output Enable to Output Valid	TAOE	-	6	-	8	-	10	nS
Chip Selection to Output in Low Z	TCLZ*	4	-	4	-	4	-	nS
Output Enable to Output in Low Z	TOLZ*	0	-	0	-	0	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	6	-	7	-	10	nS
Output Disable to Output in High Z	TOHZ*	-	6	-	7	-	10	nS
Output Hold from Address Change	TOH	3	-	3	-	3	-	nS

*These parameters are sampled but not 100% tested

(2) Write Cycle

PARAMETER	SYM.	W24L257A-12		W24L257A-15		W24L257A-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	TWC	12	-	15	-	20	-	nS
Chip Selection to End of Write	TCW	10	-	13	-	17	-	nS
Address Valid to End of Write	TAW	10	-	13	-	17	-	nS
Address Setup Time	TAS	0	-	0	-	0	-	nS
Write Pulse Width	TWP	10	-	10	-	12	-	nS
Write Recovery Time	\overline{CS} , \overline{WE} TWR	1	-	1	-	1	-	nS
Data Valid to End of Write	TDW	7	-	9	-	10	-	nS
Data Hold from End of Write	TDH	0	-	0	-	0	-	nS
Write to Output in High Z	TWHZ*	-	7	-	8	-	10	nS
Output Disable to Output in High Z	TOHZ*	-	7	-	8	-	10	nS
Output Active from End of Write	TOW	0	-	0	-	0	-	nS

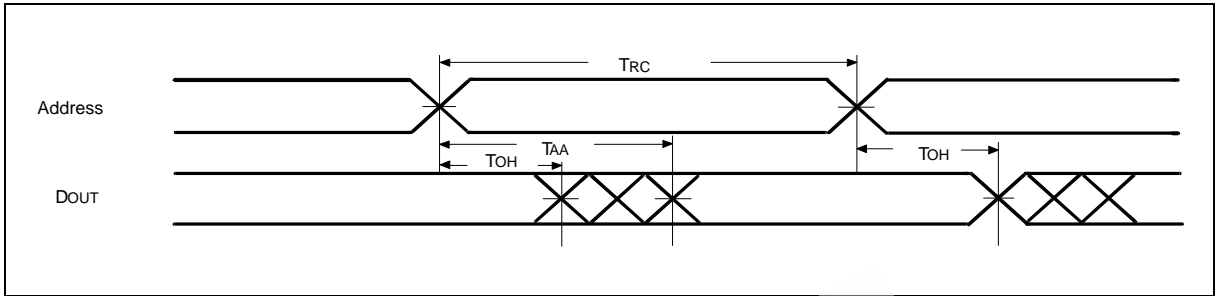
*These parameters are sampled but not 100% tested



TIMING WAVEFORMS

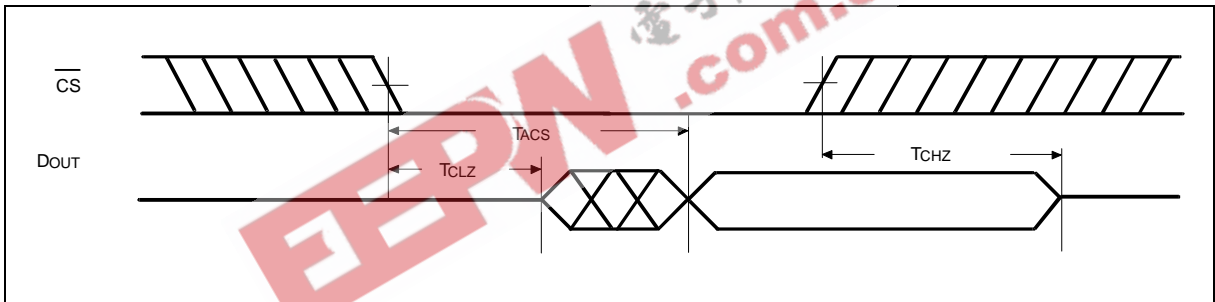
Read Cycle 1

(Address Controlled)



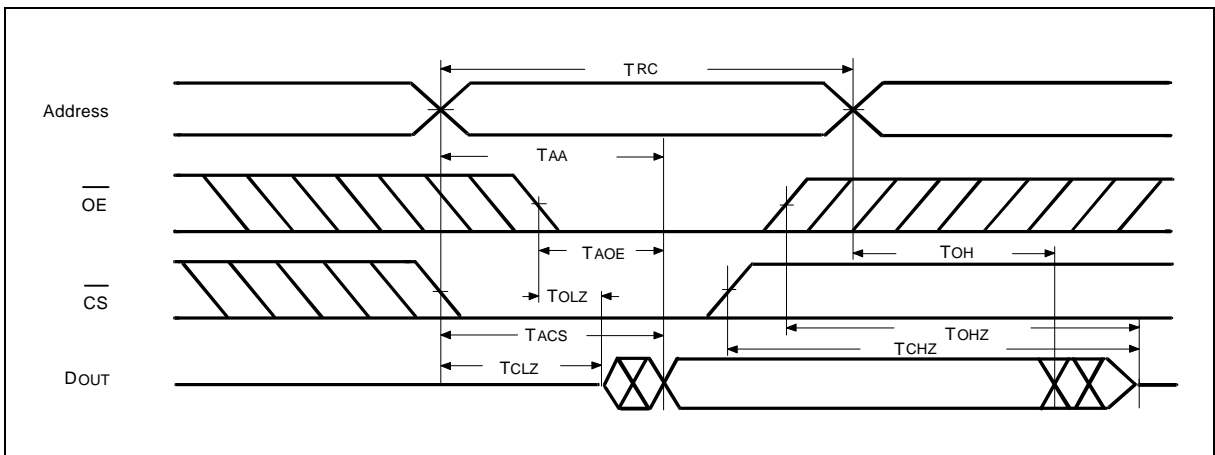
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

(Output Enable Controlled)

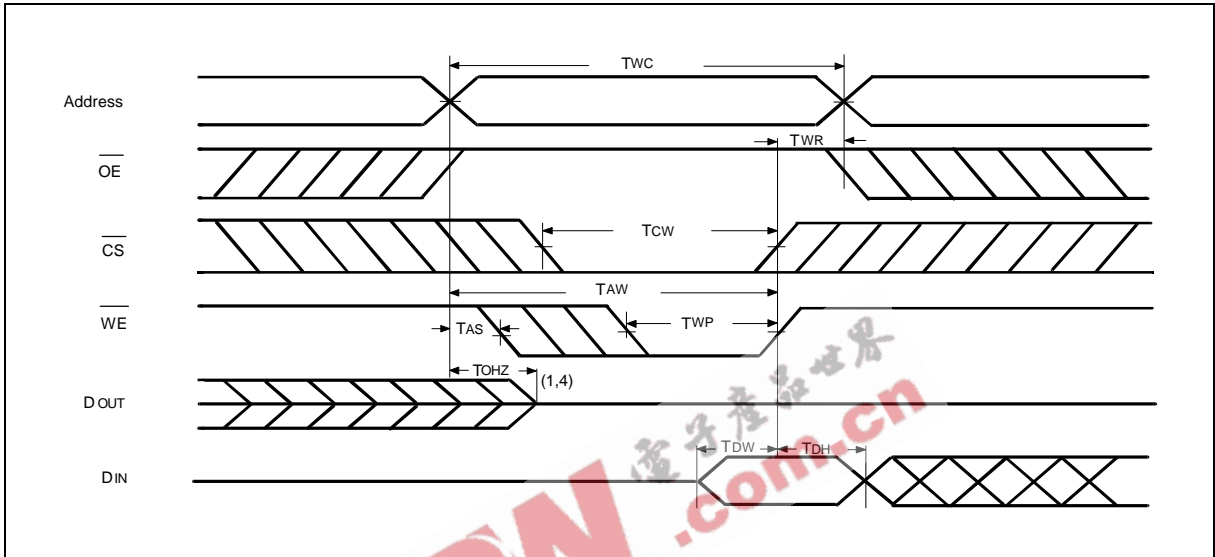




Timing Waveforms, continued

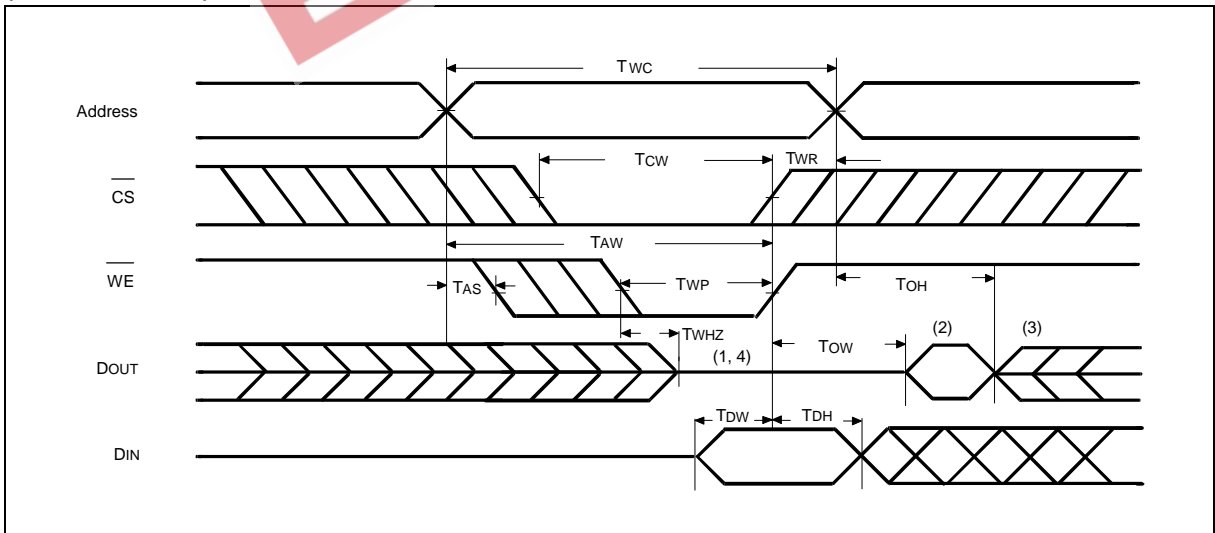
Write Cycle 1

($\overline{\text{OE}}$ Clock)



Write Cycle 2

($\overline{\text{OE}} = \text{VIL Fixed}$)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

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ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (μ A)	PACKAGE
W24L257AK-12	12	150	200	300 mil Skinny
W24L257AK-15	15	120	200	300 mil Skinny
W24L257AK-20	20	100	200	300 mil Skinny
W24L257AJ-12	12	150	200	300 mil SOJ
W24L257AJ-15	15	120	200	300 mil SOJ
W24L257AJ-20	20	100	200	300 mil SOJ
W24L257AQ-12	12	150	200	Standard type one TSOP
W24L257AQ-15	15	120	200	Standard type one TSOP
W24L257AQ-20	20	100	200	Standard type one TSOP

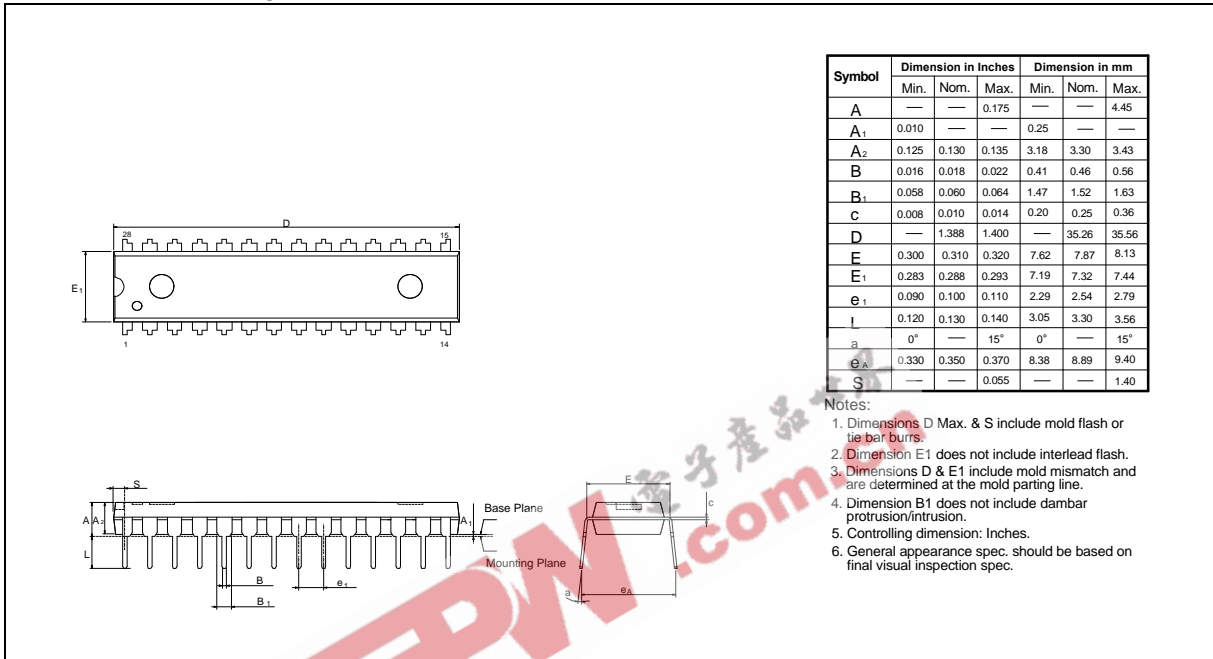
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

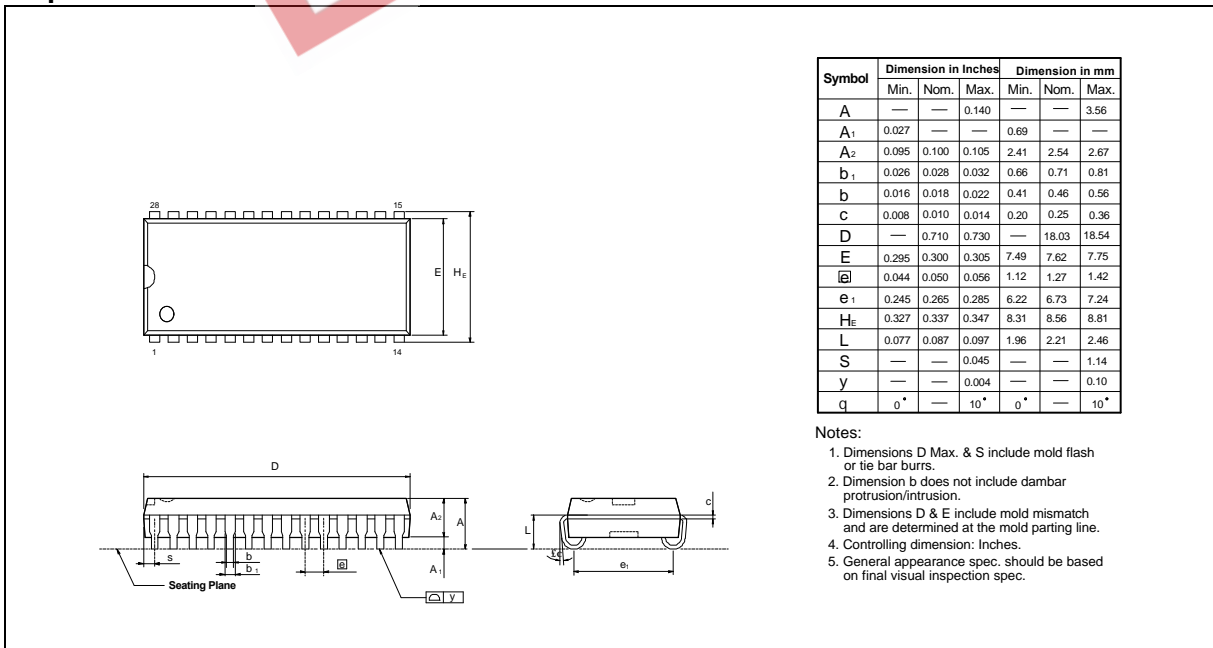


PACKAGE DIMENSIONS

28-pin P-DIP Skinny



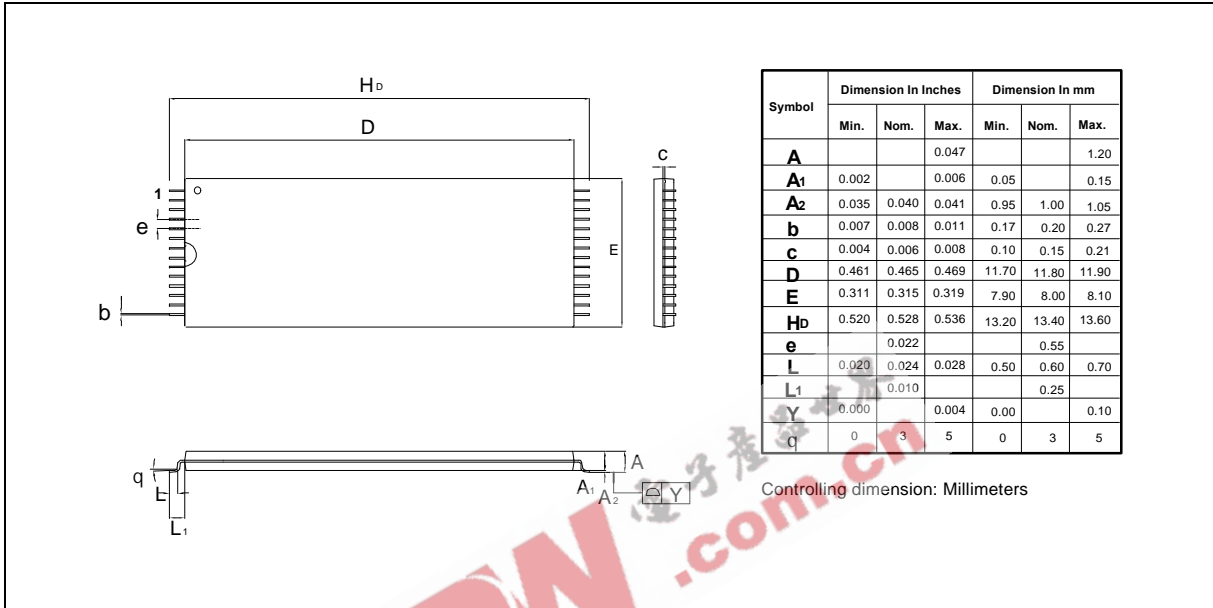
28-pin Small Outline J Band





Package Dimensions, continued

28-pin Standard Type One TSOP



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Note: All data and specifications are subject to change without notice.