WM5628L, WM5628

Production Data
Sept. 1996 Rev 2

3 & 5V Octal 8-Bit Voltage Output DAC with Serial Interface

Description

WM5628L and WM5628 are Octal 8-bit digital to analogue converters (DAC) controlled via a serial interface. Each DAC's output voltage range is programmable for either x1 or x 2 its reference input voltage, allowing near rail to rail operation for the x 2 output range. High impedance buffered voltage reference inputs are provided for each group of four DACs. WM5628L operates on a single supply voltage of 3 V while WM5628 operates on 5 V.

WM5628/L interfaces to all popular microcontrollers and microprocessors via a three wire serial interface with CMOS compatible, schmitt trigger, digital inputs. An 12 bit command word comprises 3 DAC select bits, an output range selection bit and 8-bits of data.

Individual or all DAC outputs are changed using WM5628/L's double buffered DAC registers and the separate LOAD and LDAC inputs. DAC outputs are updated simultaneously by writing a complete set of new values and then pulsing the LDAC input.

The DAC outputs are optimised for single supply operation and driving ground referenced loads.

An internal power-on-reset function sets the DAC's input codes to zero at power up.

Ideal in space critical applications WM5628/L is available in wide-bodied and DIP packages for commercial (0ºC to 70ºC) and industrial (-40ºC to 85ºC) temperature ranges.

Features

- **Eight 8-bit voltage output DAC's**
- **Three wire serial interface**
- **Programmable x1 or x 2 output range.**
- **Power-on-reset sets outputs to zero**
- **Buffered voltage reference inputs**
- **Simultaneous DAC output update**

Key Specifications

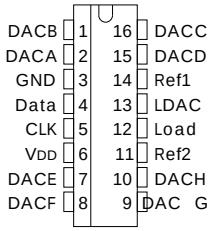
- **Single supply operation:**
  WM5628L : 3 V
  WM5628 : 5 V
- **0 to 4 V output (x 2 output range) at 5 V V_{DD}**
- **0 to 2.5 V output (x 2 output range) at 3 V V_{DD}**
- **Guaranteed monotonic output**

Applications

- **Programmable d.c. voltage sources**
- **Digitally controlled attenuator/amplifier**
- **Signal synthesis**
- **Mobile communications**
- **Automatic test equipment**
- **Process control**

Pin Configuration

Top View
16 pin N and DW packages



Ordering Information

DEVICE	TEMP. RANGE	PACKAGE
WM5628CN	0ºC to 70ºC	16 pin plastic DIP
WM5628CDW	0ºC to 70ºC	16 pin wide-bodied plastic SO
WM5628IN	-40ºC to 85ºC	16 pin plastic DIP
WM5628IDW	-40ºC to 85ºC	16 pin wide-bodied plastic SO
WM5628LCN	0ºC to 70ºC	16 pin plastic DIP
WM5628LCDW	0ºC to 70ºC	16 pin wide-bodied plastic SO
WM5628LIN	-40ºC to 85ºC	16 pin plastic DIP
WM5628LIDW	-40ºC to 85ºC	16 pin wide-bodied plastic SO

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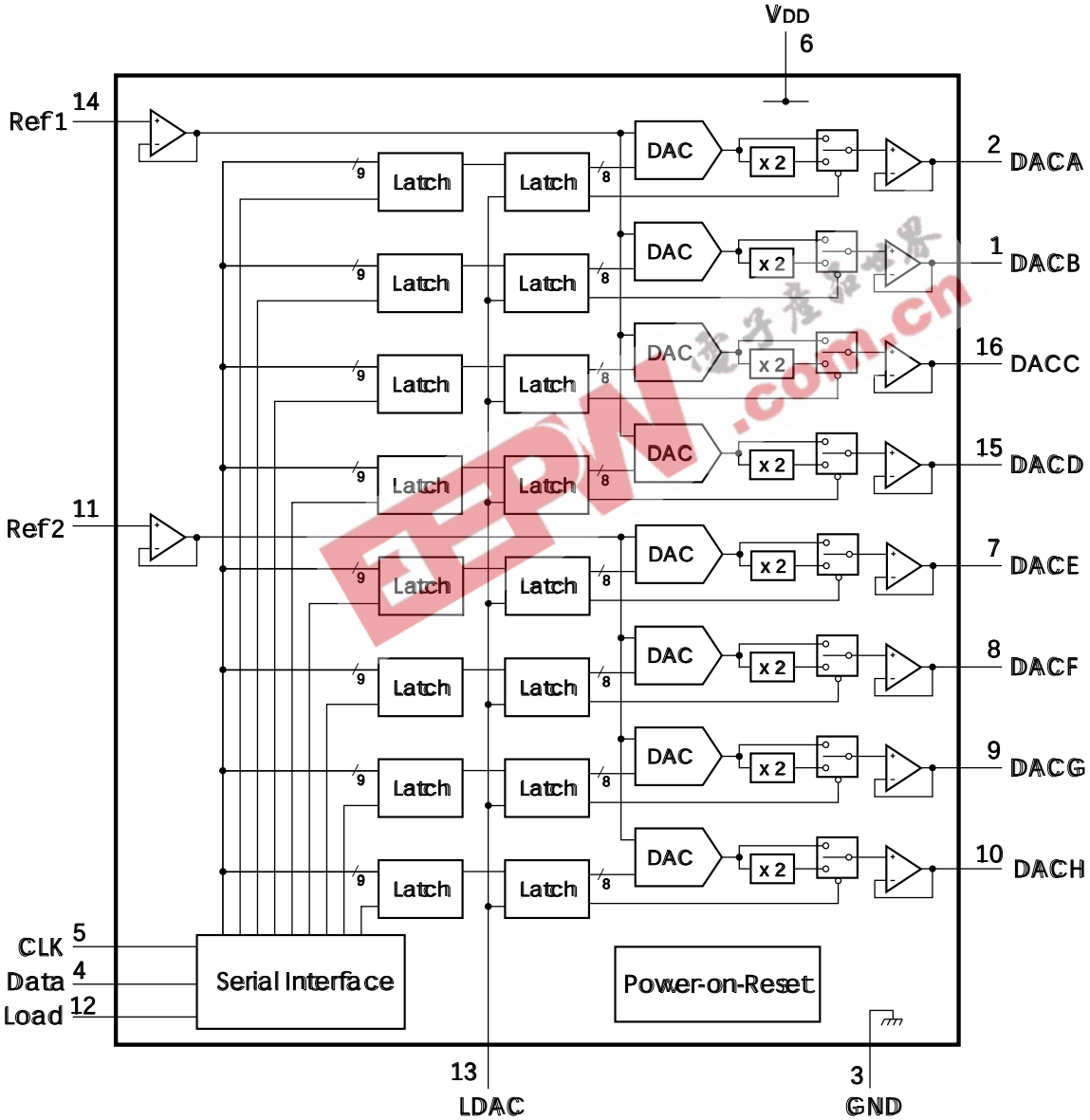
Block Diagram



Absolute Maximum Ratings (note 1)

Supply Voltage (VDD - VGND) . . . . . +7V
Digital Inputs . . . . . .GND - 0.3 V, V_{DD} + 0.3 V
Reference inputs . . . . . GND - 0.3 V, V_{DD} + 0.3 V

Operating temperature range, TA . . . . . T_{MIN} to T_{MAX}
WM5628_C_ . . . . . 0°C to +70°C
WM5628_I_ . . . . . -40°C to +85°C
Storage Temperature . . . . . -50°C to +150°C
Lead Temperature 1.6mm (1/16 inch)
from case for 10 secs . . . . . 260°C

Recommended Operating Conditions

	SYMBOL	MIN	NOMINAL	MAX	UNIT
Supply voltage WM5628	V_{DD}	4.75		5.25	V
Supply Voltage WM5628L	V_{DD}	2.7		5.25	V
Reference input range, X1 gain	V_{REF}		3.3	V_{DD} - 1.5	V
DAC output load resistance to GND	R_L	10			kΩ
High level digital input voltage	V_{IH}	0.8 VDD			V
Low level digital input voltage	V_{IL}			0.8	V
Clock frequency	F_{CLK}			1	MHz

Electrical Characteristics: WM5628

V_{DD} = 5 V, GND = 0 V, V_{REF} = 2 V, R_L = 10 kΩ, C_L = 100 pF, T_A = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
Supply current	I_{DD}	Outputs unloaded, digital inputs = 0 V or V_{DD}			4.0	mA
Static Accuracy						
Resolution			8			Bits
Monotonicity			8			Bits
Differential Nonlinearity	DNL	V_{REF} = 2 V, Range x 2. (note 3)		± 0.1	± 0.9	LSB
Integral Nonlinearity	INL	V_{REF} = 2 V, Range x 2. (note 4)			± 1.0	LSB
Zero-code error	ZCE	V_{REF} = 2 V, Range x 2. (note 5)			30	mV
Zero-code error temperature coefficient		Input code = 00 Hex (note 6)		10		µV/°C
Zero-code error supply rejection		Input code = 00 Hex, V_{DD} = 5 V ± 5 % (note 7)		0.5		mV/V
Full scale error	FSE	V_{REF} = 2 V, Range x 2. (note 8)			± 60	mV
Full scale error temperature coefficient		Input code = FF Hex (note 9)		± 25		µV/°C
Full scale error supply rejection		Input code = FF Hex, V_{DD} = 5 V ± 5 % (note 10)		0.5		mV/V
Output sink current	$I_{O(SINK)}$	Each DAC output	20			µA
Output source current	$I_{O(SOURCE)}$		2			mA

Electrical Characteristics: WM5628L

V_{DD} = 3 .6V, GND = 0 V, V_{REF} = 2 V x 1 gain, R_L = 10 kΩ, C_L = 100 pF, T_A = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
Supply current	I_{DD}	V_{DD} = 3.3v			4	mA
Static Accuracy						
Resolution			8			Bits
Monotonicity			8			Bits
Differential Nonlinearity	DNL	V_{REF} = 1.25 V, Range x 2. (note 3)			± 0.9	LSB
Integral Nonlinearity	INL	V_{REF} = 1.25 V, Range x 2. (note 4)		± 1.0		LSB
Zero-code error	ZCE	V_{REF} = 1.25 V, Range x 2. (note 5)	0		30	mV
Zero-code error temperature coefficient		Input code = 00 Hex (note 6)		10		µV/°C
Full scale error	FSE	V_{REF} = 1.25 V, Range x 2. (note 8)		± 60		mV
Full scale error temperature coefficient		Input code = FF Hex (note 9)		± 25		µV/°C
Output sink current	$I_{O(SINK)}$	Each DAC output	20			µA
Output source current	$I_{O(SOURCE)}$		1			mA
Power supply sensitivity	I_{REF} PSRR	VDD = 3.3V, V_{REF} = 1.5V		0.5		mV/V

Electrical Characteristics: WM5628 & WM5628L

V_{DD} = 2.7 to 5.5V, GND = 0 V, V_{REF} = 2 V x 1 gain, R_L = 10 kΩ, C_L = 100 pF, T_A = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
High level input current	I_{IH}	V_I = V_{DD}			±10	µA
Low level input current	I_{IL}	V_I = 0V			±10	µA
Input capacitance	C_I			15		pF
Timing Parameters						
Data input setup time	t_{SD}		50			ns
Data input hold time	t_{HD}		50			ns
CLK ↓ to Load ↓	t_{HL}		50			ns
Load ↑ to CLK ↓	t_{SL}		50			ns
Load duration	t_{WL}		250			ns
LDAC duration	t_{WD}		250			ns
Load ↓ to LDAC ↓	t_{LD}		0			ns
Reference Inputs						
Reference input voltage	V_{REF}	A, B, C, D, inputs	GND		V_{DD}-1.5	V
Reference input capacitance		A, B, C, D, inputs		15		pF
Reference feedthrough		A, B, C, D inputs (note 11)		-60		dB
Channel to channel isolation		A, B, C, D inputs (note 12)		-60		dB

Electrical Characteristics: WM5628 & WM5628L (continued)

V_{DD} = 3 .6V, GND = 0 V, V_{REF} = 2 V x 1 gain, R_L = 10 kΩ, C_L = 100 pF, T_A = full range, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Performance						
Output settling time		To 1/2LSB, VDD=3V & 5V (note 13)		10		µs
Output slew rate				1		V/µs
Input bandwidth		(note 14)		100		kHz
Large Signal Bandwidth		Measured at -3dB point		100		kHz
Digital Crosstalk		Clk = 1MHz sq wave measured at DACA - DACD		-50		dB

Notes:

1. Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating range limits are given under Recommended Operating Conditions. Guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

2. Total Unadjusted Error is the sum of integral linearity error, zero code error and full scale error over the input code range.

3. Differential Nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

4. Integral Nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).

5. Zero code error is the deviation from zero voltage output when the digital input code is zero.

6. Zero code error temperature coefficient is given by: $ZCETC = (ZCE(T_{max} - ZCE(T_{min})) / V_{REF} \times 10^6 / (T_{max} - T_{min})$

7. Zero-code Error Rejection Ratio (ZCE-RR) is measured by varying the V_{DD} voltage, from 4.5 to 5.5 V d.c., and measuring the proportion of this signal imposed on the zero-code output voltage.

8. Full-scale error is the deviation from the ideal full-scale output (V_{REF} - 1LSB) with an output load of 10kΩ

9. Full-Scale Temperature Co-efficient is given by: $FSETC = (FSE(T_{max}) - FSE(T_{min})) / V_{REF} \times 10^6 / T_{max} - T_{min})$

10. Full Scale Error Rejection Ratio (FSE-RR) is measured by varying the V_{DD} voltage from 4.5 to 5.5 V d.c. and measuring the proportion of this signal imposed on the full-scale output voltage

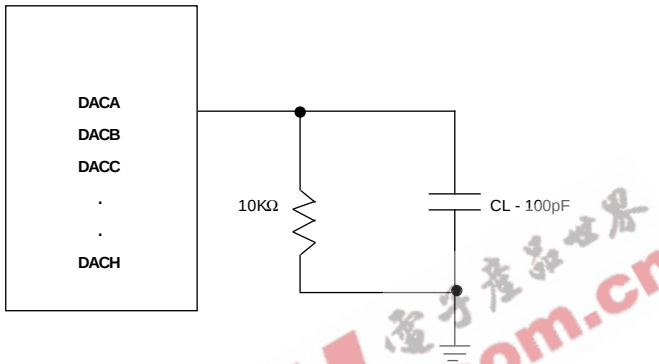
11 Reference feedthrough is measured at a DAC output with an input code = 00 Hex with a V_{REF} input = 1 V_{dc} + 1 V_{PP} at 10kHz

12. Channel to channel isolation is measured at a DAC output with an input code of one DAC to FF Hex and the code oa all other DACs to oo Hex with a V_{REF} input = 1 V_{dc} + 1 V_{pp} at 10kHz

13 Setting time is the time for the output signal to remain within ±0.5 LSB of the final measurement value for a digital input code change of 00 Hex to FF Hex. For WM 5628: V_{DD} = 5V, V_{REF} = 2V and range = x 2. For WM5628L: V_{DD} = 3, V_{REF} = 1.25V and range = x 2.

14 Reference bandwidth is the -3dB bandwidth with an input at V_{REF} = 1.25 V_{dc} =+ 2 V_{pp} with a digital input code of full-scale.

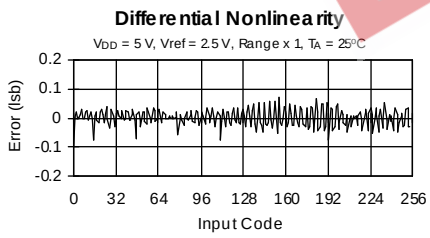
Parameter Measurement Information

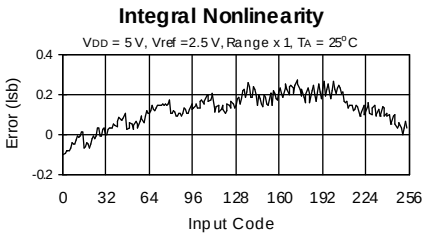


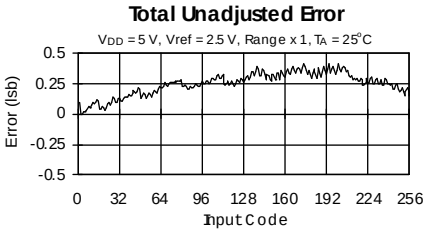
Slewing Settling Time and Linearity Measurements

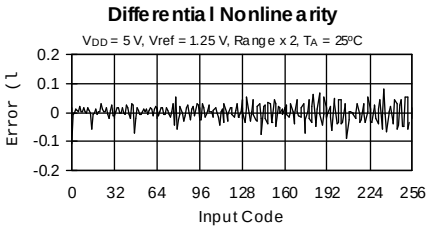
Typical Performance Characteristics

Typical DNL, INL and TUE * at V_{DD} = 5 V







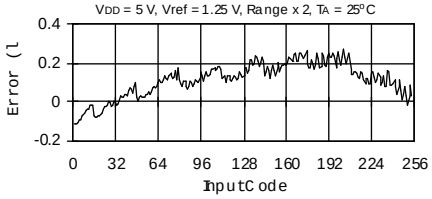


* see note 2

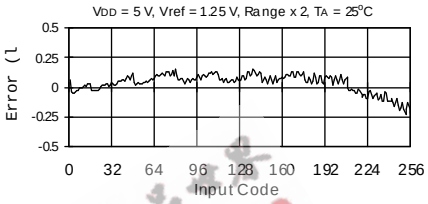
Typical Performance Characteristics (continued)

Typical DNL, INL and TUE * at V_{DD} = 5 V (continued)

Integral Nonlinearity

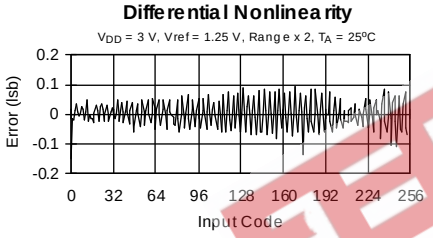


Total Unadjusted Error

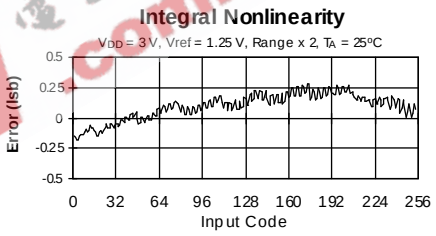


Typical DNL, INL and TUE at VDD = 3 V

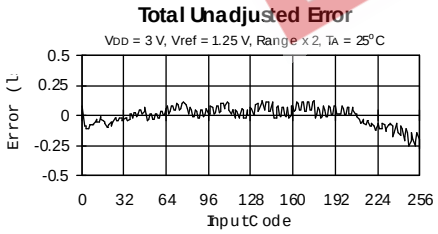
Differential Nonlinearity



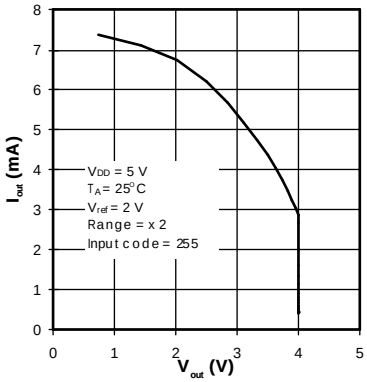
Integral Nonlinearity



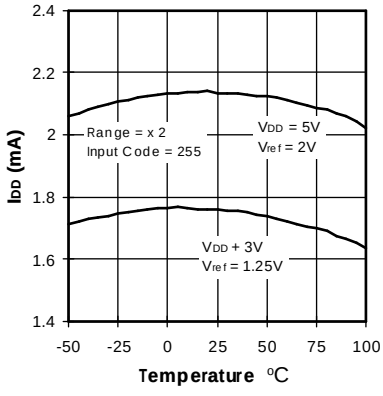
Total Unadjusted Error



Output Source Current vs Output Voltage

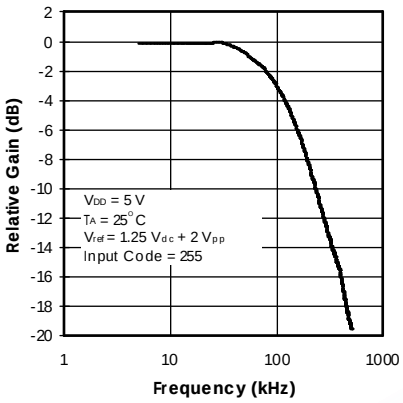


Supply Current vs Temperature

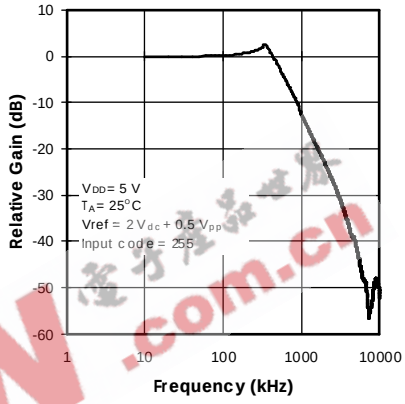


Typical Performance Characteristics (continued)

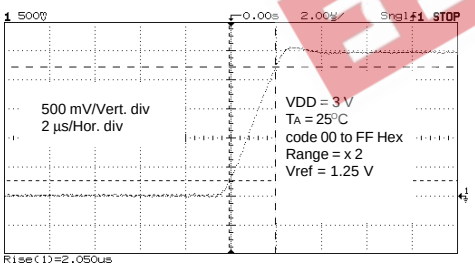
Large Signal Frequency Response



Small Signal Frequency Response

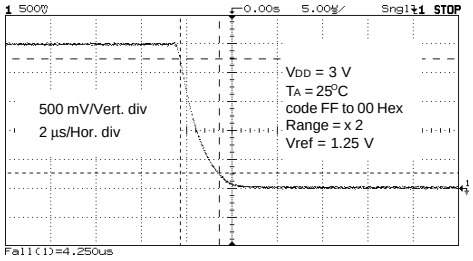


Positive Rise and Settling Time VDD = 3 V



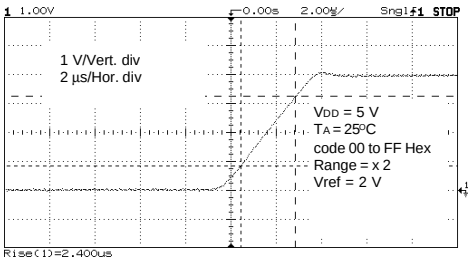
Rise time = 2.5 µs, Positive slew rate = 0.80 µs
Settling time = 4.5 µs

Negative Fall and Settling Time VDD = 3 V



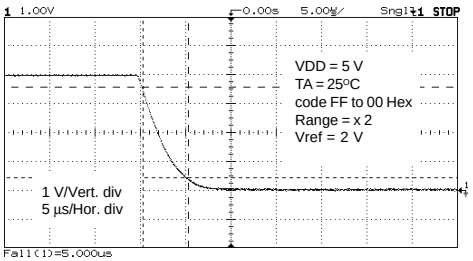
Fall time = 4.85 µs, Negative slew rate = 0.41 µs
Settling time = 8.0 µs

Positive Rise and Settling Time VDD = 5 V



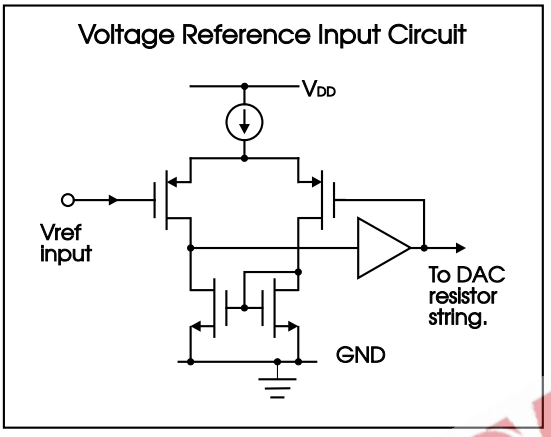
Rise time = 3.75 µs, Positive slew rate = 0.54 µs
Settling time = 5.9 µs

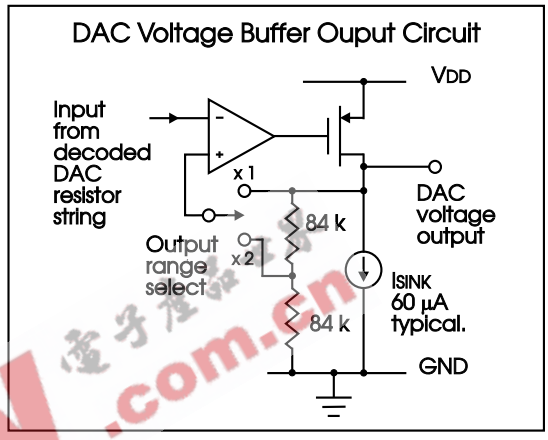
Negative Fall and Settling Time VDD = 5 V



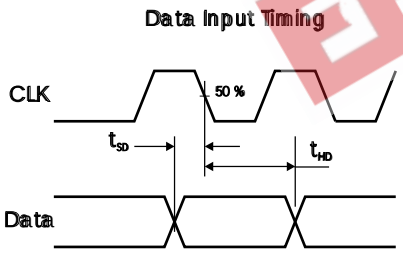
Fall time = 5.9 µs, Negative slew rate = 0.54 µs
Settling time = 8.5 µs

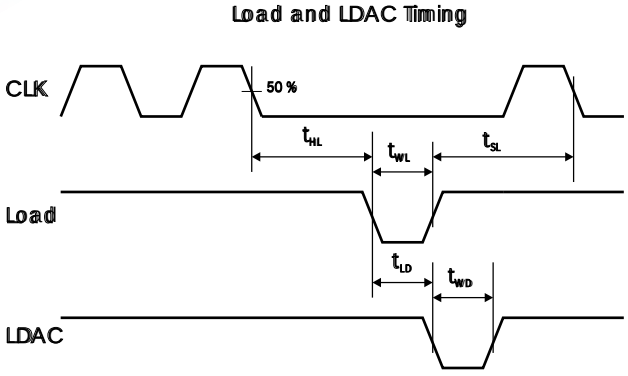
Equivalent Input and Output Circuits





Timing Waveforms





Timing Diagrams

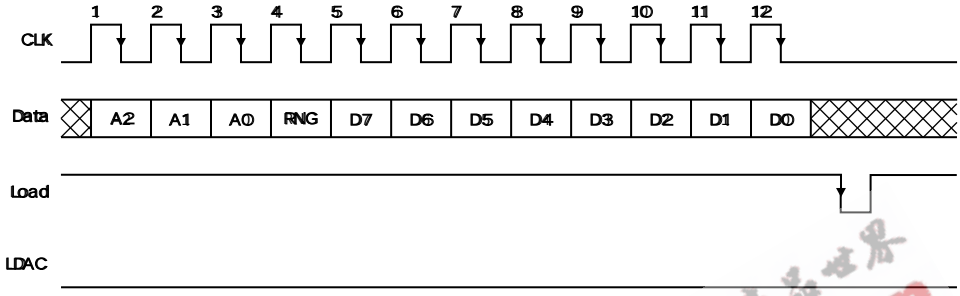


Figure 1. Load controlled update (LDAC = 0)

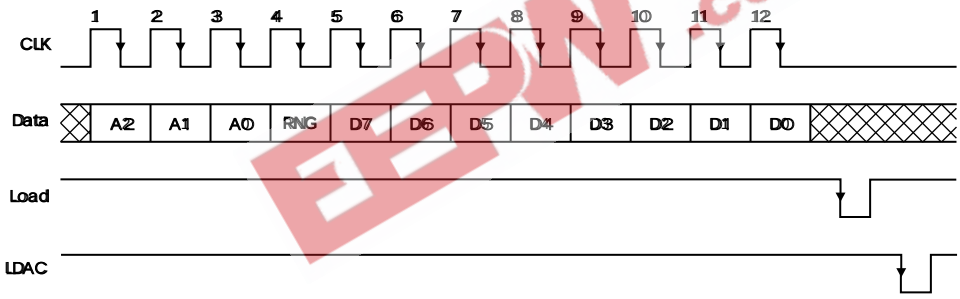


Figure 2. LDAC controlled update

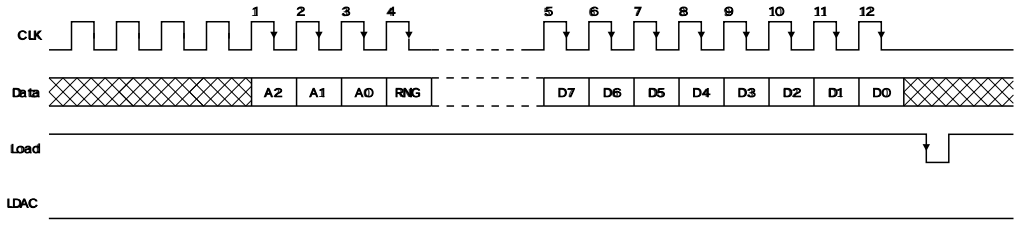


Figure 3. Load controlled update (LDAC = 0) using 8-bit serial word.

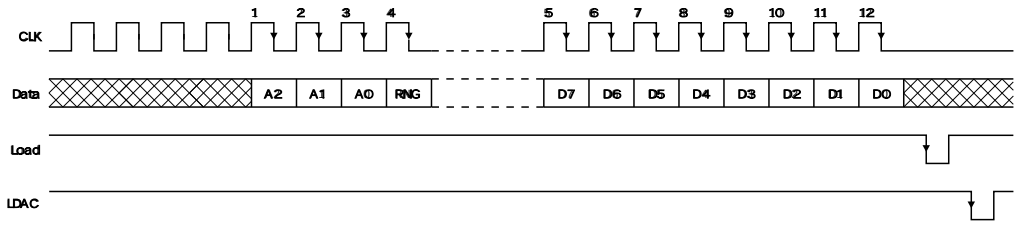


Figure 4. LDAC controlled update using 8-bit serial word.

Pin Descriptions

Pin	Name	Type	Function
1	DACB	Analogue output	DAC B output
2	DACA	Analogue input	DAC A output
3	GND	Supply	Ground return
4	Data	Digital input	Serial data input
5	CLK	Digital input	Serial interface clock, negative edge sensitive
6	V_{DD}	Supply	Positive supply voltage
7	DACE	Analogue output	DAC E output
8	DACF	Analogue output	DAC F output
9	DACG	Analogue output	DAC G output
10	DACH	Analogue output	DAC H output
11	Ref2	Analogue input	Reference to DACE, DACF, DACG and DACH
12	Load	Digital input	Serial input load
13	LDAC	Digital input	DAC update latch control
14	Ref1	Analogue input	Reference to DACA, DACB, DACC and DACD
15	DACD	Analogue output	DAC D output
16	DACC	Analogue output	DAC C output

Functional Description

DAC operation

Each of WM5628/L 's eight digital to analogue converters (DACs) are implemented using a single resistor string with 256 taps corresponding to each of the input 8-bit codes. One end of a resistor string is connected to the GND pin and the other end is driven from the output of a reference input buffer. The use of a resistor string guarantees monotonicity of the DAC's output voltage. Linearity depends upon the matching of the resistor string's individual elements and the performance of the output buffer. Two high input impedance voltage reference buffers are provided, each driving four DACs,

Each DAC has a voltage output amplifier which is programmable for gains of x1 or x 2 through the serial interface. The DAC output amplifiers feature rail to rail output stages, allowing outputs over the full supply voltage range to be achieved with a x 2 gain setting and a $V_{DD}/2$ reference voltage input. Used in this way a slight degradation in linearity will occur as the output voltage approaches V_{DD}.

A power-on-reset activates at power up resetting the DACs inputs to code 0. Each output voltage is given by:

$$V_{out} = V_{ref} \times CODE/256 \times (RNG+1)$$

Where: RNG controls the output gains of x 1 and x 2
CODE is the range 0 to 255

Data Interface

WM5628/L's eight double buffered DAC inputs allow several ways of controlling the update of each DAC's output.

Serial data is input, MSB first, into the DATA input pin Serial Input DAC Address and Output Tables using CLK, LOAD and LDAC control inputs and comprises 3 DAC address bits, an output range (RNG) bit and 8 DAC input bits.

With the LOAD pin high data is clocked into the DATA pin on each falling edge of CLK. Any number of data bits may be clocked in, only the last 12 bits are used. When all data bits have been clocked in, a falling edge at the LOAD pin latches the data and RNG bits into the correct 9 bit input latch using the 3 bit DAC address.

If the LDAC input pin is low, the second latch at the DAC input is transparent, and the DAC input and RNG bit will be updated on the falling edge of LOAD simultaneously with the input latch, as shown in figure 1. If the LDAC input is high during serial data input, as shown in figure 2, the falling edge of the LOAD input stores the data in the addressed input latch. The falling edge of LDAC updates the second latches from the input latches and hence the DAC outputs.

Functional Description (continued)

Using these inputs individual DACs can be updated using one 12 bit serial input word and the LOAD pin. Using both LOAD and LDAC, all or selected DACs can be updated after an appropriate number of data words have been inputted. Figures 3 &4 illustrate operation with the 8 clock pulses available from some microprocessors. If the data input is interrupted in this way the clock input must be held low during the break in clock pulses.

The RNG bit controls the DAC output range. When RNG = 0 the output is between Vref(A,B,C,D) and GND and when RNG = 1 the range is between 2 x Vref (A,B,C,D) and GND.

Serial Input DAC Address and Output Tables

A2	A1	A0	DAC Updated
0	0	0	DACA
0	0	1	DACB
0	1	0	DACC
0	1	1	DACD
1	0	0	DACE
1	0	1	DACF
1	1	0	DACG
1	1	1	DACH

D7	D6	D5	D4	D3	D2	D1	D0	Output Voltage
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) x Ref (1 + RNG)
o	o	o	o	o	o	o	o	o
o	o	o	o	o	o	o	o	o
0	1	1	1	1	1	1	1	(127/256) x Ref (1 + RNG)
1	0	0	0	0	0	0	0	(128/256) x Ref (1 + RNG)
o	o	o	o	o	o	o	o	o
o	o	o	o	o	o	o	o	o
1	1	1	1	1	1	1	1	(255/256) x Ref (1 + RNG)

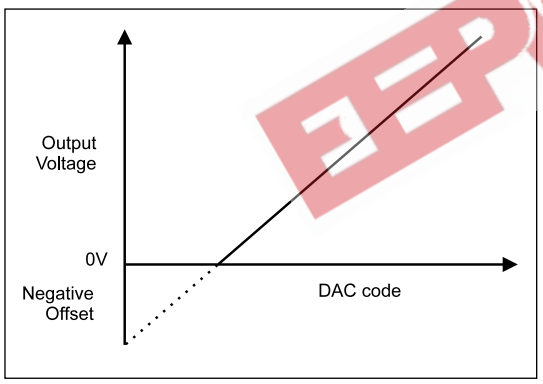
Functional Description (Continued)

Linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is GND, the output cannot drive to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at ZERO volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown below



Effect of negative offset (single supply)

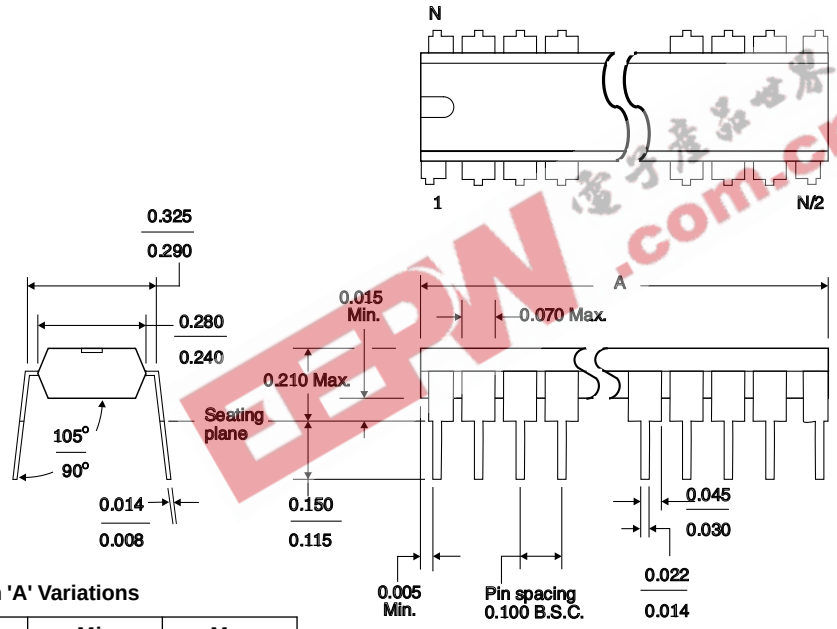
This negative offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive to a negative voltage.

For a DAC, linearity is measured between ZERO input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the break-point in the transfer function. So the linearity in the unipolar mode is measured between full scale code and the lowest code which produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

Package Descriptions

Dual-In-Line Package

N or P



Dimension 'A' Variations

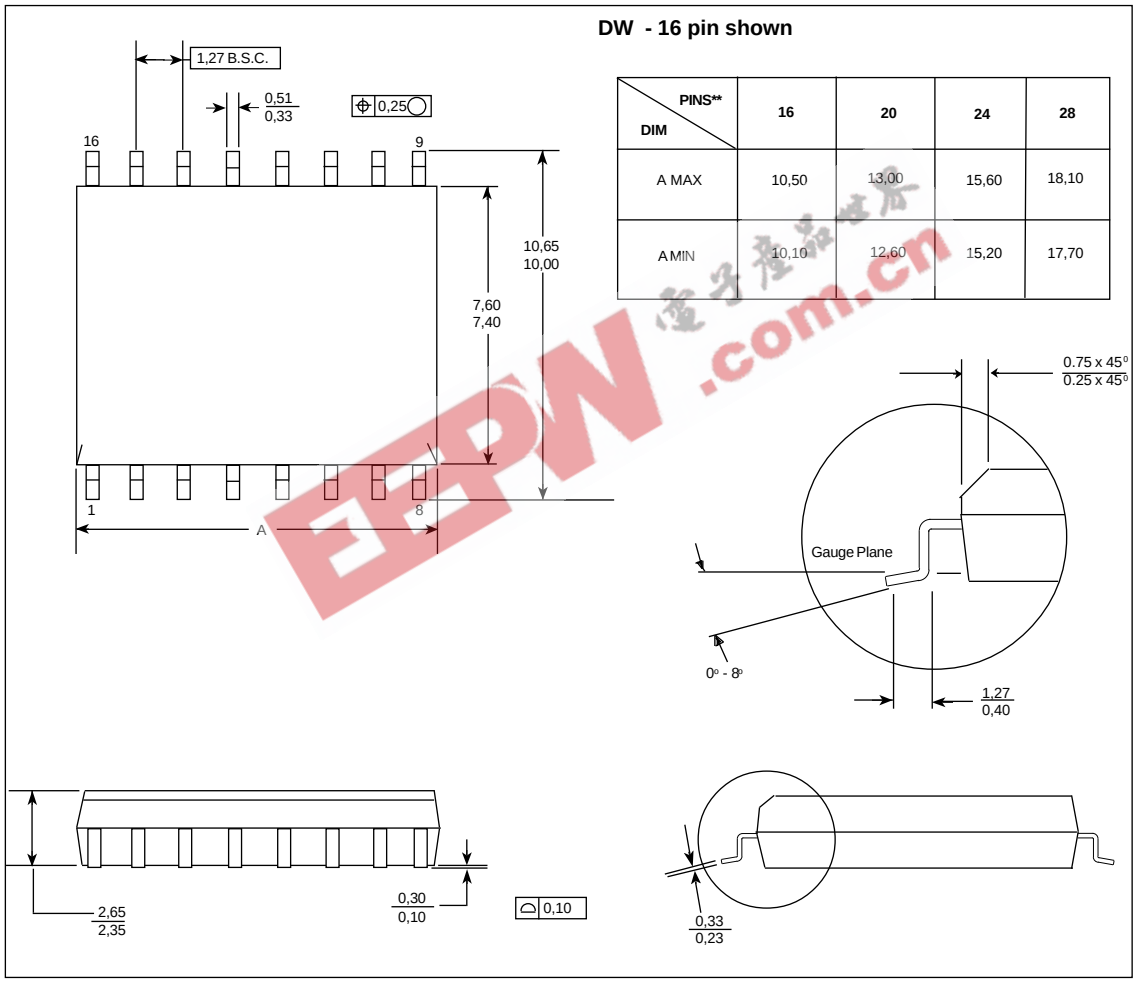
N	Min	Max
8	0.355	0.400
14	0.735	0.775
16	0.735	0.775
20	0.940	0.975

Notes:

A. Dimensions are in inches
B. Falls within JEDEC MS-001(20 pin package is shorter than MS-001)
C. N is the maximum number of terminals
D. All end pins are partial width pins as shown, except the 14 pin package which is full width.

Package Description

Wide body Plastic Small-Outline Package



DIM \ PINS**	16	20	24	28
A MAX	10,50	13,00	15,60	18,10
A MIN	10,10	12,60	15,20	17,70

Notes:

A. Dimensions in millimeters.
B. Complies with Jedec standard MS-013.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion.
E. Dimension A, mould flash or protrusion shall not exceed 0.15mm. Body width, interlead flash or protrusions shall not exceed 0.25mm.