Winbond Electronics Corp.

64K × 8 HIGH SPEED CMOS STATIC RAM

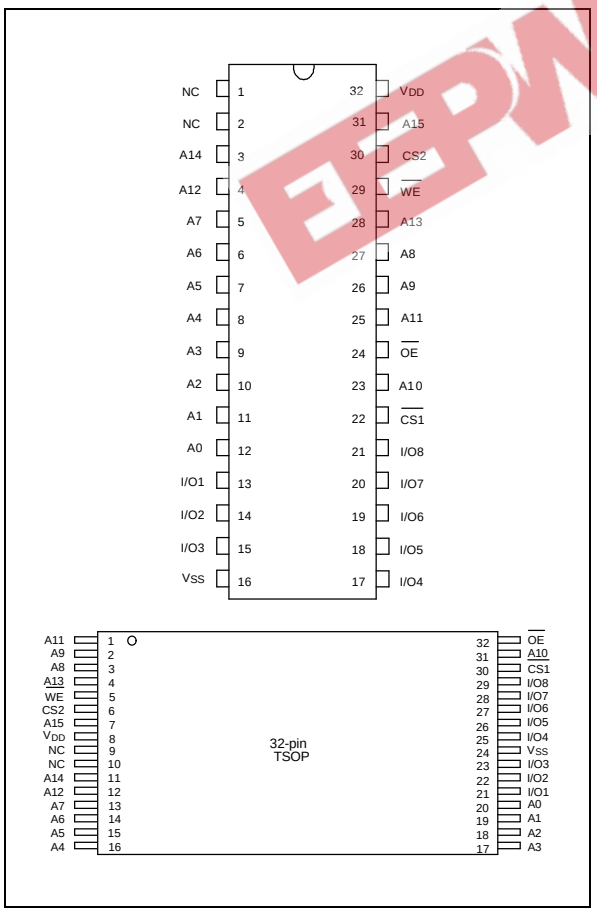
GENERAL DESCRIPTION

The W24512A is a high speed, low power CMOS static RAM organized as 65536 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

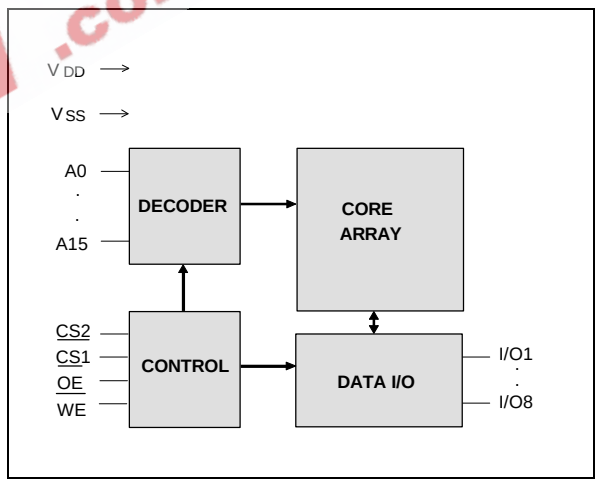
FEATURES

- High speed access time: 15/20/25/35 nS (max.)
- Low power consumption:
  - Active: 500 mW (typ.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 32-pin 300 mil SOJ, skinny DIP, 450 mil SOP, and standard type one TSOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A15	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	I/O1- I/O8	V_{DD} CURRENT
H	X	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Input/Output to V_{SS} Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD} $\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-10	-	+10	µA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH} I/O = 0 mA, Cycle = min. Duty = 100%	15	-	-	200	mA
			20			160	
			25			160	
			35	-	-	140	
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} Cycle = min., Duty = 100%		-	-	30	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{DD} -0.2V or CS2 ≤ 0.2V		-	-	10	mA

Note: Typical characteristics are at V_{DD} = 5V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	10	pF

Note: These parameters are sampled but not 100% tested.

THERMAL RESISTANCE

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Junction to Case Thermal Resistance	θ_{JC}	A. F. R. = 1m/sec, T_A = 25° C	20	°C/W
Junction to Ambient Thermal Resistance	θ_{JA}	A. F. R. = 1m/sec, T_A = 25° C	60	°C/W

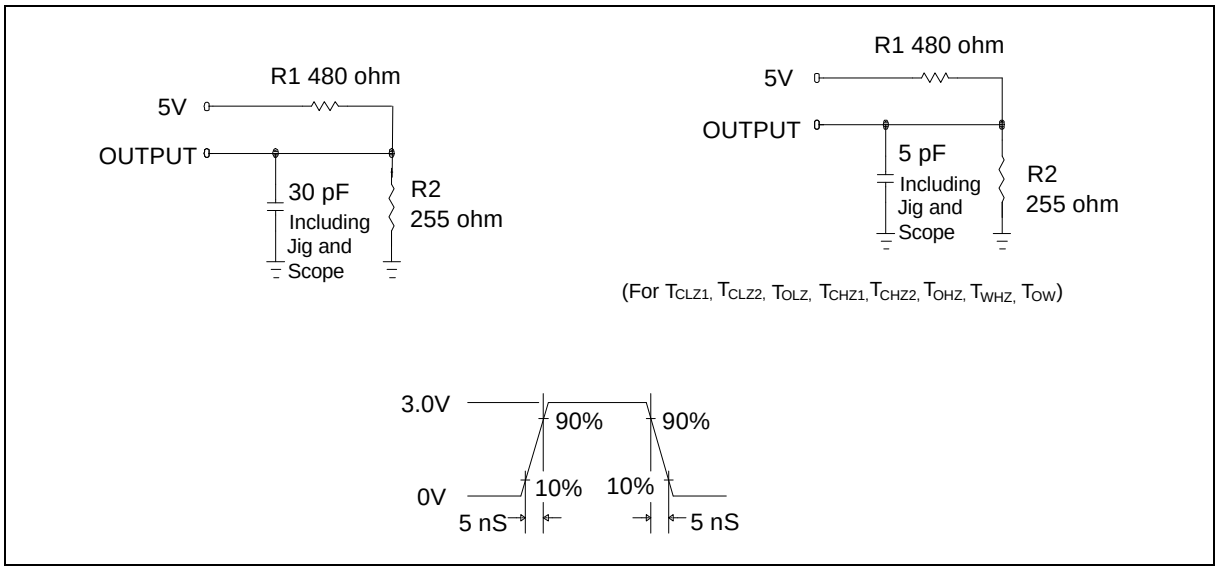
Note: These parameters are only applied to "TSOP" and "SOJ" package types.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC Test Loads and Waveform



AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER		SYM.	W24512A-15		W24512A-25		W24512A-25		W24512A-35		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time		T_{RC}	15	-	20	-	25	-	35	-	nS
Address Access Time		T_{AA}	-	15	-	20	-	25	-	35	nS
Chip Select Access Time	$\overline{CS1}$	T_{ACS1}	-	15	-	20	-	25	-	35	nS
	CS2	T_{ACS2}	-	15	-	20	-	25	-	35	nS
Output Enable to Output Valid		T_{AOE}	-	7	-	10	-	12	-	17	nS
Chip Selection to Output in Low Z	$\overline{CS1}$	T_{CLZ1}*	3	-	3	-	3	-	3	-	nS
	CS2	T_{CLZ2}*	3	-	3	-	3	-	3	-	nS
Output Enable to Output in Low Z		T_{OLZ}*	0	-	0	-	0	-	0	-	nS
Chip Deselection to Output in High Z	$\overline{CS1}$	T_{CHZ1}*	-	7	-	10	-	12	-	17	nS
	CS2	T_{CHZ2}*	-	7	-	10	-	12	-	17	nS
Output Disable to Output in High Z		T_{OHZ}*	-	7	-	1	-	12	-	17	nS
Output Hold from Address Change		T_{OH}	3	-	3	-	3	-	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

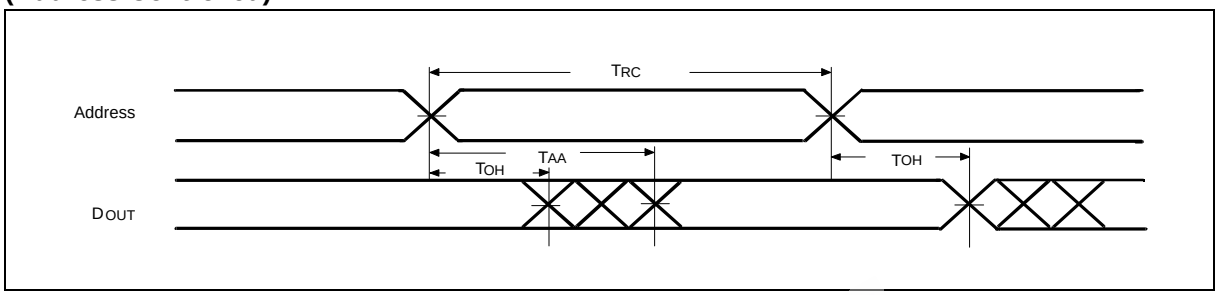
PARAMETER		SYM.	W24512A-15		W24512A-25		W24512A-25		W24512A-35		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	15	-	20	-	25	-	35	-	nS
Chip Selection to End of Write	$\overline{CS1}$	T_{CW1}	13	-	17	-	18	-	20	-	nS
	CS2	T_{CW2}	13	-	17	-	18	-	20	-	nS
Address Valid to End of Write		T_{AW}	13	-	17	-	18	-	20	-	nS
Address Setup Time		T_{AS}	0	-	0	-	0	-	0	-	nS
Write Pulse Width		T_{WP}	10	-	12	-	15	-	18	-	nS
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	T_{WR1}	0	-	0	-	0	-	0	-	nS
	CS2	T_{WR2}	0	-	0	-	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	9	-	10	-	12	-	15	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	8	-	10	-	12	-	15	nS
Output Disable to Output in High Z		T_{OHZ}*	-	8	-	10	-	12	-	15	nS
Output Active from End of Write		T_{OW}	0	-	0	-	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

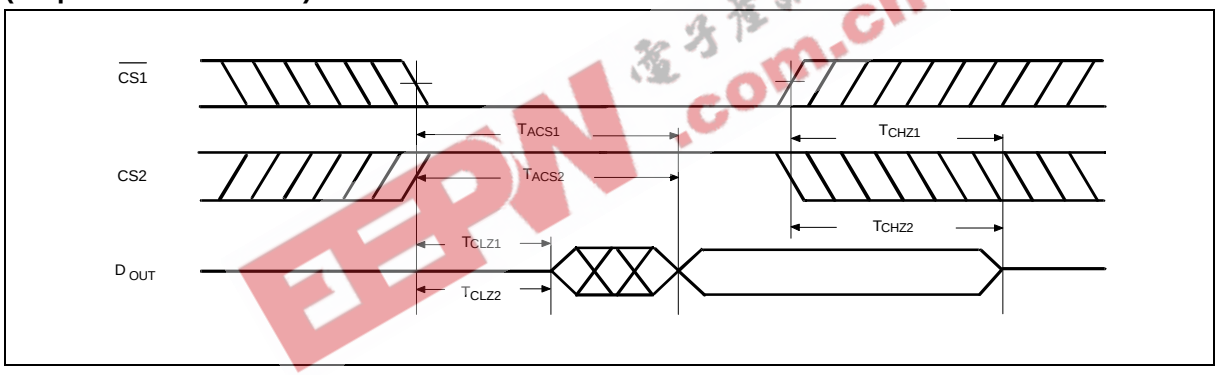
Read Cycle 1

(Address Controlled)



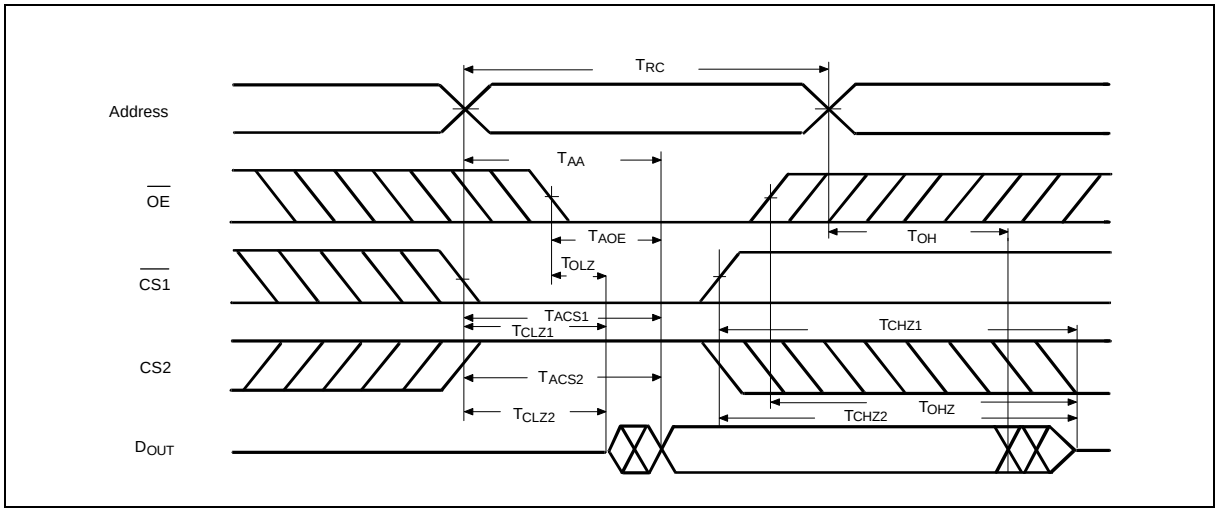
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

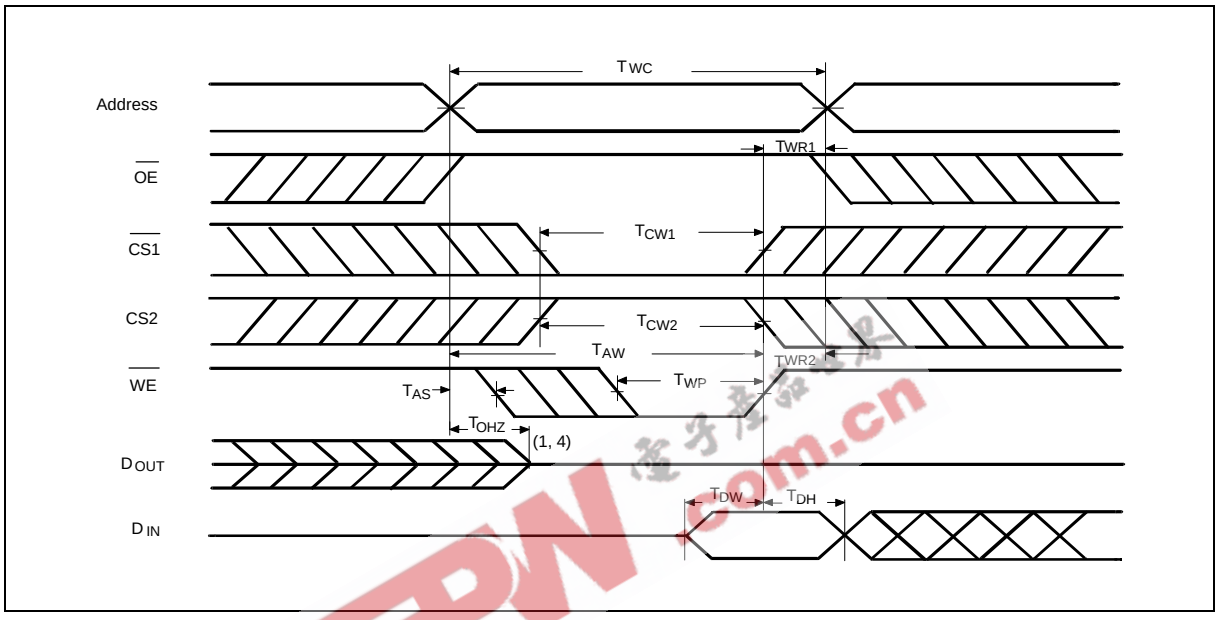
(Output Enable Controlled)



Timing Waveforms, continued

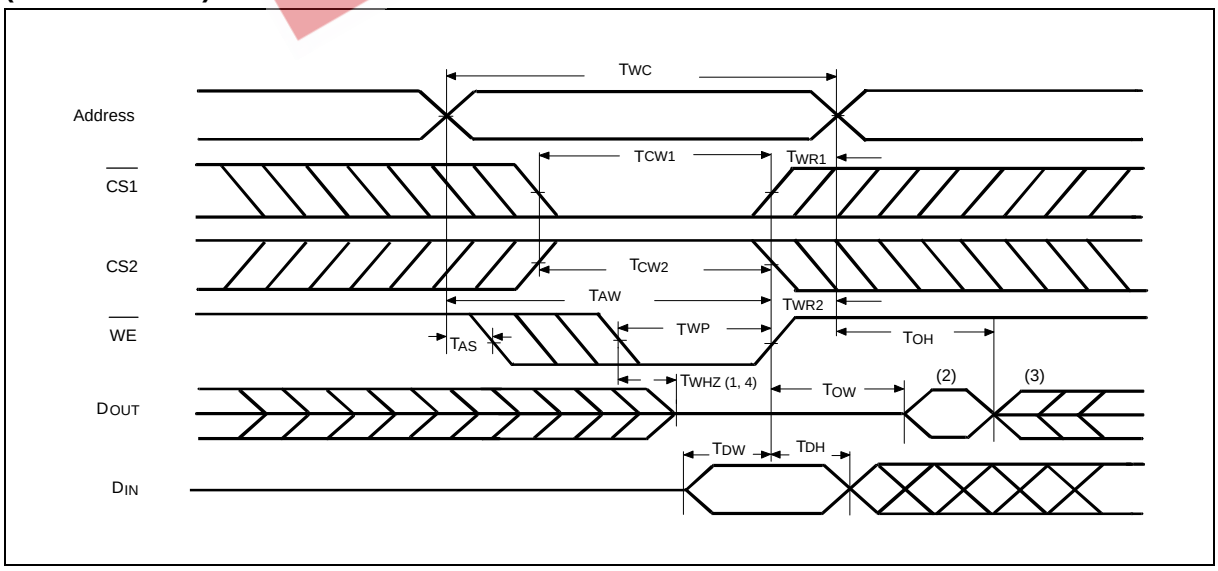
Write Cycle 1

($\overline{OE}$ Clock)



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24512AK-15	15	200	10	300 mil skinny DIP
W24512AK-20	20	160	10	300 mil skinny DIP
W24512AK-25	25	160	10	300 mil skinny DIP
W24512AK-35	35	140	10	300 mil skinny DIP
W24512AJ-15	15	200	10	300 mil SOJ
W24512AJ-20	20	160	10	300 mil SOJ
W24512AJ-25	25	160	10	300 mil SOJ
W24512AJ-35	35	140	10	300 mil SOJ
W24512AS-15	15	200	10	450 mil SOP
W24512AS-20	20	160	10	450 mil SOP
W24512AS-25	25	160	10	450 mil SOP
W24512AS-35	35	140	10	450 mil SOP
W24512AT-15	15	200	10	standard type one TSOP
W24512AT-20	20	160	10	standard type one TSOP
W24512AT-25	25	160	10	standard type one TSOP
W24512AT-35	35	140	10	standard type one TSOP

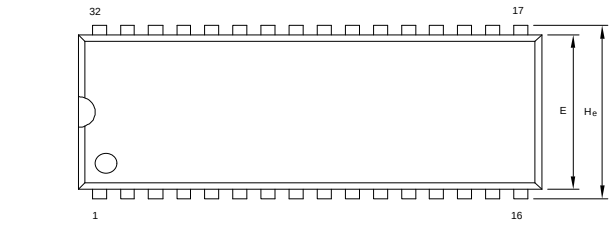
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

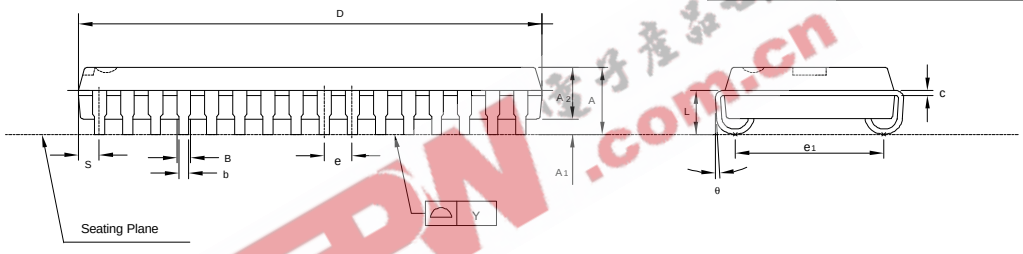
Winbond Electronics Corp.

PACKAGE DIMENSIONS

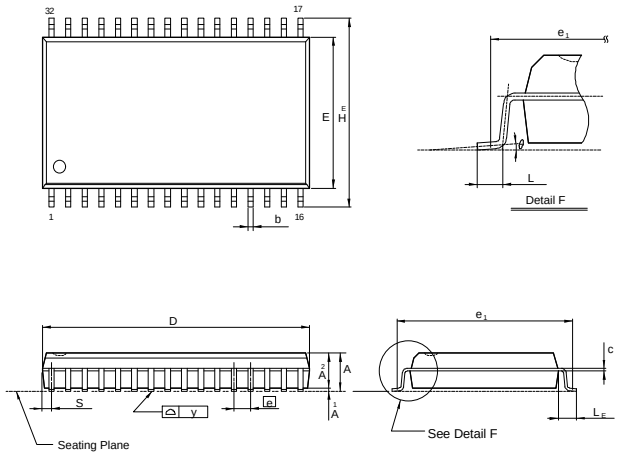
32-pin SOJ



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.140			3.556
A_1	0.020	—	—	0.508	—	—
A_2	0.095	0.100	0.105	2.413	2.540	2.667
B	0.026	0.028	0.032	0.660	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.815	0.825	0.835	20.701	20.955	21.209
E	0.295	0.300	0.305	7.493	7.620	7.747
e	0.044	0.050	0.056	1.118	1.270	1.422
e_1	0.247	0.267	0.287	6.274	6.782	7.290
H_e	0.325	0.335	0.345	8.255	8.509	8.763
L	0.080	—		2.032	—	
S	—	—	0.045	—	—	1.143
Y	—	—	0.004		—	0.102
θ	0	—	10	0°	—	10°



32-pin SO Wide Body

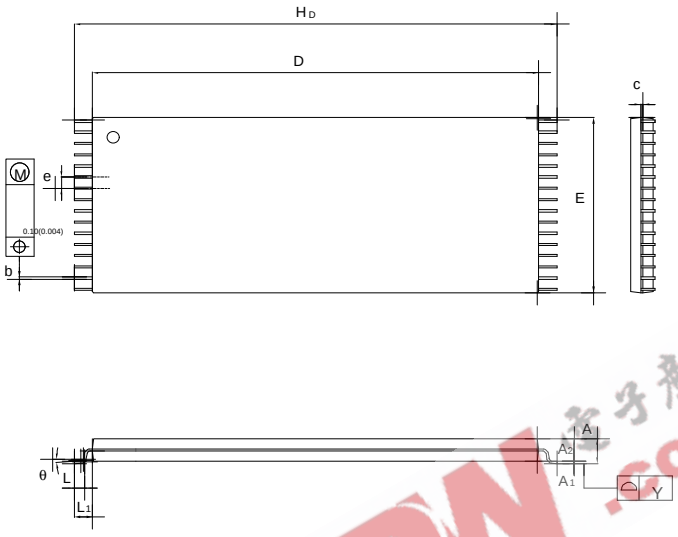


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.118	—	—	3.00
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	—	0.805	0.817	—	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.556	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	—	—	0.036	—	—	0.91
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

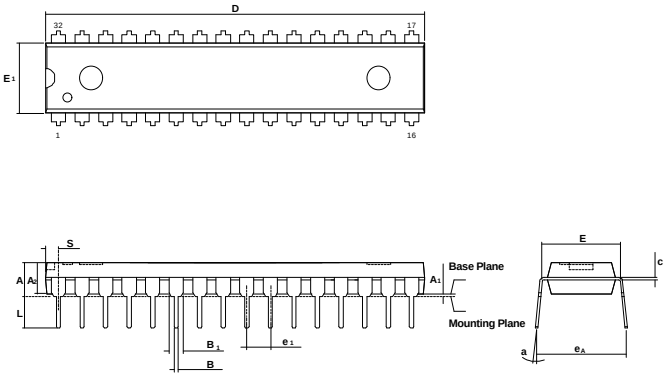
32-pin TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:
Controlling dimension: Millimeter

32-pin P-DIP Skinny (300 mil)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.200	—	—	5.08
A_1	0.015	—	—	0.38	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.60	1.62	—	40.64	41.15
E	0.295	0.315	0.335	7.49	8.00	8.50
E_1	0.286	0.290	0.294	7.26	7.36	7.46
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0°	—	15°
e_A	0.430	0.450	0.470	10.92	11.43	11.94
S	—	—	0.065	—	—	1.65

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based or final visual inspection spec.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A7	Mar. 1999	-	Arrange access time for 15/20/25/35 nS

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